

- 28:4 Data Channel Compression at up to 227.5 Million Bytes per Second Throughput
- Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI
- 28 Data Channels and Clock-In Low-Voltage TTL
- 4 Data Channels and Clock-Out Low-Voltage Differential
- Operates From a Single 3.3-V Supply With 250 mW (Typ)
- ESD Protection Exceeds 6 kV
- 5-V Tolerant Data Inputs
- Selectable Rising or Falling Edge-Triggered Inputs
- Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch
- Consumes Less Than 1 mW When Disabled
- Wide Phase-Lock Input Frequency Range . . . 31 MHz to 68 MHz
- No External Components Required for PLL
- Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
- Improved Replacement for the DS90C581

## description

The SN75LVDS83 FlatLink transmitter contains four 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and five low-voltage differential-signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended low-voltage TTL (LVTTTL) data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82. The SN75LVDS83 can also be used in 21-bit links with the SN75LVDS86 receiver.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected by way of the clock select (CLKSEL) terminal. The frequency of CLKIN is multiplied seven times (7×) and then used to unload the data registers in 7-bit slices and serially. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN75LVDS83 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user. The only user intervention is the possible use of the shutdown/clear ( $\overline{\text{SHTDN}}$ ) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level signal on  $\overline{\text{SHTDN}}$  clears all internal registers to a low level.

The SN75LVDS83 is characterized for operation over free-air temperature ranges of 0°C to 70°C.

## DGG PACKAGE (TOP VIEW)

V <sub>CC</sub>	1	56	D4
D5	2	55	D3
D6	3	54	D2
D7	4	53	GND
GND	5	52	D1
D8	6	51	D0
D9	7	50	D27
D10	8	49	LVDSGND
V <sub>CC</sub>	9	48	Y0M
D11	10	47	Y0P
D12	11	46	Y1M
D13	12	45	Y1P
GND	13	44	LVDSV <sub>CC</sub>
D14	14	43	LVDSGND
D15	15	42	Y2M
D16	16	41	Y2P
CLKSEL	17	40	CLKOUTM
D17	18	39	CLKOUTP
D18	19	38	Y3M
D19	20	37	Y3P
GND	21	36	LVDSGND
D20	22	35	PLL <sub>GND</sub>
D21	23	34	PLL <sub>V<sub>CC</sub></sub>
D22	24	33	PLL <sub>GND</sub>
D23	25	32	$\overline{\text{SHTDN}}$
V <sub>CC</sub>	26	31	CLKIN
D24	27	30	D26
D25	28	29	GND



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FlatLink is a registered trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



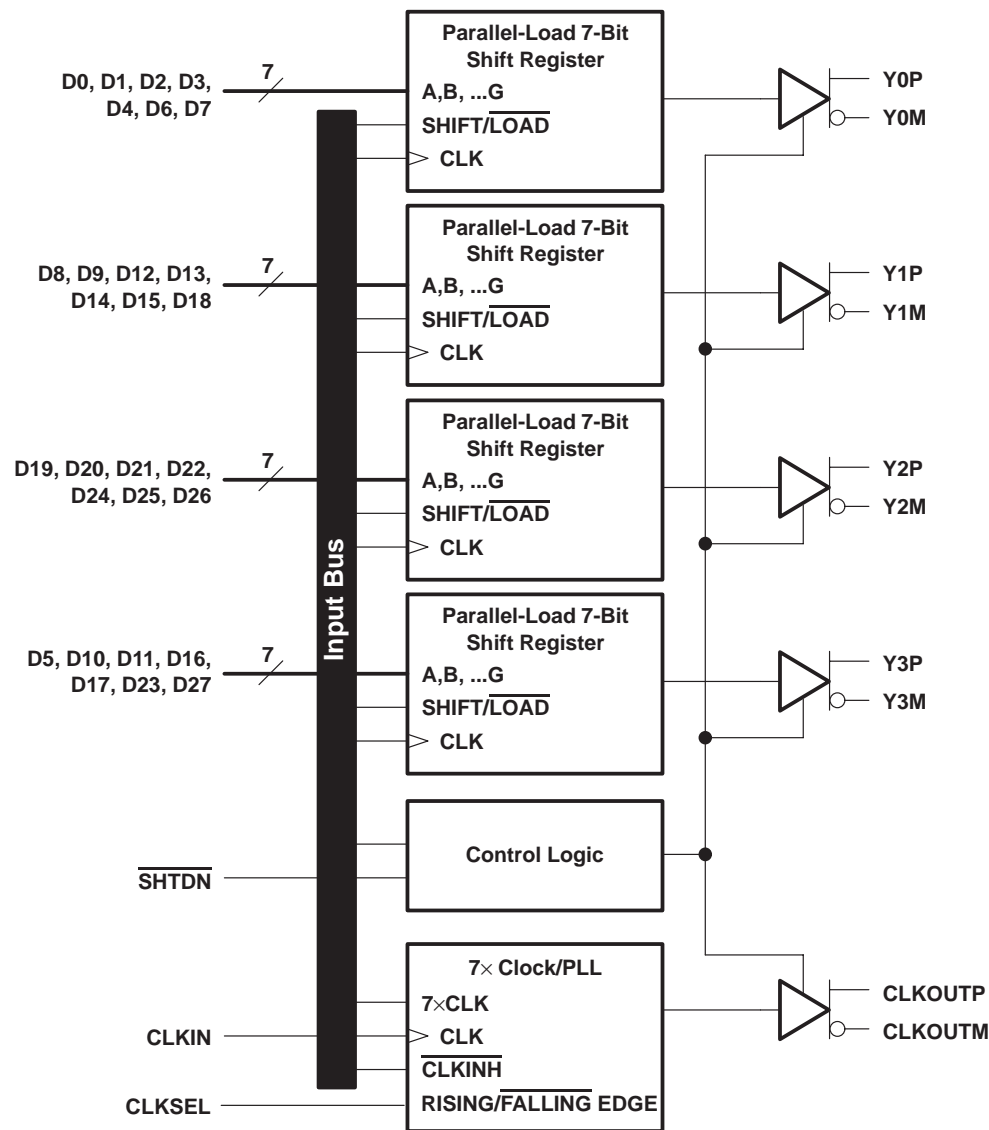
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

SN75LVDS83  
FLATLINK™ TRANSMITTER

SLLS271C – MARCH 1997 – REVISED JULY 2000

functional block diagram



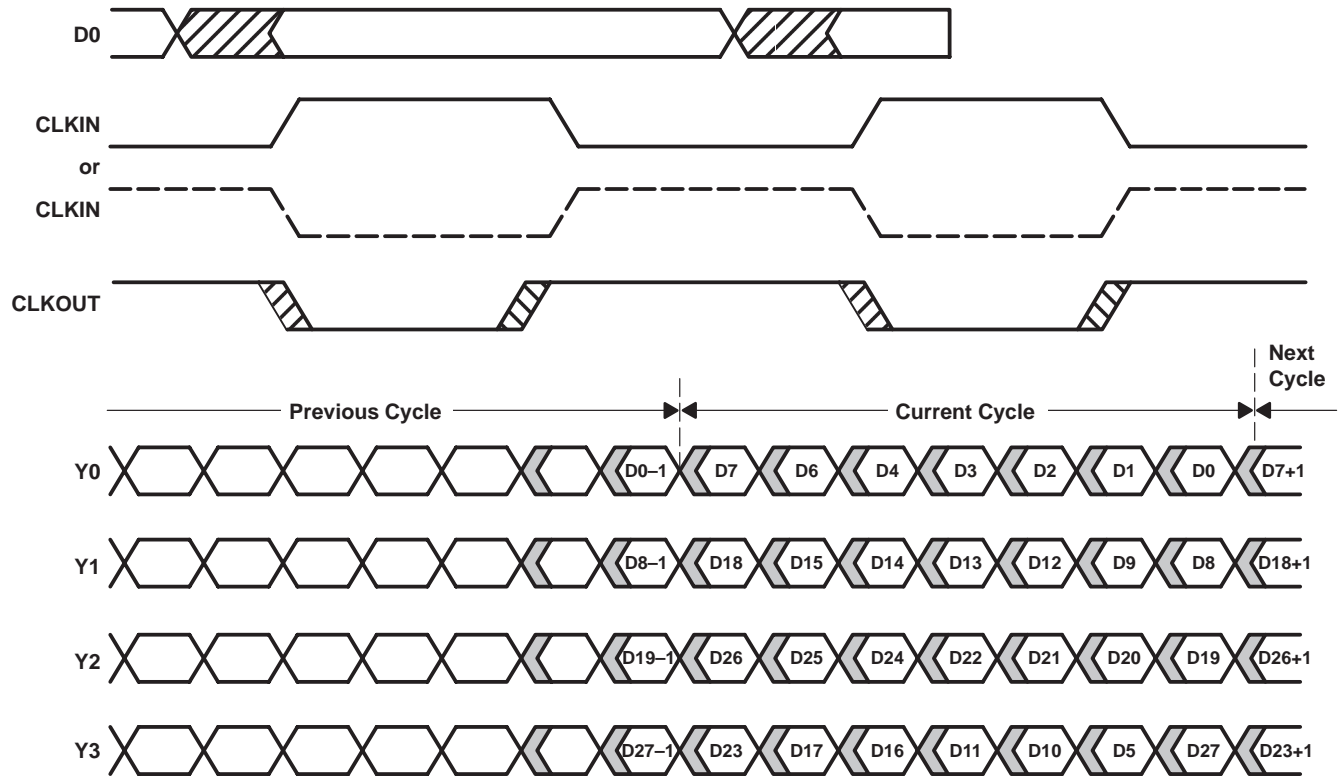
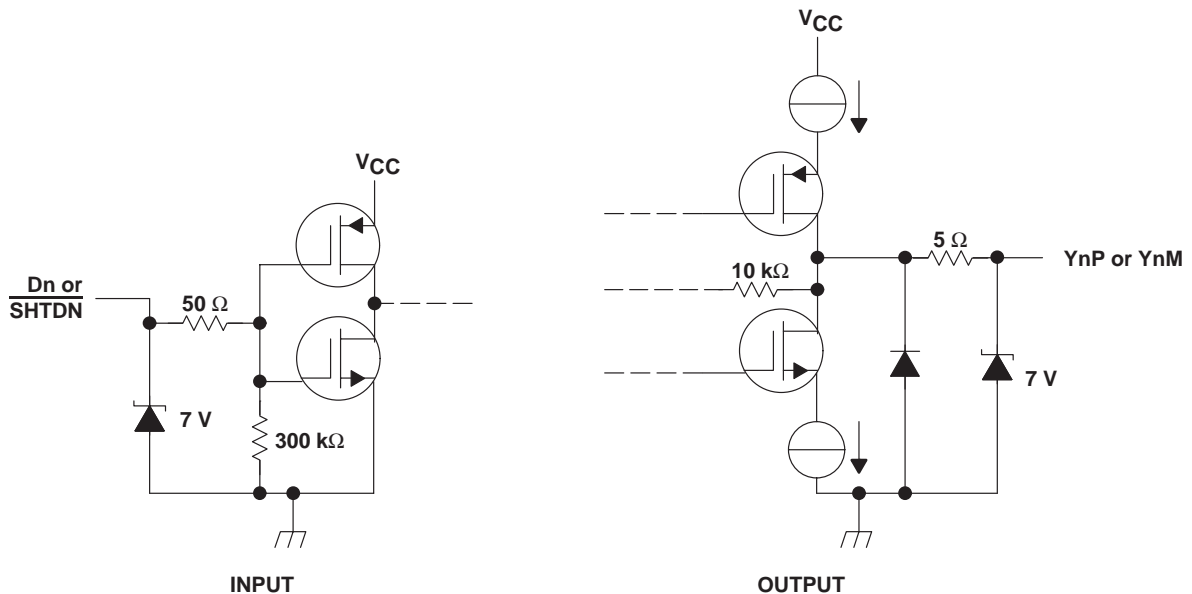


Figure 1. SN75LVDS83 Load and Shift Timing Sequences

equivalent input and output schematic diagrams



# SN75LVDS83 FLATLINK™ TRANSMITTER

SLLS271C – MARCH 1997 – REVISED JULY 2000

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 4 V
Output voltage range, $V_O$ (all terminals)	–0.5 V to $V_{CC} + 0.5$ V
Input voltage range, $V_I$ (all terminals)	–0.5 V to 5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DGG	1377 mW	11.0 mW/°C	822 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	3	3.3	3.6	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
Differential load impedance, $Z_L$	90		132	$\Omega$
Operating free-air temperature, $T_A$	0		70	°C

## timing requirements

	MIN	NOM	MAX	UNIT
$t_C$ Cycle time, input clock	14.7		32.4	ns
$t_W$ Pulse duration, high-level input clock	$0.4t_C$		$0.6t_C$	ns
$t_t$ Transition time, input signal			5	ns
$t_{su}$ Setup time, data, D0 – D27 valid before $CLKIN\uparrow$ or $CLKIN\downarrow$ (see Figure 2)	3			ns
$t_h$ Hold time, data, D0 – D27 valid after $CLKIN\uparrow$ or $CLKIN\downarrow$ (see Figure 2)	1.5			ns



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IT}$	Input threshold voltage			1.4		V
$ V_{OD} $	Differential steady-state output voltage magnitude	$R_L = 100\ \Omega$ , See Figure 3	247		454	mV
$\Delta V_{OD} $	Change in the steady-state differential output voltage magnitude between opposite binary states				50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$I_{IH}$	High-level input current	$V_{IH} = V_{CC}$			25	$\mu A$
$I_{IL}$	Low-level input current	$V_{IL} = 0$			$\pm 10$	$\mu A$
$I_{OS}$	Short-circuit output current	$V_{O(Yn)} = 0$			$\pm 24$	mA
		$V_{OD} = 0$			$\pm 12$	mA
$I_{OZ}$	High-impedance state output current	$V_O = 0$ to $V_{CC}$			$\pm 10$	$\mu A$
$I_{CC}$	Quiescent supply current	Disabled, All inputs at GND			280	$\mu A$
		Enabled, $R_L = 100\ \Omega$ , Gray-scale pattern (see Figure 4), $V_{CC} = 3.3\ V$ , $t_c = 15.38\ ns$		72	90	mA
		Enabled, $R_L = 100\ \Omega$ , Worst-case pattern (see Figure 5), $t_c = 15.38\ ns$		85	110	mA
$C_I$	Input capacitance			3		pF

† All typical values are at  $V_{CC} = 3.3\ V$ ,  $T_A = 25^\circ C$ .

# SN75LVDS83 FLATLINK™ TRANSMITTER

SLLS271C – MARCH 1997 – REVISED JULY 2000

## switching characteristics over recommended operating conditions (unless otherwise noted)

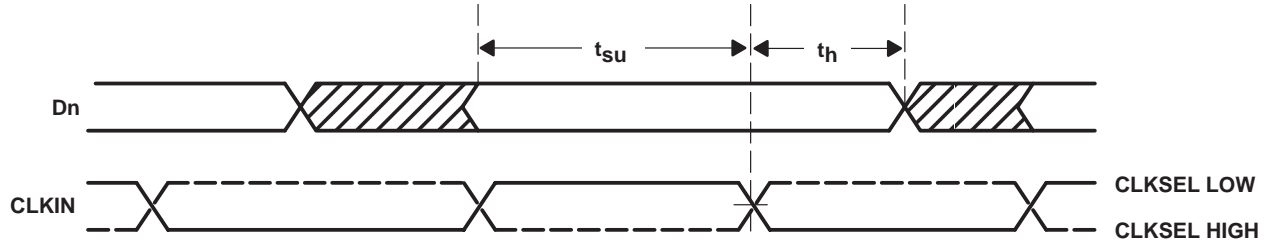
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>d0</sub> Delay time, CLKOUT↑ to serial bit position 0	t <sub>C</sub> = 15.38 ns (± 0.2%),  Input clock jitter  < 50 ps‡, See Figure 6	-0.2	0	0.2	ns
t <sub>d1</sub> Delay time, CLKOUT↑ to serial bit position 1		$\frac{1}{7}t_C - 0.2$		$\frac{1}{7}t_C + 0.2$	ns
t <sub>d2</sub> Delay time, CLKOUT↑ to serial bit position 2		$\frac{2}{7}t_C - 0.2$		$\frac{2}{7}t_C + 0.2$	ns
t <sub>d3</sub> Delay time, CLKOUT↑ to serial bit position 3		$\frac{3}{7}t_C - 0.2$		$\frac{3}{7}t_C + 0.2$	ns
t <sub>d4</sub> Delay time, CLKOUT↑ to serial bit position 4		$\frac{4}{7}t_C - 0.2$		$\frac{4}{7}t_C + 0.2$	ns
t <sub>d5</sub> Delay time, CLKOUT↑ to serial bit position 5		$\frac{5}{7}t_C - 0.2$		$\frac{5}{7}t_C + 0.2$	ns
t <sub>d6</sub> Delay time, CLKOUT↑ to serial bit position 6		$\frac{6}{7}t_C - 0.2$		$\frac{6}{7}t_C + 0.2$	ns
t <sub>sk(o)</sub> Output skew, t <sub>n</sub> - $\frac{n}{7}t_C$		-0.2		0.2	ns
t <sub>d7</sub> Delay time, CLKIN↓ to CLKOUT↑	t <sub>C</sub> = 18.51 ns (± 0.2%),  Input clock jitter  < 50 ps‡, See Figure 6	3.75	5.6	7.75	ns
Δt <sub>C(o)</sub> Cycle time, output clock jitter§	t <sub>C</sub> = 15.38 ± 0.75 sin (2π500E3t) + 0.05 ns, See Figure 7		±70		ps
	t <sub>C</sub> = 15.38 ± 0.75 sin (2π3E6t) + 0.05 ns, See Figure 7		±187		ps
t <sub>w</sub> Pulse duration, high-level output clock			$\frac{4}{7}t_C$		ns
t <sub>t</sub> Transition time, differential output (t <sub>r</sub> or t <sub>f</sub> )	See Figure 3	260	700	1500	ps
t <sub>en</sub> Enable time, SHTDN↑ to phase lock (Y <sub>n</sub> valid)	See Figure 8		1		ms
t <sub>dis</sub> Disable time, SHTDN↓ to off state (CLKOUT low)	See Figure 9		250		ns

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ |Input clock jitter| is the magnitude of the change in the input clock period.

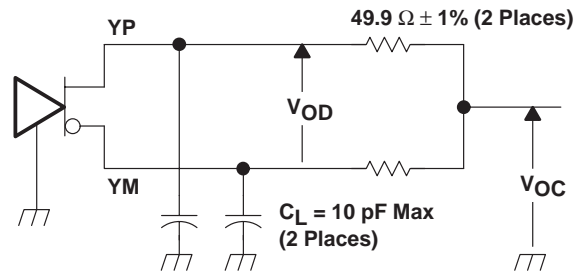
§ Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15000 cycles.

## PARAMETER MEASUREMENT INFORMATION



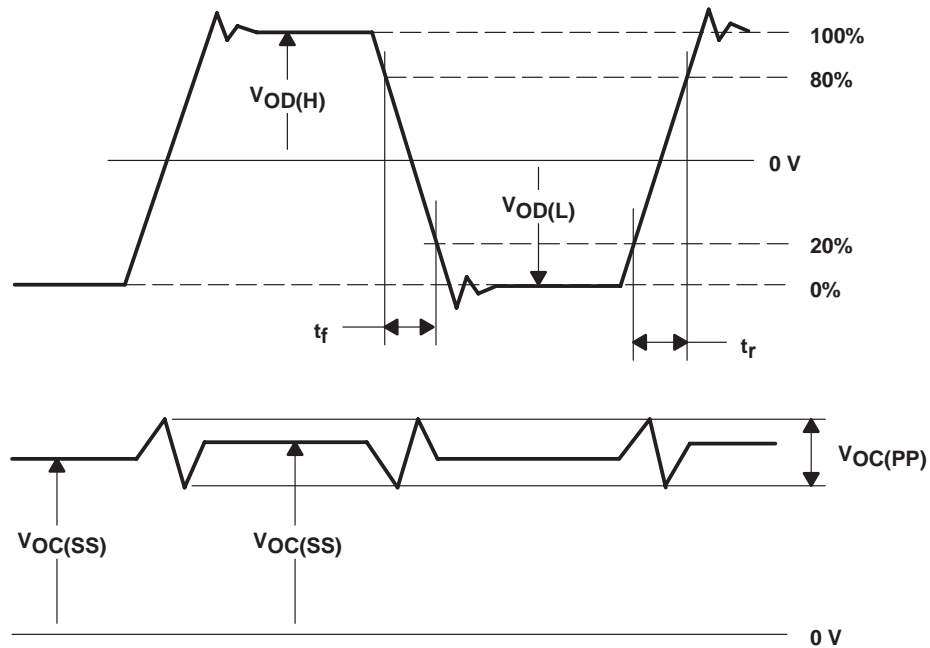
NOTE A: All input timing is defined at 1.4 V on an input signal with a 10%-to-90% rise or fall time of less than 5 ns.

Figure 2. Setup and Hold Time Waveforms



NOTE A: The lumped instrumentation capacitance for any single-ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output is similarly loaded.

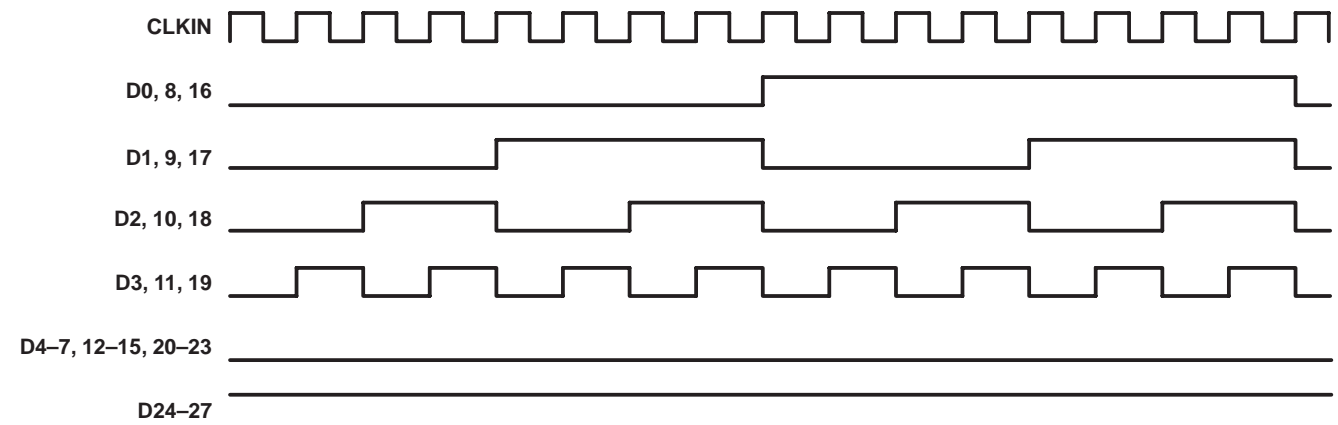
(a) SCHEMATIC



(b) WAVEFORMS

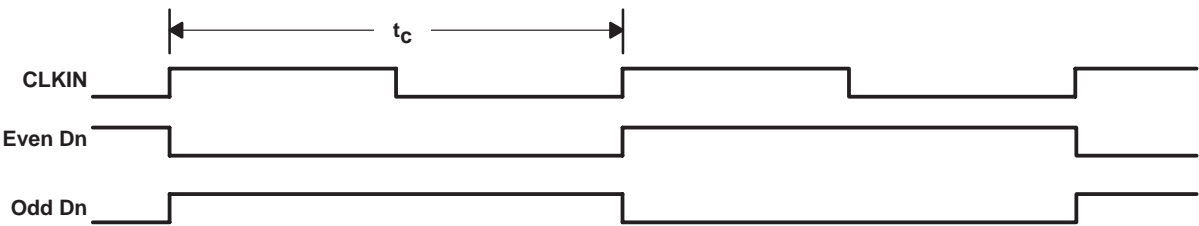
Figure 3. Test Load and Voltage Waveforms for LVDS Outputs

PARAMETER MEASUREMENT INFORMATION



NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern. Pattern with CLKSEL low shown.

Figure 4. 16-Grayscale Test-Pattern Waveforms

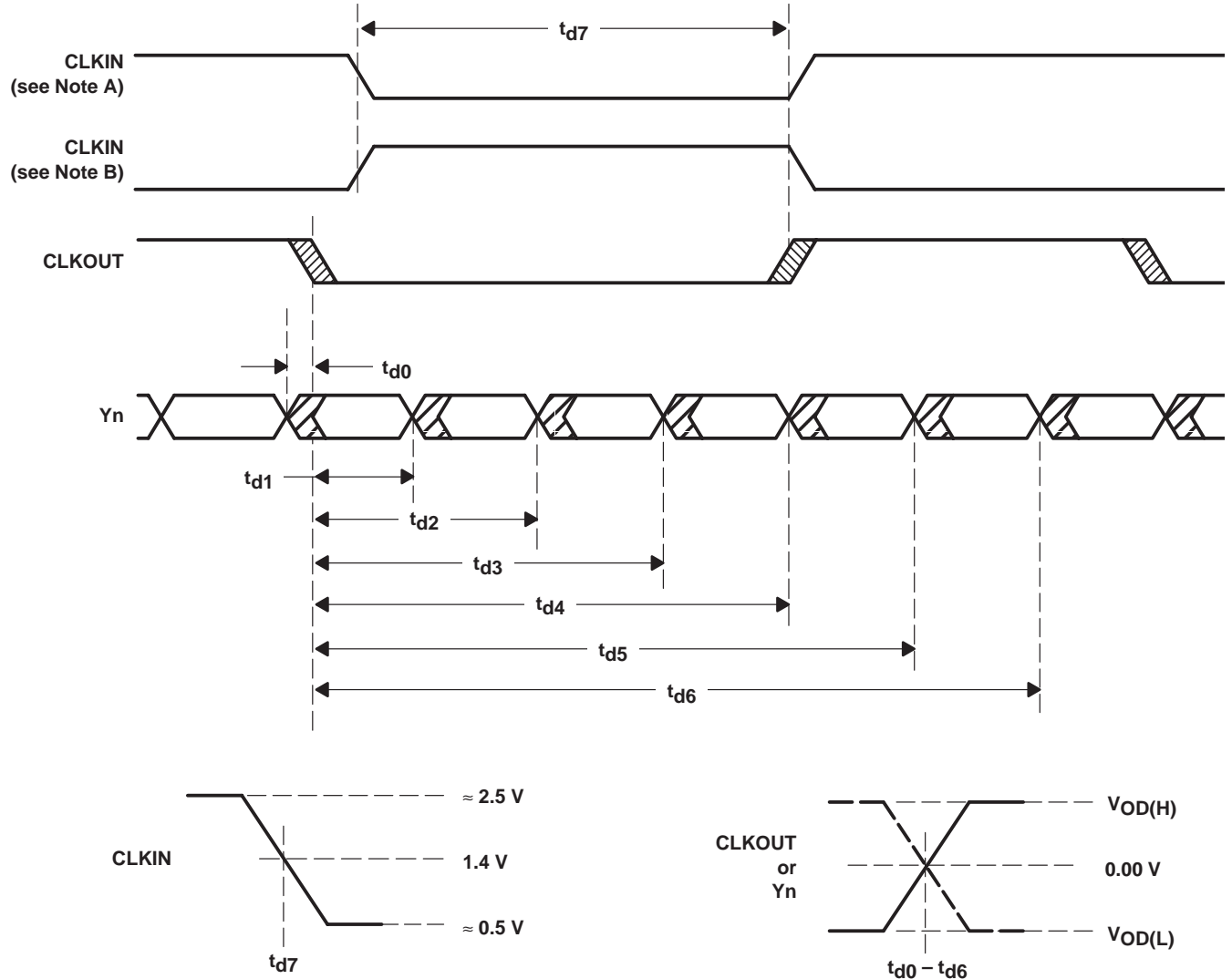


NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs. Pattern with CLKSEL low shown.

Figure 5. Worst-Case Test-Pattern Waveforms



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. This wave form is valid when CLKSEL is low.  
B. This wave form is valid when CLKSEL is high.

Figure 6. SN75LVDS83 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

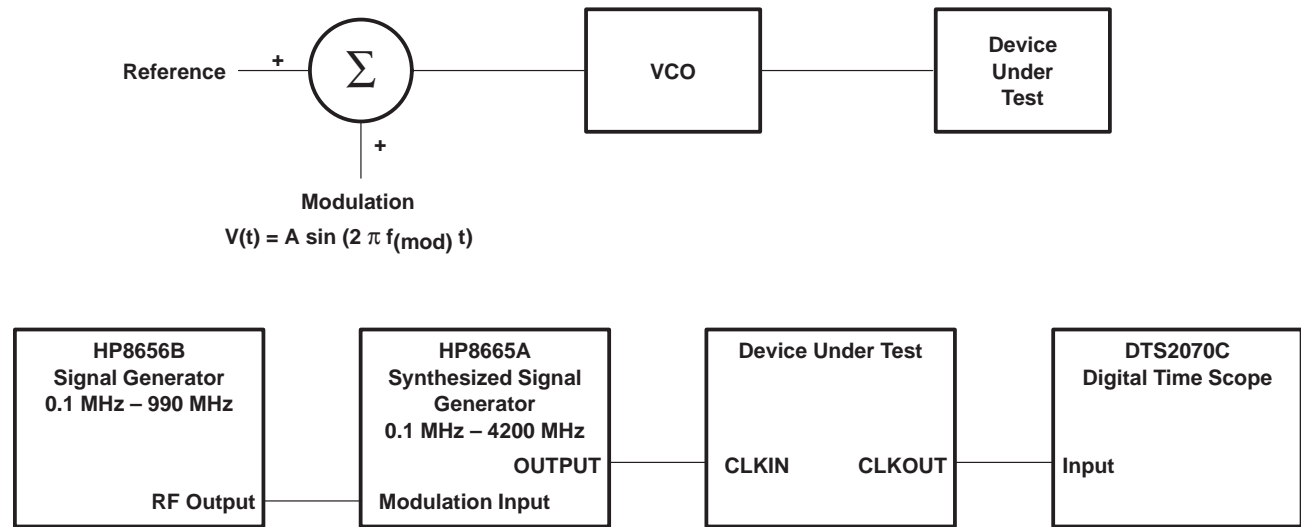


Figure 7. Output Clock Jitter Testing

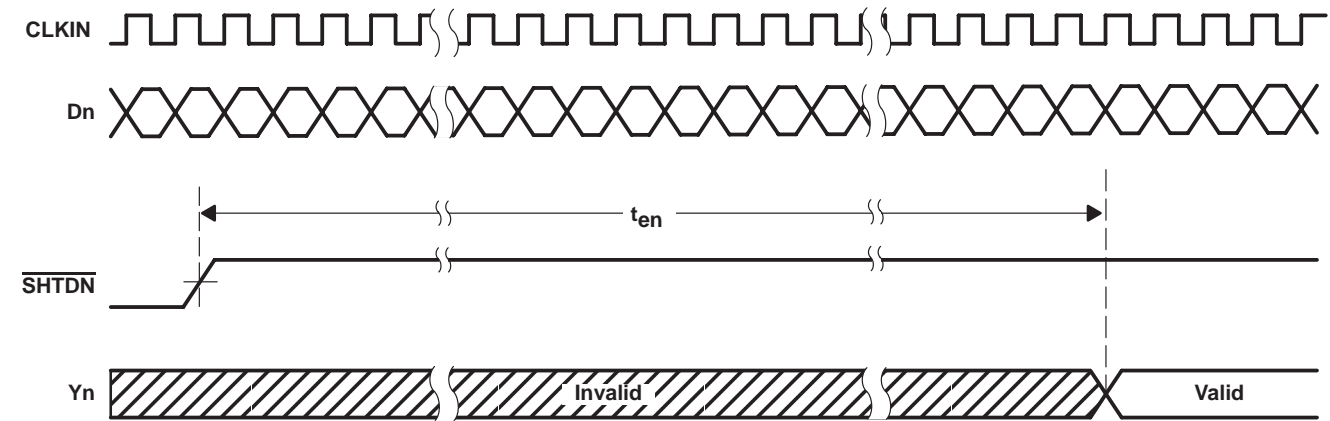


Figure 8. Enable Time Waveforms

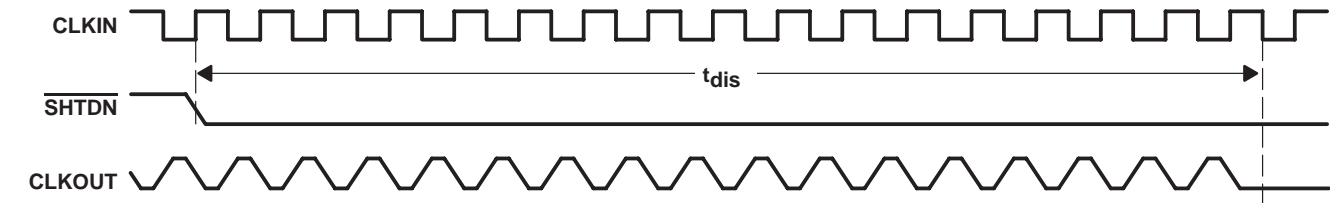


Figure 9. Disable Time Waveforms

## TYPICAL CHARACTERISTICS

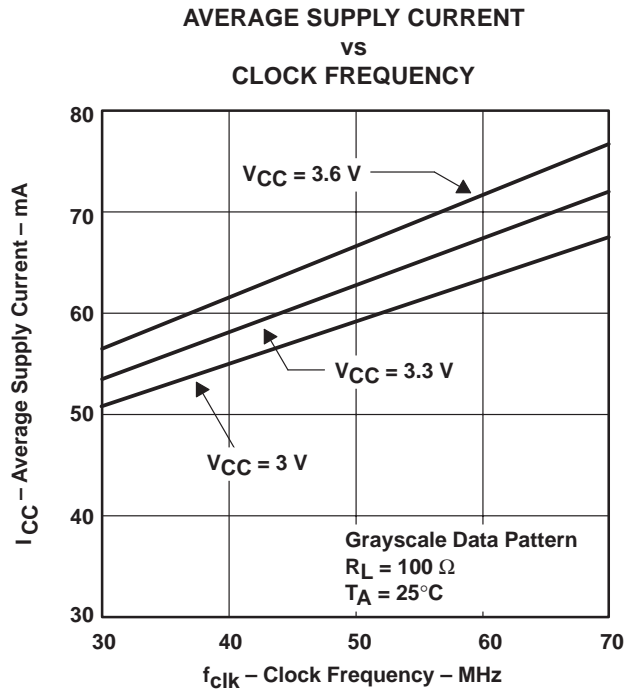


Figure 10

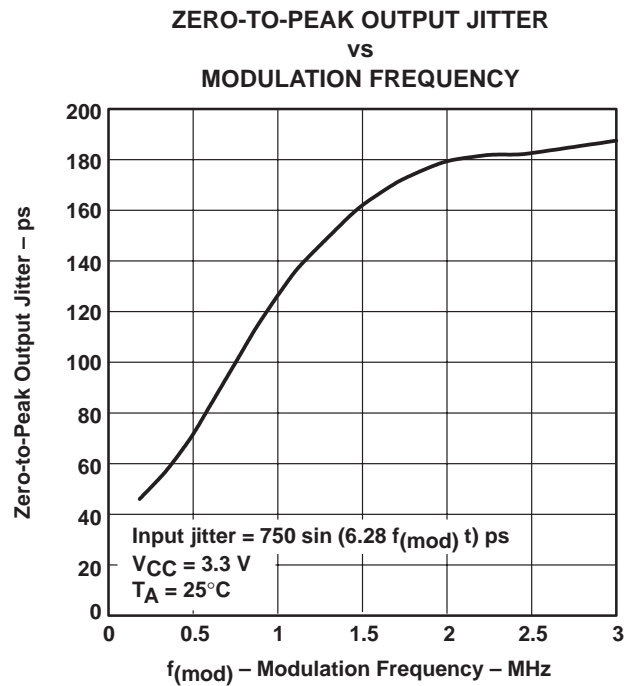
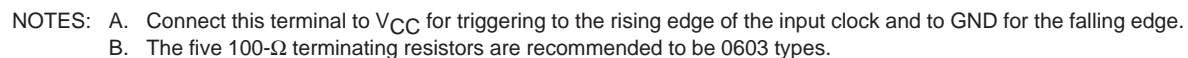


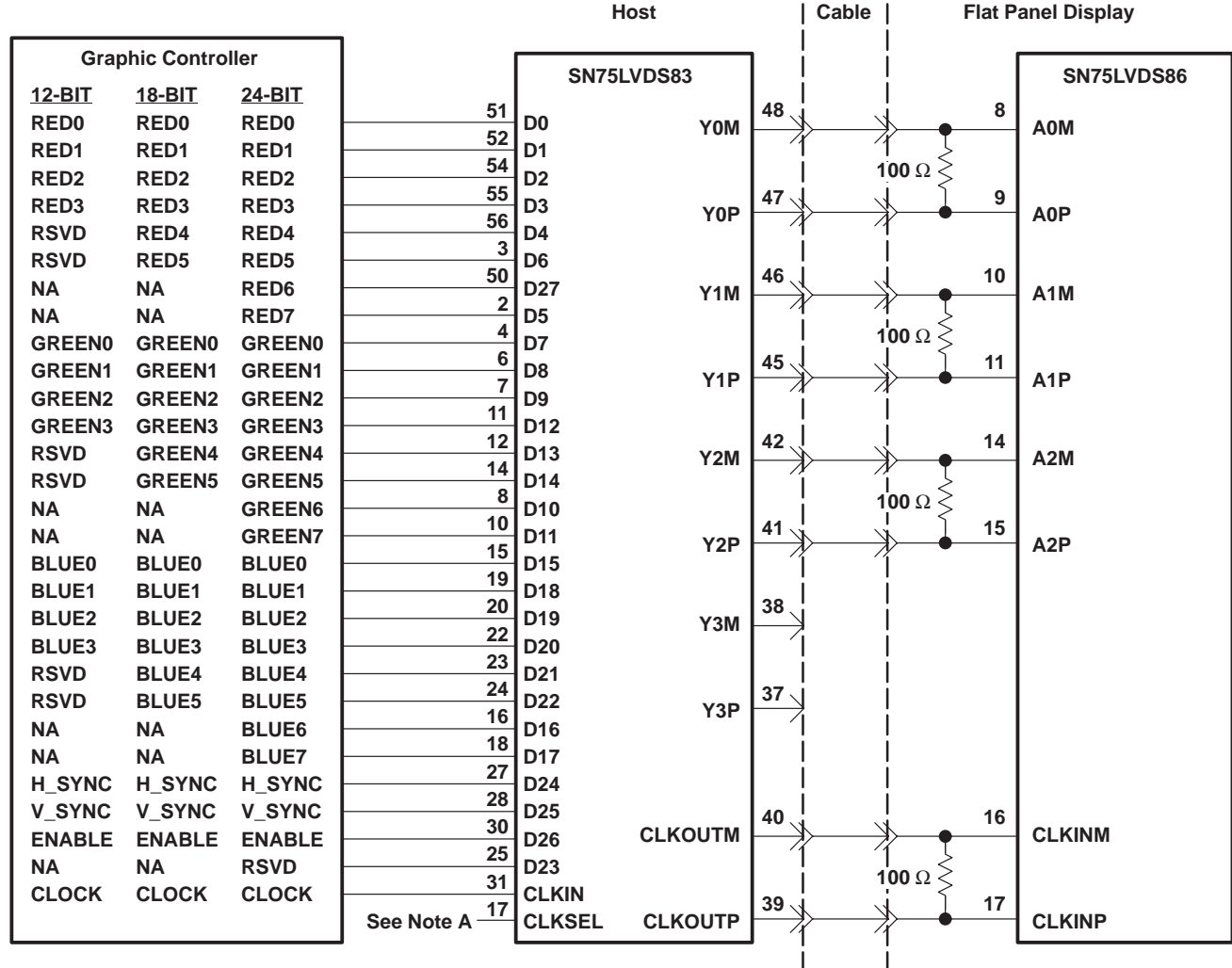
Figure 11

Host	Cable	Flat Panel Display
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15
16	16	16
17	17	17
18	18	18
19	19	19
20	20	20
21	21	21
22	22	22
23	23	23
24	24	24
25	25	25
26	26	26
27	27	27
28	28	28
29	29	29
30	30	30
31	31	31
32	32	32
33	33	33
34	34	34
35	35	35
36	36	36
37	37	37
38	38	38
39	39	39
40	40	40
41	41	41
42	42	42
43	43	43
44	44	44
45	45	45
46	46	46
47	47	47
48	48	48
49	49	49
50	50	50
51	51	51
52	52	52
53	53	53
54	54	54
55	55	55
56	56	56
57	57	57
58	58	58
59	59	59
60	60	60
61	61	61
62	62	62
63	63	63
64	64	64
65	65	65
66	66	66
67	67	67
68	68	68
69	69	69
70	70	70
71	71	71
72	72	72
73	73	73
74	74	74
75	75	75
76	76	76
77	77	77
78	78	78
79	79	79
80	80	80
81	81	81
82	82	82
83	83	83
84	84	84
85	85	85
86	86	86
87	87	87
88	88	88
89	89	89
90	90	90
91	91	91
92	92	92
93	93	93
94	94	94
95	95	95
96	96	96
97	97	97
98	98	98
99	99	99
100	100	100



### Figure 12. 24-Bit Color Host To 24-Bit LCD Panel Display Application

## APPLICATION INFORMATION



SN75LVDS83

FLATLINK™ TRANSMITTER

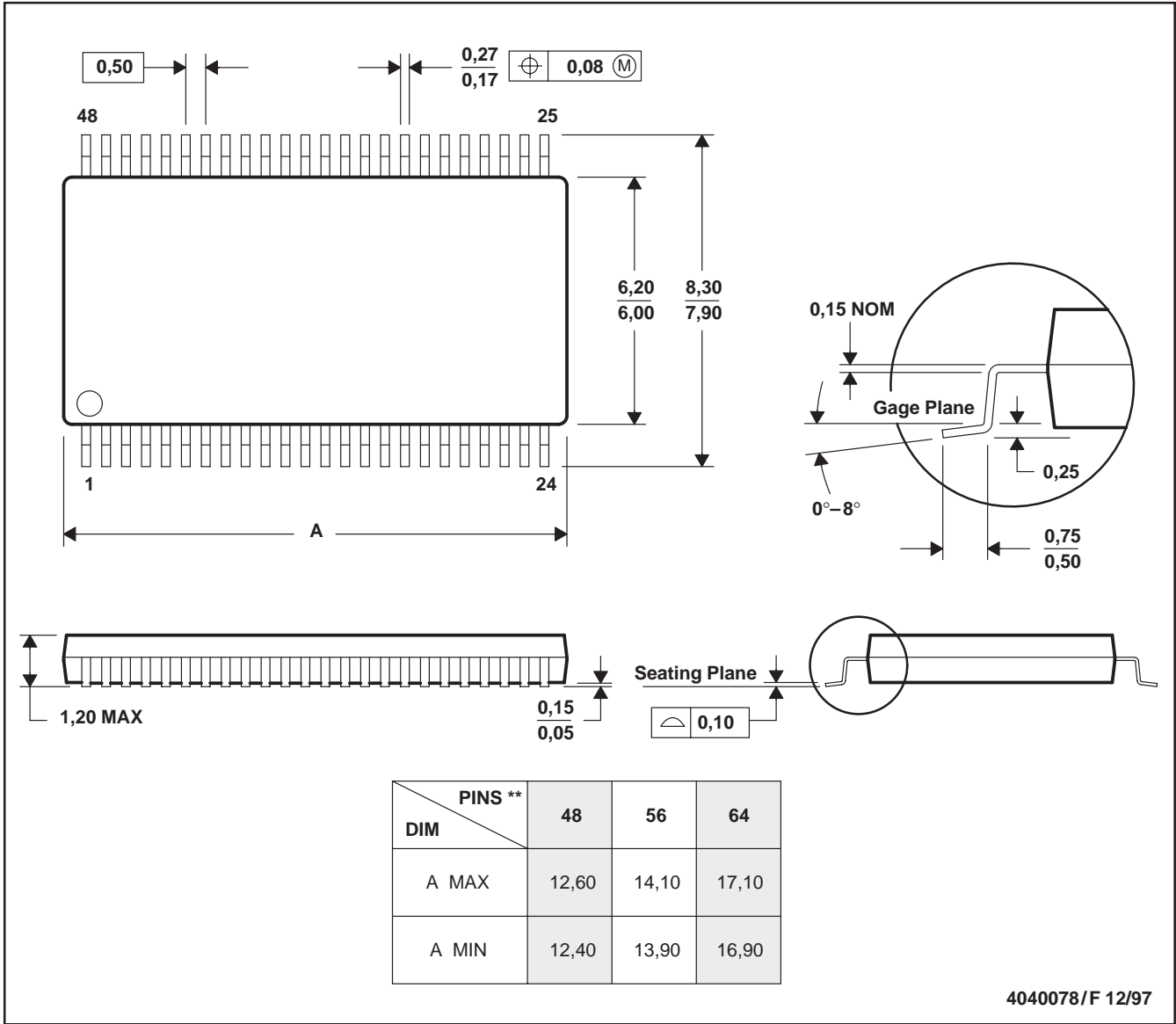
SLLS271C – MARCH 1997 – REVISED JULY 2000

MECHANICAL INFORMATION

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-153

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.