

# SN54HCT126, SN74HCT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCLS070A – NOVEMBER 1988 – REVISED NOVEMBER 1990

- High-Current 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Inputs Are TTL-Voltage Compatible
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

These bus buffers feature independent line drivers with 3-state outputs. Each output is disabled when the associated OE is low.

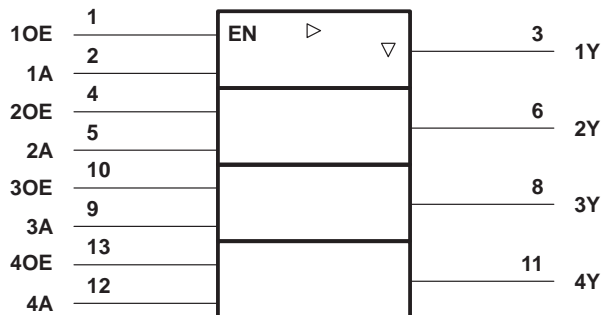
The SN54HCT126 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HCT126 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

H = high level, L = low level,  
X = irrelevant

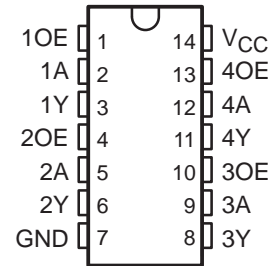
## logic symbol†



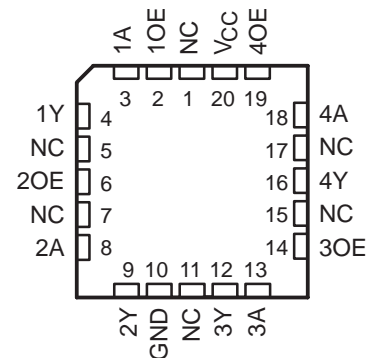
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

SN54HCT126 . . . J PACKAGE  
SN74HCT126 . . . D OR N PACKAGE  
(TOP VIEW)

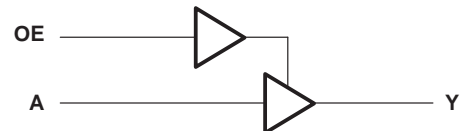


SN54HCT126 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## logic diagram, each buffer (positive logic)



# SN54HCT126, SN74HCT126

## QUADRUPLE BUS BUFFER GATES

### WITH 3-STATE OUTPUTS

SCLS070A – NOVEMBER 1988 – REVISED NOVEMBER 1990

#### absolute maximum ratings over operating free-air temperature†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND pins	$\pm 70$ mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package	260°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SN54HCT126			SN74HCT126			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2			2			V
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	0		0.8	0		0.8	V
$V_I$	Input voltage		0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage		0		$V_{CC}$	0		$V_{CC}$	V
$t_t$	Input transition (rise and fall) time		0		500	0		500	ns
$T_A$	Operating free-air temperature		–55		125	–40		85	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT126		SN74HCT126		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -20$ $\mu\text{A}$	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OH} = -6$ mA		3.98	4.3		3.7		3.84		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 20$ $\mu\text{A}$	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or $V_{IL}$ , $I_{OL} = 6$ mA			0.17	0.26		0.4		0.33	
$I_I$	$V_I = V_{CC}$ or 0	5.5 V	$\pm 0.1$	$\pm 100$		$\pm 1000$		$\pm 1000$		nA
$I_{OZ}$	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or $V_{IL}$	5.5 V	$\pm 0.01$	$\pm 0.5$		$\pm 10$		$\pm 5$		$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V			8	160		80		$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	One input at 0.5 V or 2.4 V, Other inputs at 0 or $V_{CC}$	5.5 V		1.4	2.4		3		2.9	mA
$C_i$		4.5 V to 5.5 V		3	10		10*		10	pF

\* On products compliant to MIL-STD-883C, Class B, this parameter is not production tested.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

**SN54HCT126, SN74HCT126**  
**QUADRUPLE BUS BUFFER GATES**  
**WITH 3-STATE OUTPUTS**

SCLS070A – NOVEMBER 1988 – REVISED NOVEMBER 1990

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT126		SN74HCT126		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	4.5 V		15	26		39		33	ns
			5.5 V		12	23		35		30	
$t_{en}$	OE	Y	4.5 V		19	26		39		33	ns
			5.5 V		15	23		35		30	
$t_{dis}$	OE	Y	4.5 V		18	26		39		33	ns
			5.5 V		15	23		35		30	
$t_t$		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

**switching characteristics over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT126		SN74HCT126		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	4.5 V		21	36		58		46	ns
			5.5 V		17	32		48		42	
$t_{en}$	OE	Y	4.5 V		25	36		58		46	ns
			5.5 V		21	32		48		42	
$t_t$		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	35	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

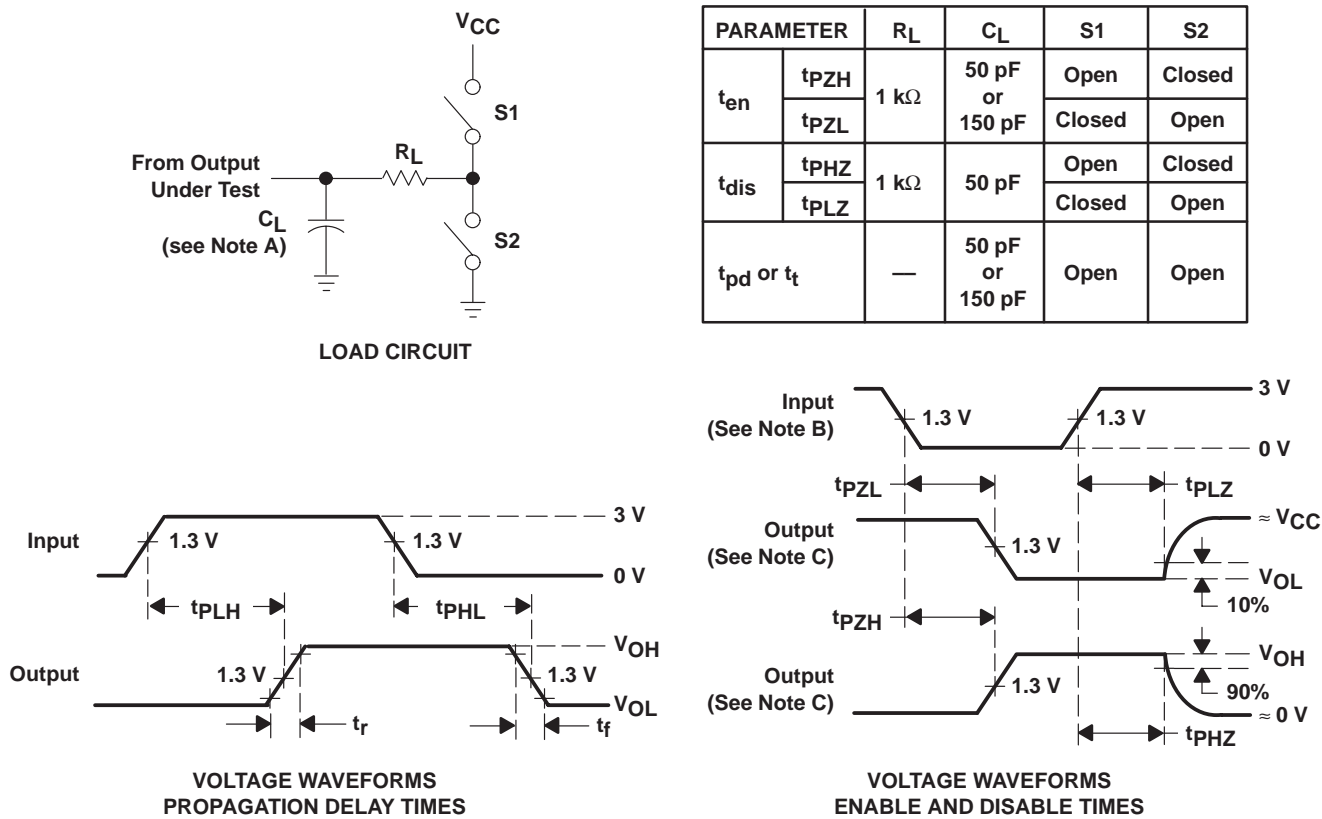


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54HCT126, SN74HCT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCLS070A – NOVEMBER 1988 – REVISED NOVEMBER 1990

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$ .
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.