

# SN74ALVC162834

## 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCES172A – DECEMBER 1998 – REVISED FEBRUARY 1999

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

### description

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

Data flow from A to Y is controlled by the output-enable ( $\overline{OE}$ ) input. The device operates in the transparent mode when the latch-enable ( $\overline{LE}$ ) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If  $\overline{LE}$  is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

The SN74ALVC162834 is characterized for operation from -40°C to 85°C.

### DGG, DGV, OR DL PACKAGE (TOP VIEW)

NC	1	56	GND
NC	2	55	NC
Y1	3	54	A1
GND	4	53	GND
Y2	5	52	A2
Y3	6	51	A3
$V_{CC}$	7	50	$V_{CC}$
Y4	8	49	A4
Y5	9	48	A5
Y6	10	47	A6
GND	11	46	GND
Y7	12	45	A7
Y8	13	44	A8
Y9	14	43	A9
Y10	15	42	A10
Y11	16	41	A11
Y12	17	40	A12
GND	18	39	GND
Y13	19	38	A13
Y14	20	37	A14
Y15	21	36	A15
$V_{CC}$	22	35	$V_{CC}$
Y16	23	34	A16
Y17	24	33	A17
GND	25	32	GND
Y18	26	31	A18
$\overline{OE}$	27	30	CLK
$\overline{LE}$	28	29	GND

NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

SN74ALVC162834
18-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

SCES172A – DECEMBER 1998 – REVISED FEBRUARY 1999

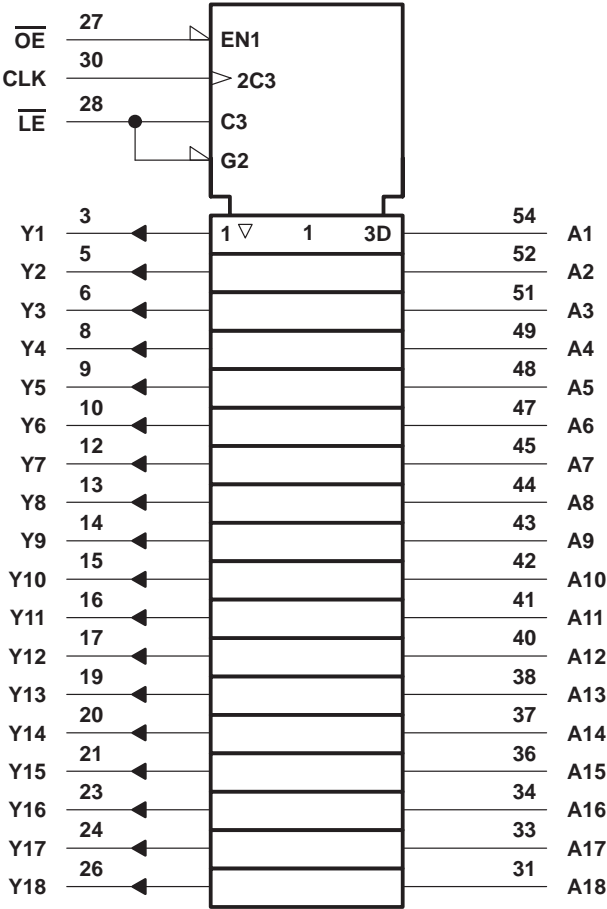
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	$\uparrow$	L	L
L	H	$\uparrow$	H	H
L	H	H	X	$Y_0^\dagger$
L	H	L	X	$Y_0^\ddagger$

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before  $\overline{LE}$  goes high

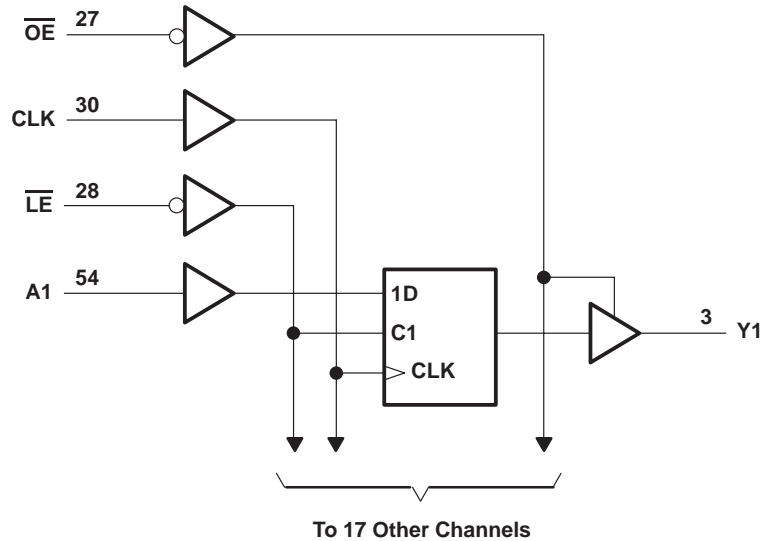
‡ Output level before the indicated steady-state input conditions were established

logic symbols



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	
DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 4.6 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51.

**SN74ALVC162834**  
**18-BIT UNIVERSAL BUS DRIVER**  
**WITH 3-STATE OUTPUTS**

SCES172A – DECEMBER 1998 – REVISED FEBRUARY 1999

**recommended operating conditions (see Note 4)**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		1.65	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		0.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	
$V_I$	Input voltage		0	$V_{CC}$	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65\text{ V}$		–2	mA
		$V_{CC} = 2.3\text{ V}$		–6	
		$V_{CC} = 2.7\text{ V}$		–8	
		$V_{CC} = 3\text{ V}$		–12	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$		2	mA
		$V_{CC} = 2.3\text{ V}$		6	
		$V_{CC} = 2.7\text{ V}$		8	
		$V_{CC} = 3\text{ V}$		12	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
$T_A$	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74ALVC162834**  
**18-BIT UNIVERSAL BUS DRIVER**  
**WITH 3-STATE OUTPUTS**

SCES172A – DECEMBER 1998 – REVISED FEBRUARY 1999

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = –100 µA	1.65 V to 3.6 V	V <sub>CC</sub> –0.2			V
		I <sub>OH</sub> = –2 mA	1.65 V	1.2			
		I <sub>OH</sub> = –4 mA	2.3 V	1.9			
		I <sub>OH</sub> = –6 mA	2.3 V	1.7			
			3 V	2.4			
		I <sub>OH</sub> = –8 mA	2.7 V	2			
		I <sub>OH</sub> = –12 mA	3 V	2			
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V	0.2			V
		I <sub>OL</sub> = 2 mA	1.65 V	0.45			
		I <sub>OL</sub> = 4 mA	2.3 V	0.4			
		I <sub>OL</sub> = 6 mA	2.3 V	0.55			
			3 V	0.55			
		I <sub>OL</sub> = 8 mA	2.7 V	0.6			
		I <sub>OL</sub> = 12 mA	3 V	0.8			
I <sub>I</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5			µA
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10			µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	40			µA
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	750			µA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	4			pF
	Data inputs			5.5			
C <sub>o</sub>	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7			pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

				V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			‡		150		150		150		MHz
t <sub>w</sub>	Pulse duration	LE low		‡		3.3		3.3		3.3		ns
		CLK high or low		‡		3.3		3.3		3.3		
t <sub>su</sub>	Setup time	Data before CLK↑		‡		2.1		2.1		1.7		ns
		Data before LE↑	CLK high	‡		2.3		2.3		1.9		
			CLK low	‡		1.9		1.9		1.5		
t <sub>h</sub>	Hold time	Data after CLK↑		‡		0.6		0.6		0.7		ns
		Data after LE↑	CLK high or low	‡		0.8		0.8		0.9		

‡ This information was not available at the time of publication.



# SN74ALVC162834

## 18-BIT UNIVERSAL BUS DRIVER

### WITH 3-STATE OUTPUTS

SCES172A – DECEMBER 1998 – REVISED FEBRUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			†		150		150		150		MHz
t <sub>pd</sub>	A	Y		†	1	5.2	5		1	4.2	ns
	$\overline{\text{LE}}$			†	1.3	6	6.8		1.3	5.8	
	CLK			†	1.4	6.8	6.1		1.4	5.4	
t <sub>en</sub>	$\overline{\text{OE}}$	Y		†	1.4	6.3	6.5		1.5	5.9	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		†	1	4.4	5.2		1.8	5	ns

† This information was not available at the time of publication.

switching characteristics from 0°C to 65°C, C<sub>L</sub> = 50 pF

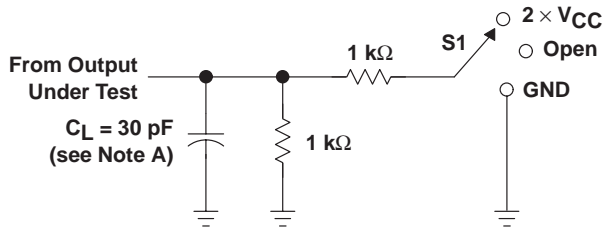
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t <sub>pd</sub>	A	Y	1.4	3.9	ns
	$\overline{\text{LE}}$		1.8	5.5	
	CLK		1.8	5.2	

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	C <sub>L</sub> = 0, f = 10 MHz	†	38	41	pF
	Outputs disabled		†	13	15	

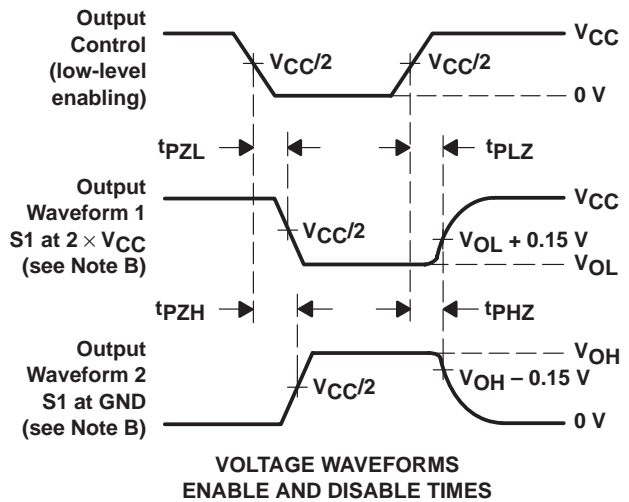
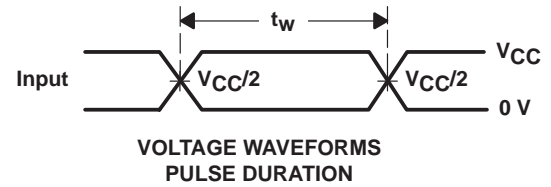
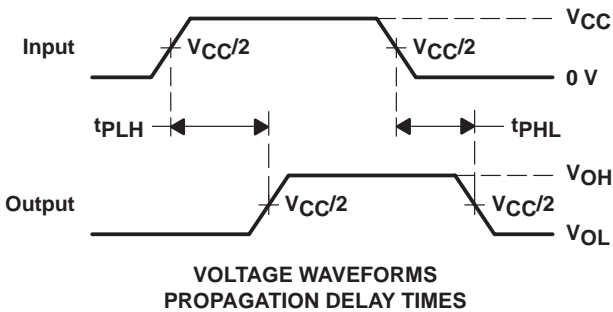
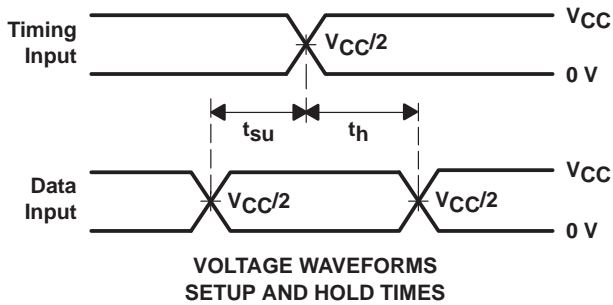
† This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION  
 $V_{CC} = 1.8 \text{ V}$



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

# SN74ALVC162834

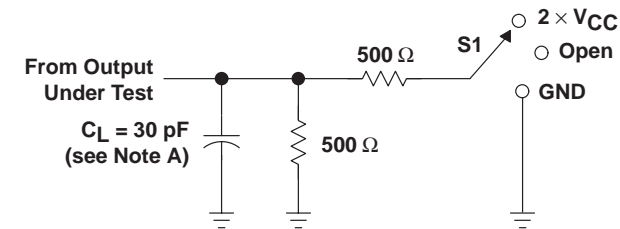
## 18-BIT UNIVERSAL BUS DRIVER

### WITH 3-STATE OUTPUTS

SCES172A – DECEMBER 1998 – REVISED FEBRUARY 1999

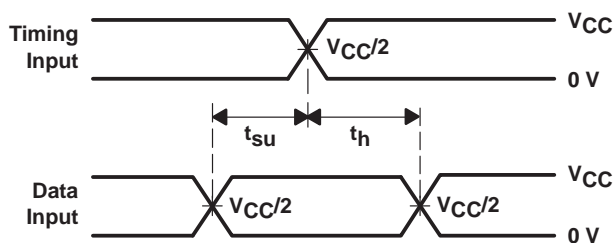
#### PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

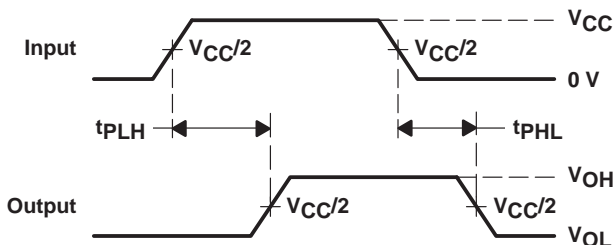


LOAD CIRCUIT

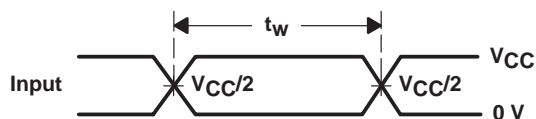
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PHZ}$	GND



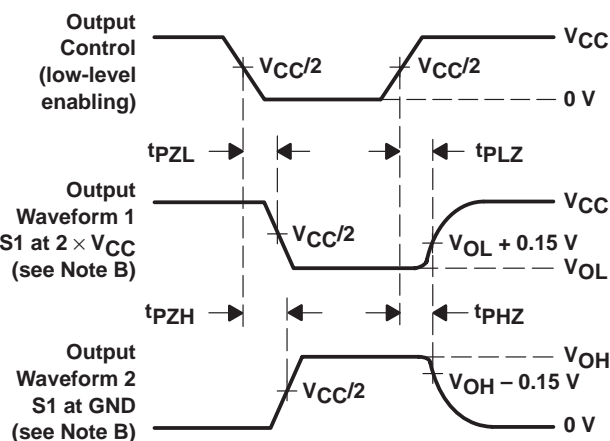
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



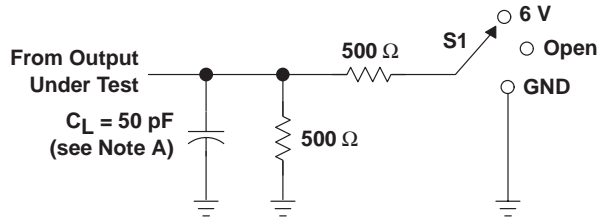
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

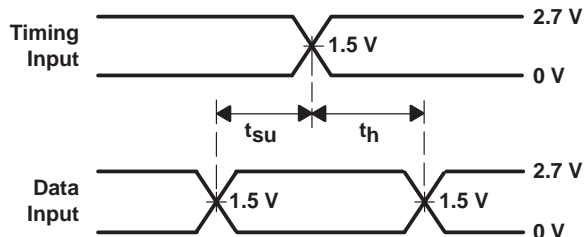
# PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

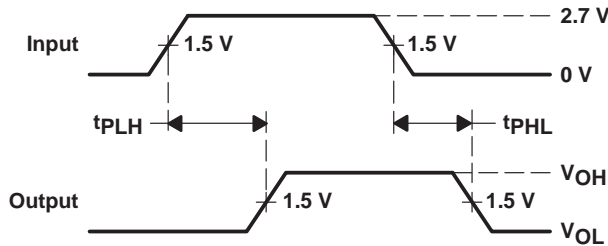


LOAD CIRCUIT

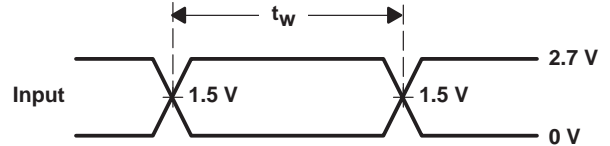
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



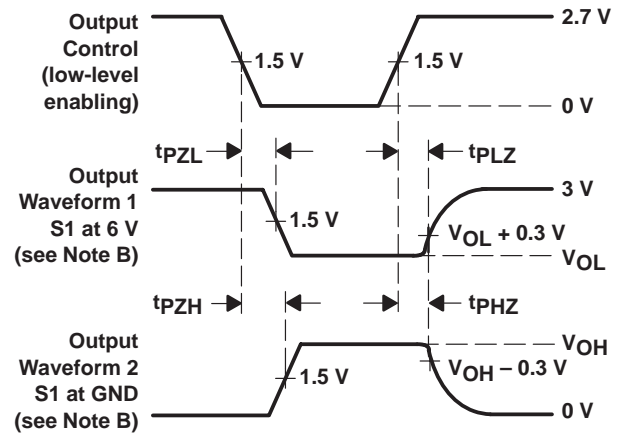
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.