

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **DOC™** (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages

description

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

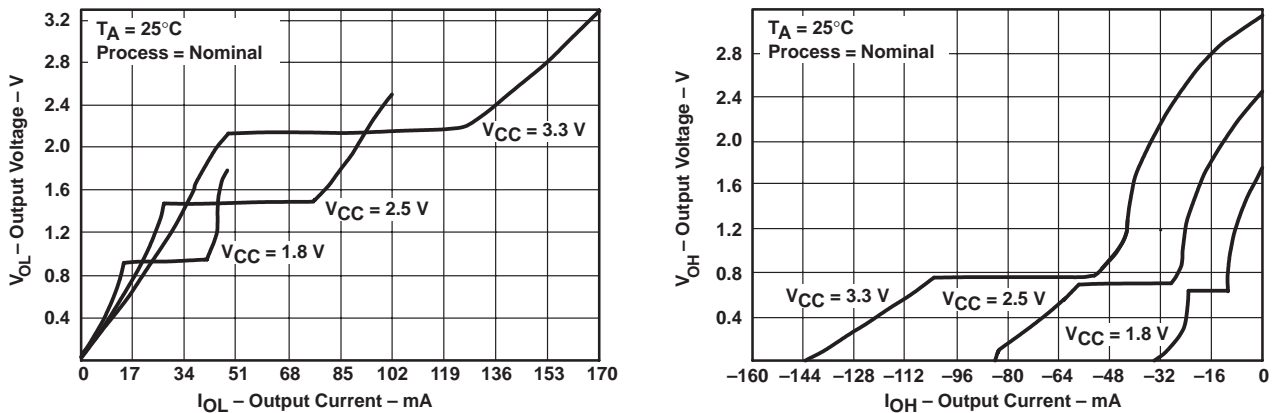


Figure 1. Output Voltage vs Output Current

This quadruple 2-input positive-NAND gate is operational at 1.2-V to 3.6-V V_{CC} , but is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The SN74AVC00 performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC00 is characterized for operation from -40°C to 85°C .



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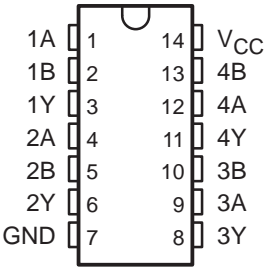
SN74AVC00

QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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terminal assignments

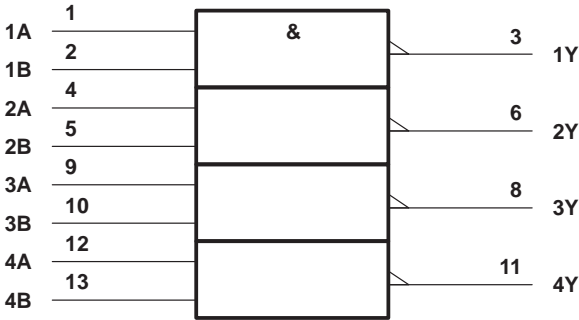
D, DGV, OR PW PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	± 50 mA
Continuous current through each V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3):		
D package	86°C/W
DGV package	127°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.4	3.6	V
	Data retention only	1.2		
V_{IH} High-level input voltage	$V_{CC} = 1.2\text{ V}$	V_{CC}		V
	$V_{CC} = 1.4\text{ V to }1.6\text{ V}$	$0.65 \times V_{CC}$		
	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
	$V_{CC} = 3\text{ V to }3.6\text{ V}$	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.2\text{ V}$	GND		V
	$V_{CC} = 1.4\text{ V to }1.6\text{ V}$	$0.35 \times V_{CC}$		
	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$		
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7		
	$V_{CC} = 3\text{ V to }3.6\text{ V}$	0.8		
V_I Input voltage		0	3.6	V
V_O Output voltage	Active state	0	V_{CC}	V
	3-state	0	3.6	
I_{OHS} Static high-level output current†	$V_{CC} = 1.4\text{ V to }1.6\text{ V}$		–2	mA
	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		–4	
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		–8	
	$V_{CC} = 3\text{ V to }3.6\text{ V}$		–12	
I_{OLS} Static low-level output current†	$V_{CC} = 1.4\text{ V to }1.6\text{ V}$		2	mA
	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		4	
	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		8	
	$V_{CC} = 3\text{ V to }3.6\text{ V}$		12	
$\Delta t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 1.4\text{ V to }3.6\text{ V}$		5	ns/V
T_A Operating free-air temperature		–40	85	°C

† Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of $\pm 24\text{ mA}$ at $2.5\text{-V }V_{CC}$. See Figure 1 for V_{OL} vs I_{OL} and V_{OH} vs I_{OH} characteristics. Refer to the TI application reports, **AVC Logic Family Technology and Applications**, literature number **SCEA006**, and **Dynamic Output Control (DOC™) Circuitry Technology and Applications**, literature number **SCEA009**.

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW



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SN74AVC00

QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OHS} = -100 µA	1.4 V to 3.6 V	V _{CC} -0.2			V
	I _{OHS} = -2 mA, V _{IH} = 0.91 V	1.4 V	1.05			
	I _{OHS} = -4 mA, V _{IH} = 1.07 V	1.65 V	1.2			
	I _{OHS} = -8 mA, V _{IH} = 1.7 V	2.3 V	1.75			
	I _{OHS} = -12 mA, V _{IH} = 2 V	3 V	2.3			
V _{OL}	I _{OLS} = 100 µA	1.4 V to 3.6 V	0.2			V
	I _{OLS} = 2 mA, V _{IL} = 0.49 V	1.4 V	0.4			
	I _{OLS} = 4 mA, V _{IL} = 0.57 V	1.65 V	0.45			
	I _{OLS} = 8 mA, V _{IL} = 0.7 V	2.3 V	0.55			
	I _{OLS} = 12 mA, V _{IL} = 0.8 V	3 V	0.7			
I _I	V _I = V _{CC} or GND	3.6 V	±2.5			µA
I _{off}	V _I or V _O = 3.6 V	0	±10			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	40			µA
C _i	V _I = V _{CC} or GND	2.5 V				pF
		3.3 V				

† Typical values are measured at T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.2 V	V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y										ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per gate	C _L = 0, f = 10 MHz				pF

PRODUCT PREVIEW

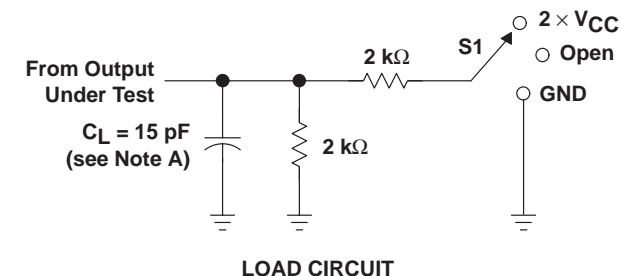


SN74AVC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

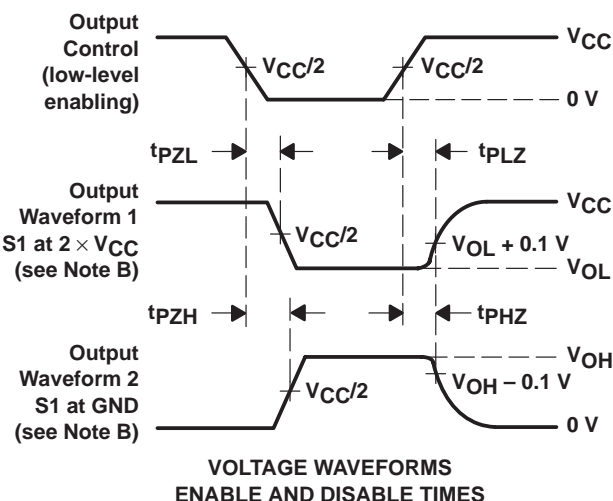
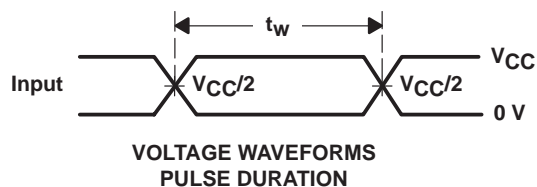
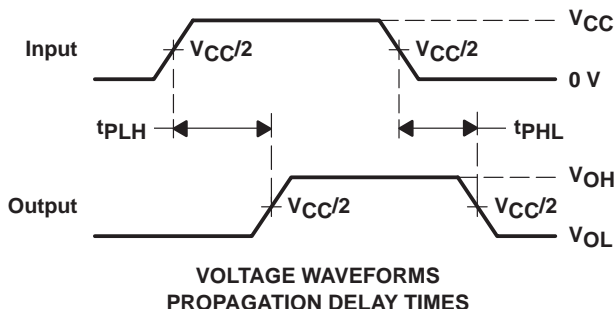
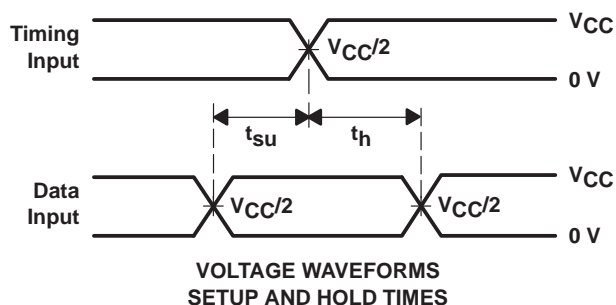
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PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2\text{ V AND } 1.5\text{ V} \pm 0.1\text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PHZ}	GND

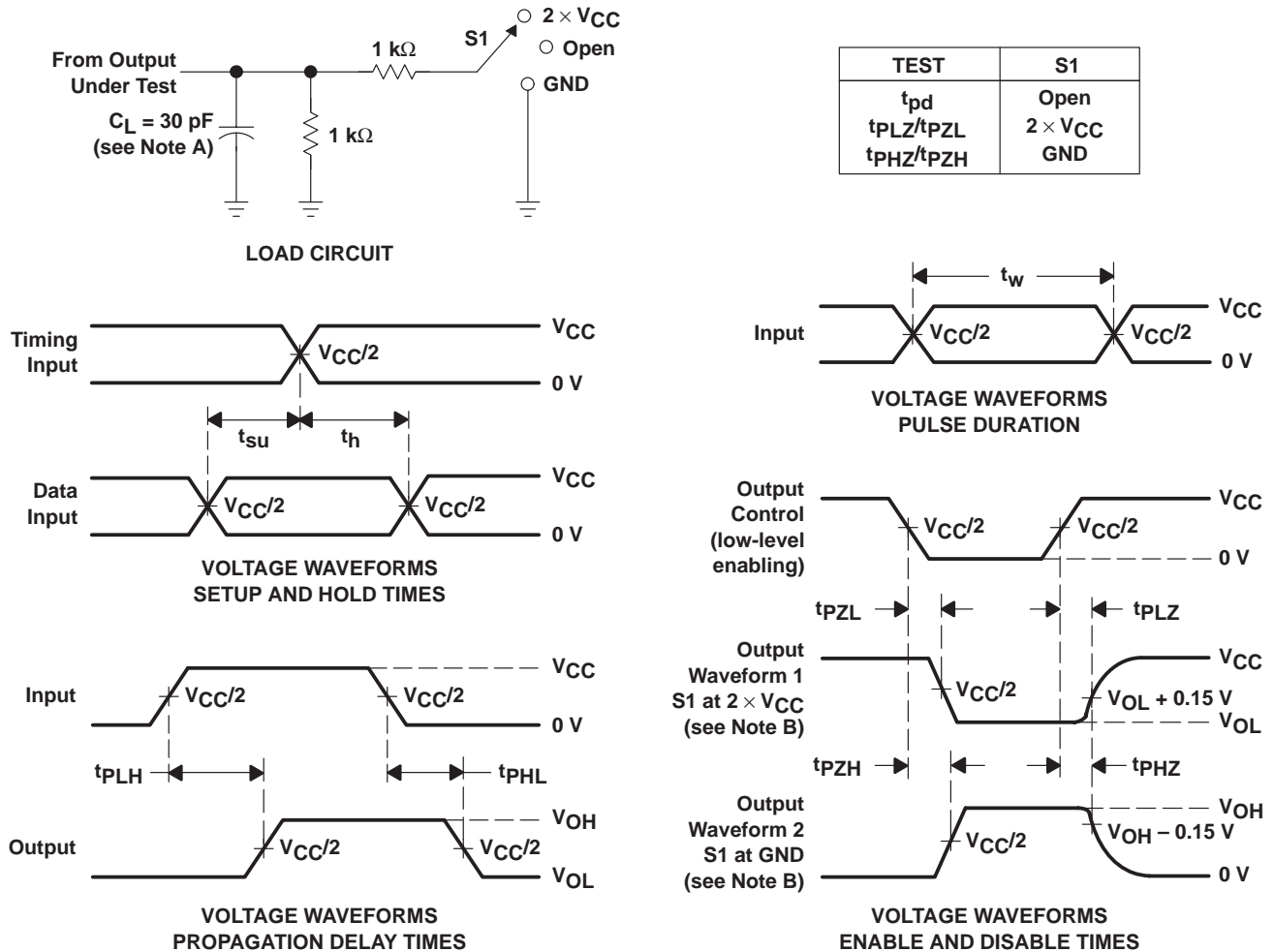


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



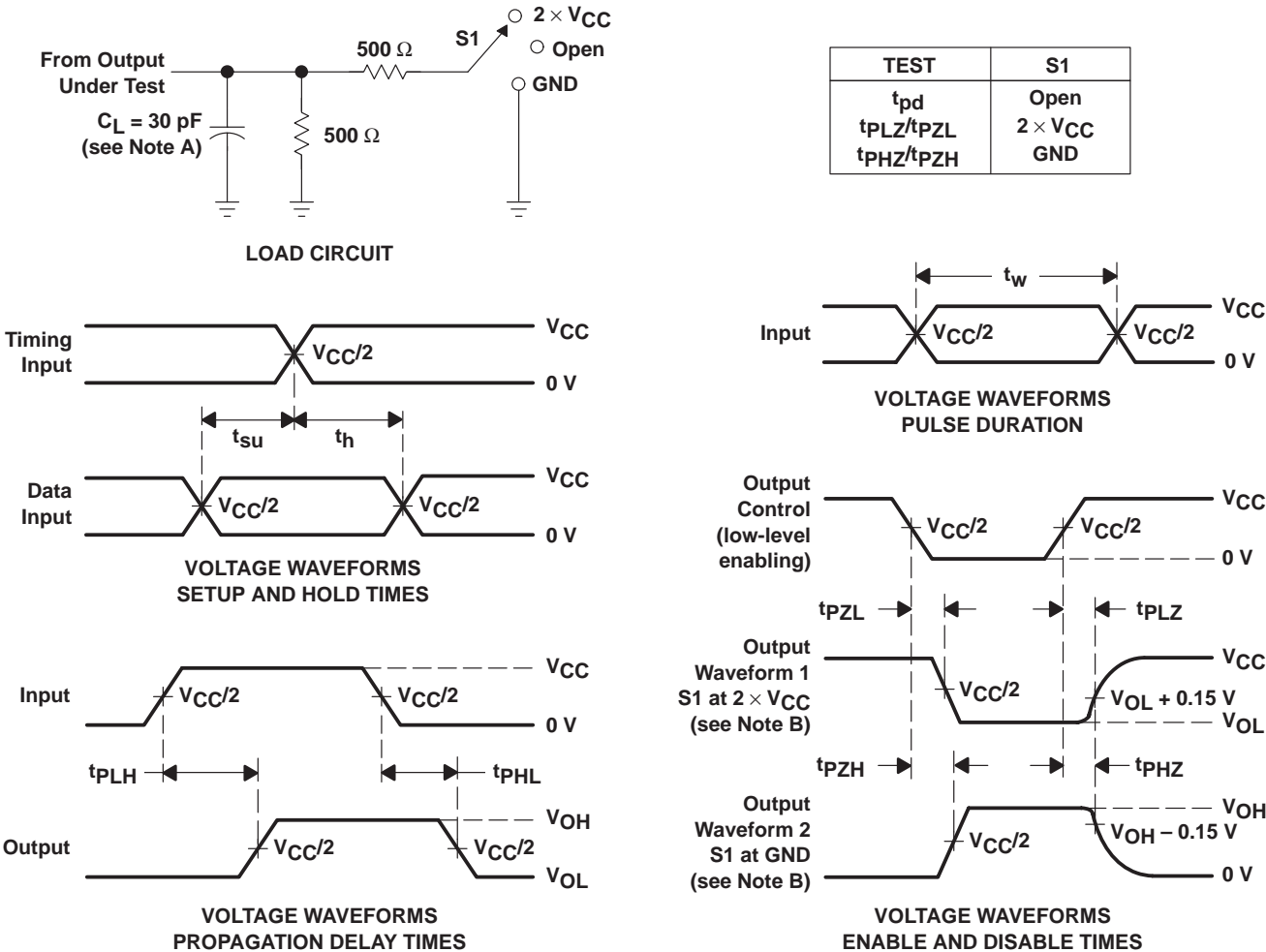
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 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

SN74AVC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

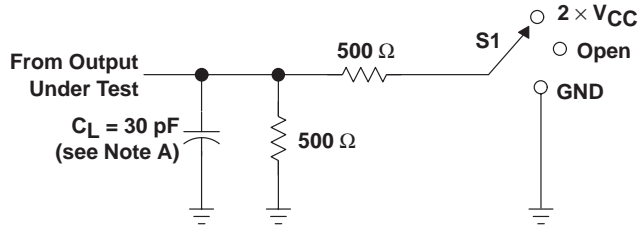


- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

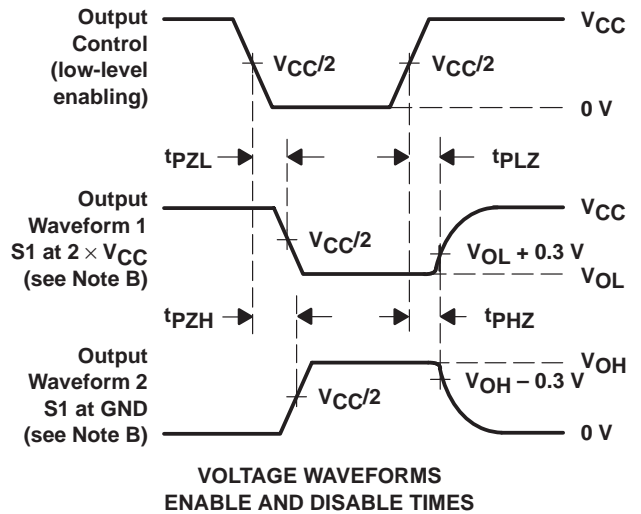
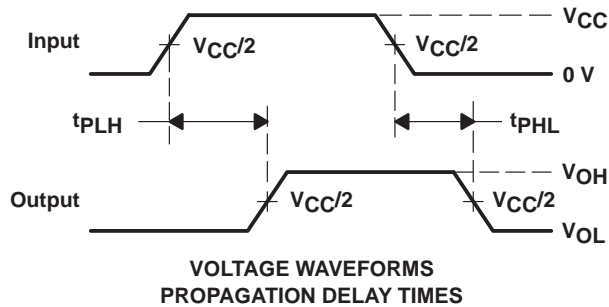
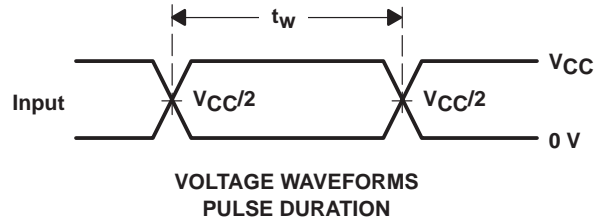
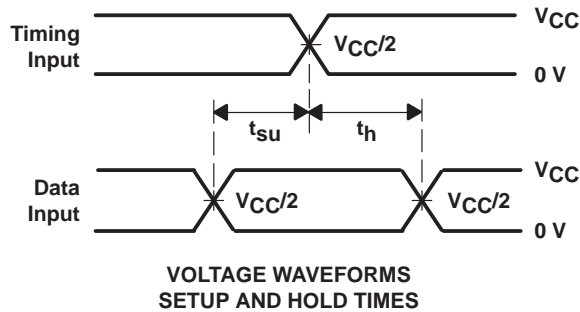
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 \times V_{CC}
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms

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