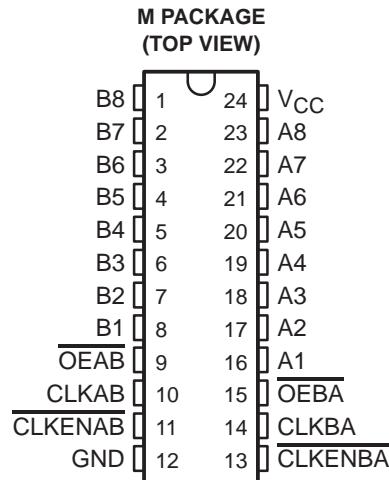


CD74FCT2952A

BiCMOS OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCBS720 – JULY 2000

- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Noninverted Outputs
- Input/Output Isolation From V_{CC}
- Controlled Output Edge Rates
- 64-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V at $V_{CC} = 5\text{ V}$
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- Packaged in Plastic Small-Outline Package



description

The CD74FCT2952A is an octal transceiver and register, consisting of two 8-bit, back-to-back registers that store data flowing in both directions between two bidirectional buses. It uses a small-geometry BiCMOS technology. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock ($\overline{\text{CLKAB}}$ or $\overline{\text{CLKBA}}$) input if the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

This device contains two 8-bit, back-to-back registers that store data flowing in both directions between two bidirectional buses. Each register has separate clock, clock enable, and 3-state output enable signals associated with it.

The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below V_{CC} . This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CD74FCT2952A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{CLKAB}}$	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0^\ddagger
X	H or L	L	X	B_0^\ddagger
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar, but uses $\overline{\text{CLKENBA}}$, $\overline{\text{CLKBA}}$, and $\overline{\text{OEBA}}$.

‡ Level of B before the indicated steady-state input conditions were established



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

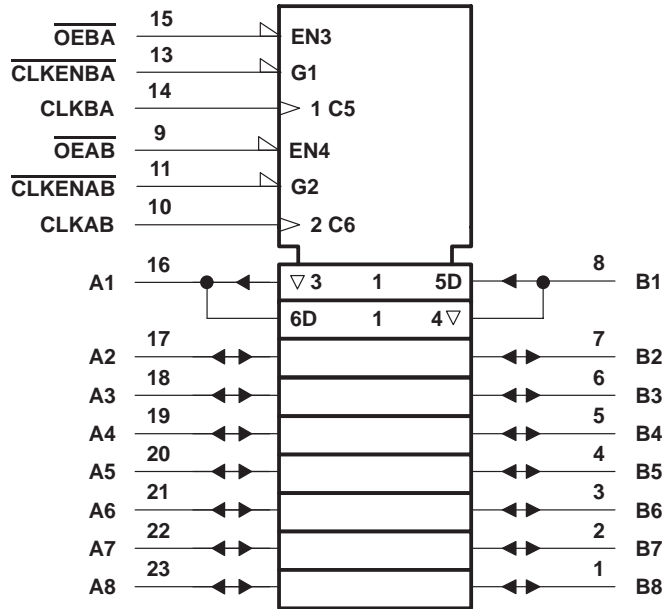
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.75	5.25	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		-15	mA
I _{OL}	Low-level output current		48	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _A	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V _{IK}	I _I = -18 mA	4.75 V		-1.2		-1.2	V
V _{OH}	I _{OH} = -15 mA	4.75 V	2.4		2.4		V
V _{OL}	I _{OL} = 64 mA	4.75 V		0.55		0.55	V
I _I	V _I = V _{CC} or GND	5.25 V		±0.1		±1	μA
I _{OZ}	V _O = V _{CC} or GND	5.25 V		±0.5		±10	μA
I _{OS} [†]	V _I = V _{CC} or GND, V _O = 0	5.25 V		-60		-60	mA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.25 V		8		80	μA
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.25 V		1.6		1.6	mA
C _i	V _I = V _{CC} or GND			10		10	pF
C _o	V _O = V _{CC} or GND			15		15	pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

[‡] This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
t _w	Pulse duration	CLK high or low	3		ns
t _{su}	Setup time	A or B	2		ns
		CLKEN	3		
t _h	Hold time	A or B	2		ns
		CLKEN	2		



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

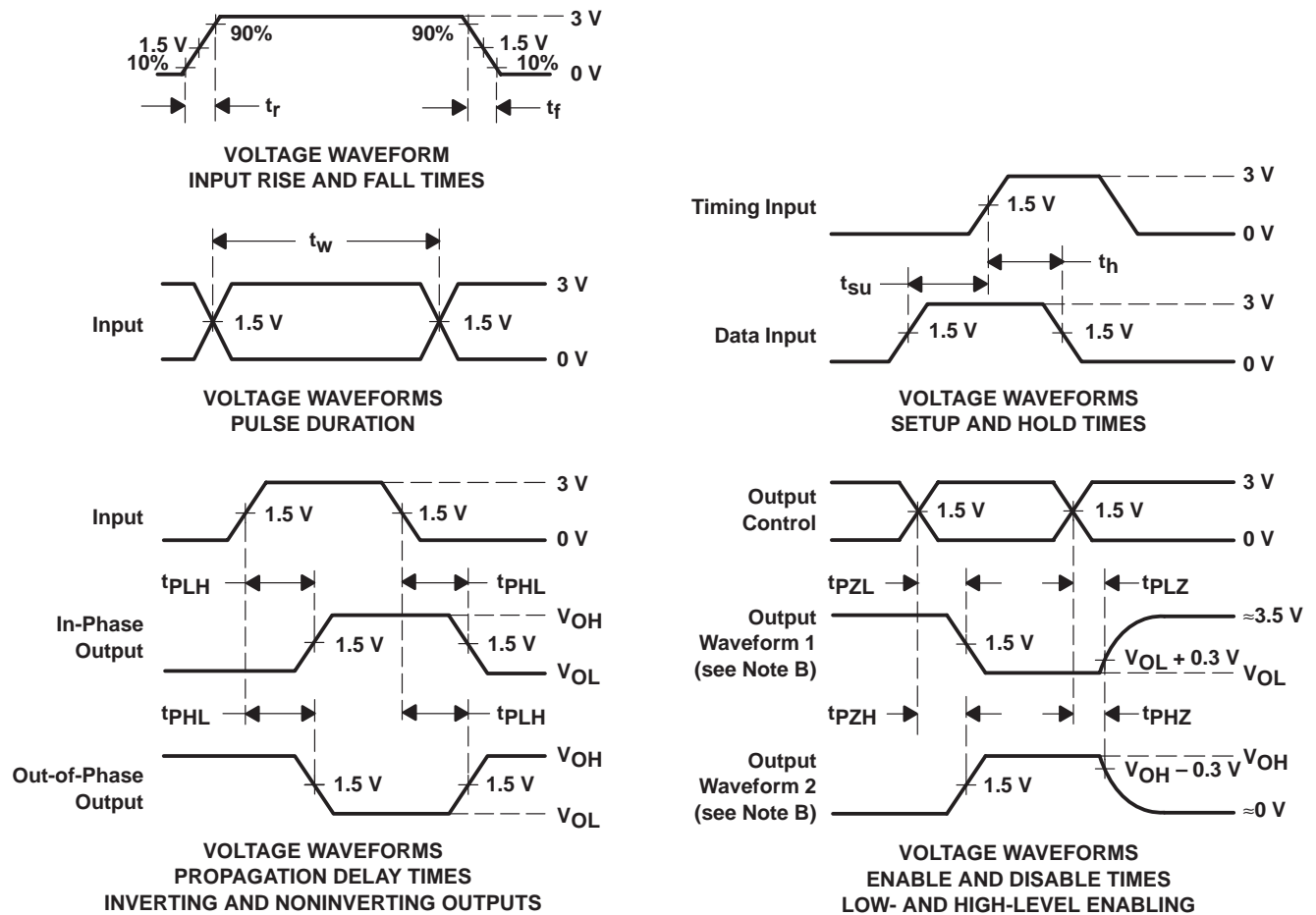
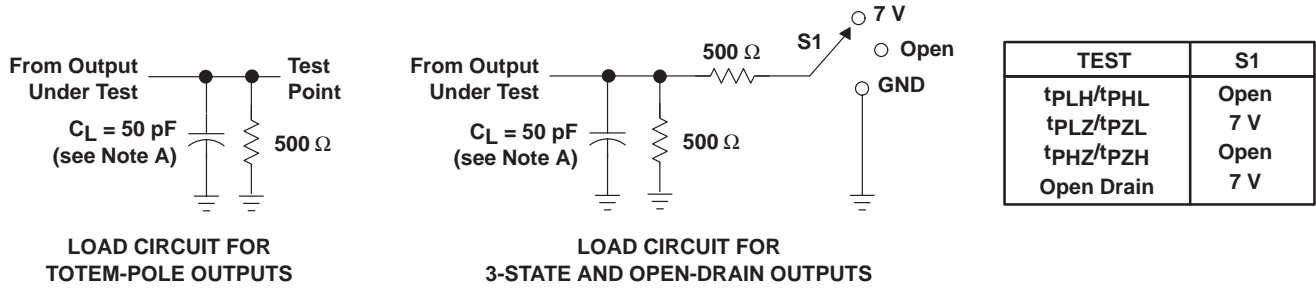
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$	MIN	MAX	UNIT
			TYP			
t_{pd}	CLKBA or CLKAB	A or B	5.5	2	10	ns
t_{en}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	5.5	1.5	10.5	ns
t_{dis}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	5.5	1.5	10	ns



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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, t_r and $t_f = 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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