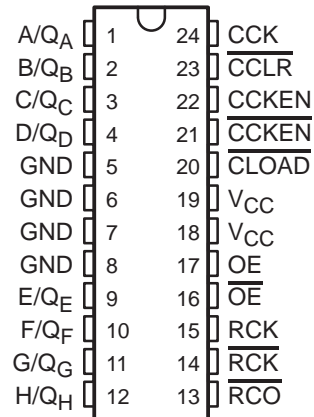


74ACT11593  
8-BIT BINARY COUNTER  
WITH PARALLEL-INPUT REGISTERS AND 3-STATE OUTPUTS  
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- Inputs Are TTL-Voltage Compatible
- Parallel Register Inputs/Binary Counter/3-State Outputs
- Counter Has Direct Overriding Load and Clear
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE  
(TOP VIEW)



## description

The 74ACT11593 contains eight multiplexed parallel I/Os with 3-state output capability and an 8-bit storage register that feeds an 8-bit binary counter. Both the register and the counter have individual positive-edge triggered clocks.

The function tables show the operation of the counter clock-enable (CCKEN,  $\overline{CCKEN}$ ) and output-enable (OE,  $\overline{OE}$ ) inputs.

The counter input has direct load and clear functions. A low-going  $\overline{RCO}$  pulse is obtained when the counter reaches the hex word FF.

Expansion is easily accomplished for two stages by connecting  $\overline{RCO}$  of the first stage to  $\overline{CCKEN}$  of the second stage. Cascading for larger count chains is accomplished by connecting  $\overline{RCO}$  of each stage to CCK of the following stage.

The 74ACT11593 is characterized for operation from –40°C to 85°C.

## Function Tables

COUNTER CLOCK ENABLE

INPUTS		OUTPUTS A/Q <sub>A</sub> THRU H/Q <sub>H</sub>
CCKEN	$\overline{CCKEN}$	
L	L	Disable
L	H	Disable
H	L	Enable
H	H	Disable

OUTPUT ENABLE

INPUTS		OUTPUTS A/Q <sub>A</sub> THRU H/Q <sub>H</sub>
OE	$\overline{OE}$	
L	L	Input mode
L	H	Input mode
H	L	Output mode
H	H	Input mode

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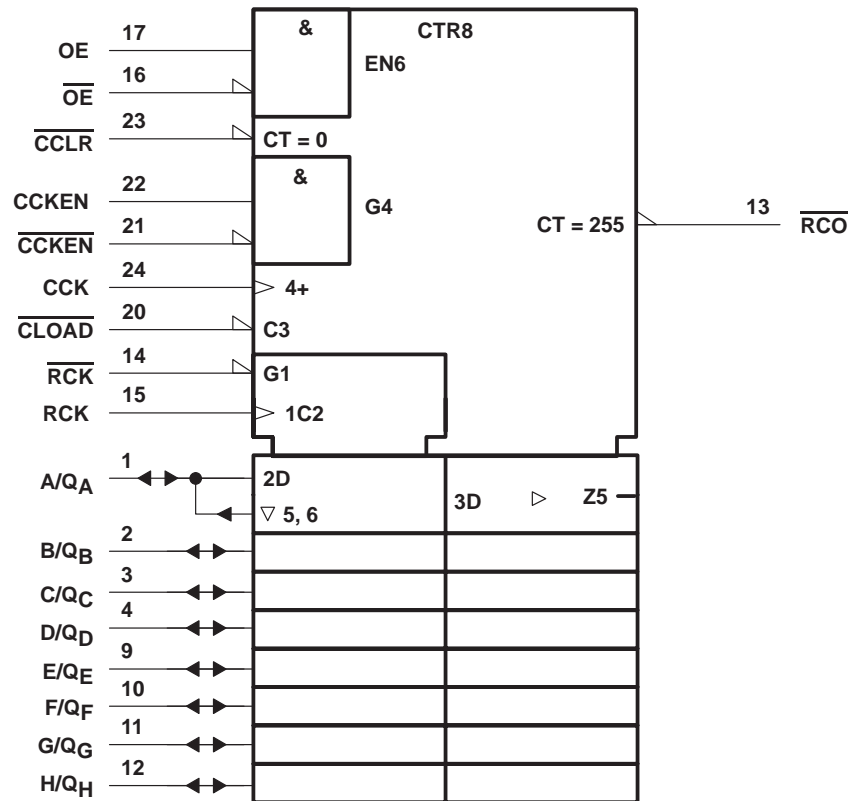


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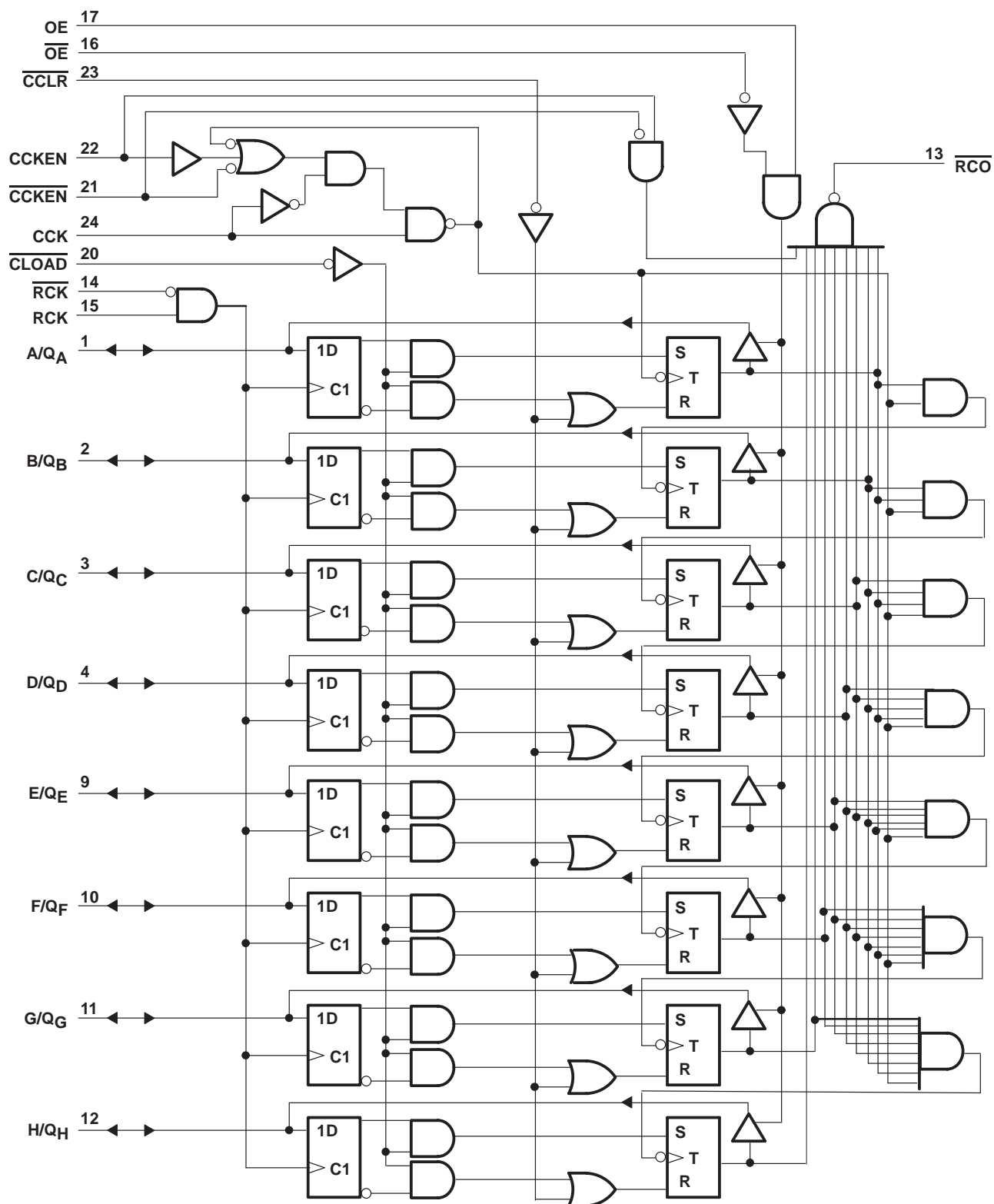
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

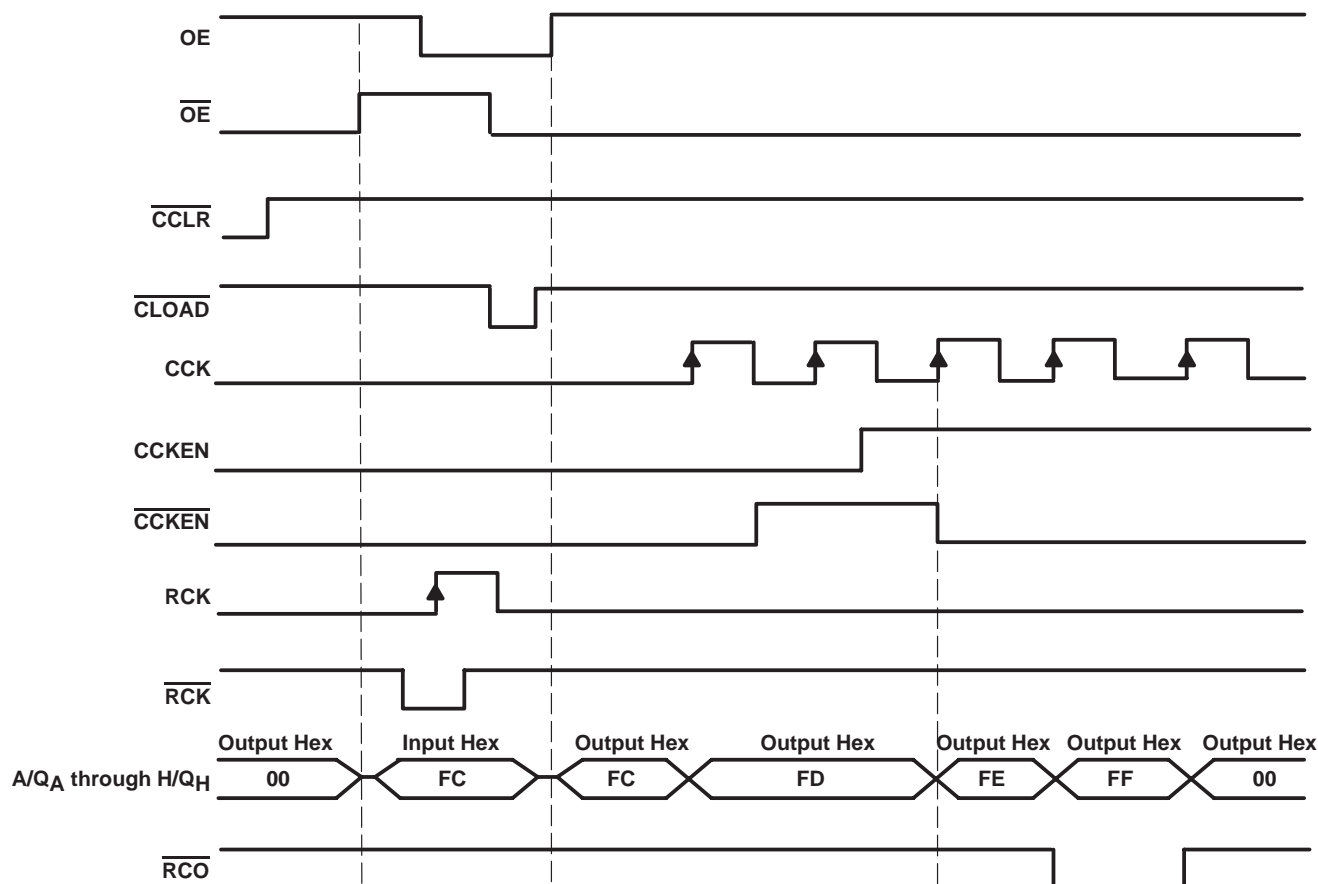
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logic diagram (positive logic)



**74ACT11593**  
**8-BIT BINARY COUNTER**  
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**typical operating sequence**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 225$ mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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**recommended operating conditions (see Note 2)**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_I$	Input voltage	0	$V_{CC}$		V
$V_O$	Output voltage	0	$V_{CC}$		V
$I_{OH}$	High-level output current			-24	mA
$I_{OL}$	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
$T_A$	Operating free-air temperature	-40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	4.5 V	4.4			4.4		V
		5.5 V	5.4			5.4		
	$I_{OH} = -24\ \text{mA}$	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	$I_{OH} = -75\ \text{mA}^\dagger$	5.5 V				3.85		
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	4.5 V			0.1		0.1	V
		5.5 V			0.1		0.1	
	$I_{OL} = 24\ \text{mA}$	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	$I_{OL} = 75\ \text{mA}^\dagger$	5.5 V					1.65	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5 V			$\pm 0.5$		$\pm 5$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	$\mu\text{A}$
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			0.9		1	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		3.5				pF
$C_{io}$	$V_O = V_{CC}$ or GND	5 V		12.5				pF

$^\dagger$  Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

$^\ddagger$  This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

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timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f <sub>clock</sub>	Clock frequency, CCK or RCK		52		52		MHz
t <sub>w</sub>	Pulse duration	CCK high or low	9.6		9.6		ns
		RCK high or low	5.8		5.8		
		$\overline{\text{CCLR}}$ low	7.6		7.6		
		$\overline{\text{CLOAD}}$ low	6.2		6.2		
t <sub>su</sub>	Setup time	$\overline{\text{CCKEN}}$ low before CCK↑	3.6		3.6		ns
		CCKEN high before CCK↑	4		4		
		$\overline{\text{CCLR}}$ high before CCK↑	1.2		1.2		
		$\overline{\text{CLOAD}}$ high before CCK↑	5.1		5.1		
		RCK↑ before $\overline{\text{CLOAD}}$ ↑↑	7.4		7.4		
		Data A thru H before RCK↑	2.4		2.4		
t <sub>h</sub>	Hold time	Data A thru H after RCK↑	1.2		1.2		ns
		All others	0.8		0.8		

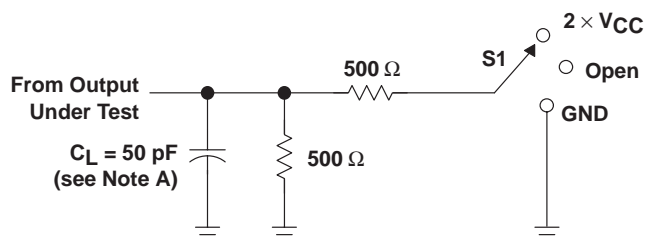
switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f <sub>max</sub>			52			52		MHz
t <sub>PLH</sub>	CCK	Q	5.6	10.2	13.3	5.6	15.1	ns
t <sub>PHL</sub>			5.8	10.3	13.3	5.8	15	
t <sub>PLH</sub>	$\overline{\text{CLOAD}}$	Q	5.5	12	16.9	5.5	19.1	ns
t <sub>PHL</sub>			5.8	13.5	19.4	5.8	21.7	
t <sub>PHL</sub>	$\overline{\text{CCLR}}$	Q	5	10.4	14.3	5	16	ns
t <sub>PZH</sub>	OE	Q	5.9	10.9	14.3	5.9	16.3	ns
t <sub>PZL</sub>			5.9	11.1	14.8	5.9	16.9	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q	4.9	10.4	14.4	4.9	16.5	ns
t <sub>PZL</sub>			5.1	10.7	15	5.1	17	
t <sub>PHZ</sub>	OE	Q	5.3	9	11.8	5.3	12.9	ns
t <sub>PLZ</sub>			6.2	10.2	13.1	6.2	14.4	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q	5.6	8.6	10.7	5.6	11.6	ns
t <sub>PLZ</sub>			6.4	9.9	12	6.4	13.3	
t <sub>PLH</sub>	CCK	$\overline{\text{RCO}}$	4.9	9.2	12.1	4.9	13.7	ns
t <sub>PHL</sub>			5.8	10.9	14.3	5.8	16.3	
t <sub>PLH</sub>	$\overline{\text{CLOAD}}$	$\overline{\text{RCO}}$	4.6	9.6	13.3	4.6	15	ns
t <sub>PHL</sub>			7.1	13.6	18.5	7.1	21	
t <sub>PLH</sub>	$\overline{\text{CCLR}}$	$\overline{\text{RCO}}$	5.1	10.3	14.5	5.1	16.2	ns
t <sub>PLH</sub>	RCK	$\overline{\text{RCO}}$	6.7	12	15.6	6.7	17.7	ns
t <sub>PHL</sub>			7.5	13.6	17.8	7.5	20.2	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

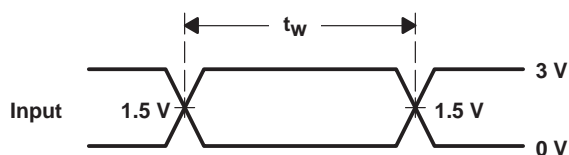
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	61	pF
	Outputs disabled		15	

### PARAMETER MEASUREMENT INFORMATION

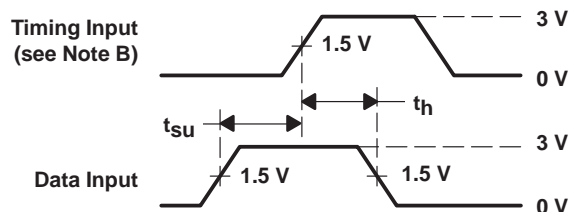


LOAD CIRCUIT

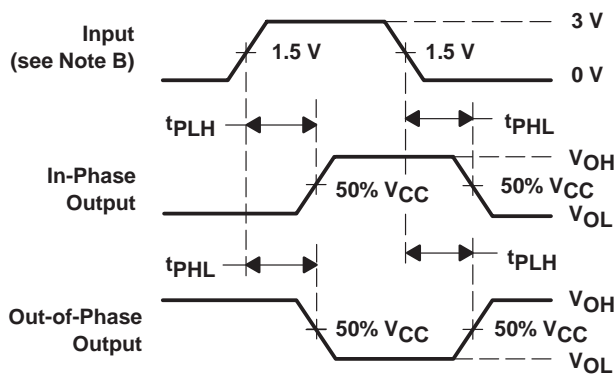
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



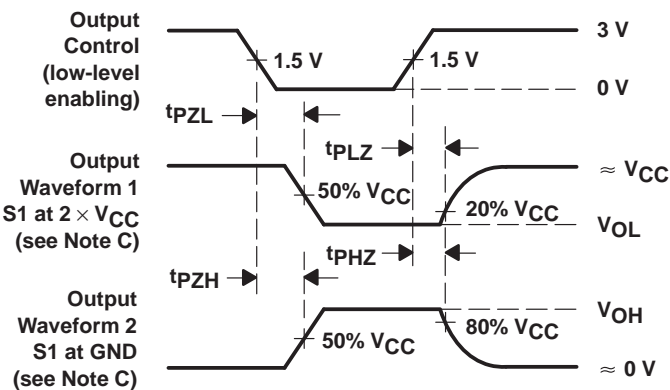
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ .

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





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