

54ACT16544, 74ACT16544 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS161A – AUGUST 1990 – REVISED APRIL 1996

- **Members of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Inverted Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

description

The 'ACT16544 are 16-bit registered transceivers that contain two sets of D-type latches for temporary storage of data flowing in either direction. They can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low to enter data from A or to output data to B. Having $\overline{\text{CEAB}}$ low and $\overline{\text{LEAB}}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition at $\overline{\text{LEAB}}$ puts the A latches in the storage mode. Data flow from B to A is similar, but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.

The 74ACT16544 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16544 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16544 is characterized for operation from –40°C to 85°C.

54ACT16544 ... WD PACKAGE
74ACT16544 ... DL PACKAGE
(TOP VIEW)

$\overline{1\text{OEAB}}$	1	56	$\overline{1\text{OEBA}}$
$\overline{1\text{LEAB}}$	2	55	$\overline{1\text{LEBA}}$
$\overline{1\text{CEAB}}$	3	54	$\overline{1\text{CEBA}}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V _{CC}	7	50	V _{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V _{CC}	22	35	V _{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{2\text{CEAB}}$	26	31	$\overline{2\text{CEBA}}$
$\overline{2\text{LEAB}}$	27	30	$\overline{2\text{LEBA}}$
$\overline{2\text{OEAB}}$	28	29	$\overline{2\text{OEBA}}$



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**TEXAS
INSTRUMENTS**

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54ACT16544, 74ACT16544

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FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A	
H	X	X	X	Z
L	X	H	X	Z
L	H	L	X	B_0^\ddagger
L	L	L	L	H
L	L	L	H	L

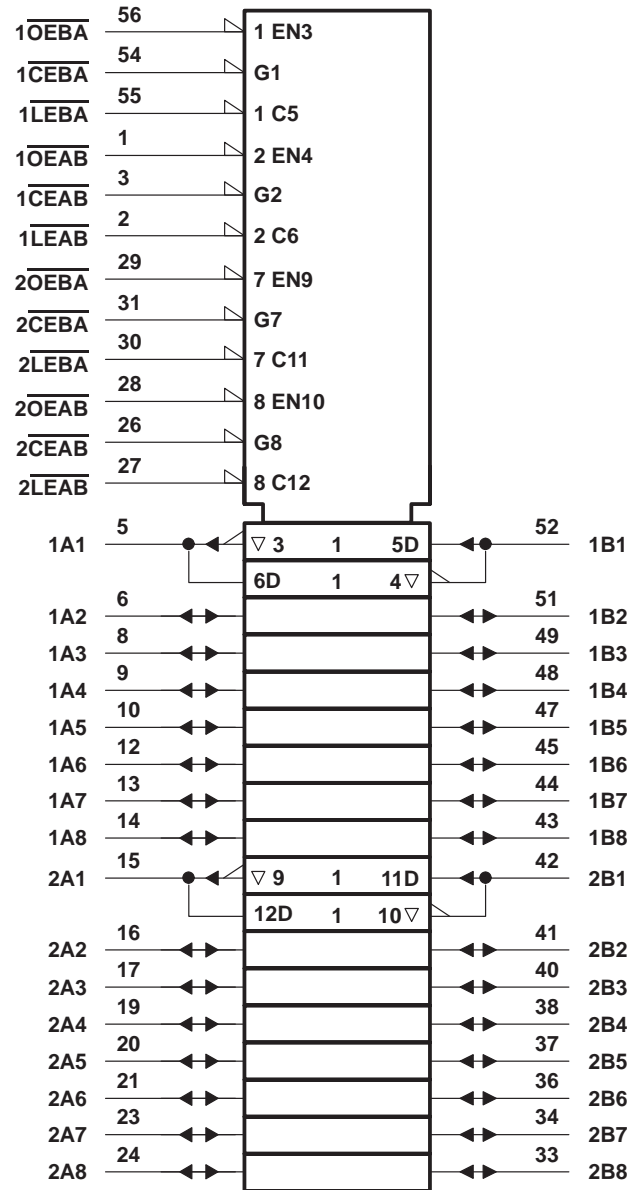
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

‡ Output level before the indicated steady-state input conditions were established

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

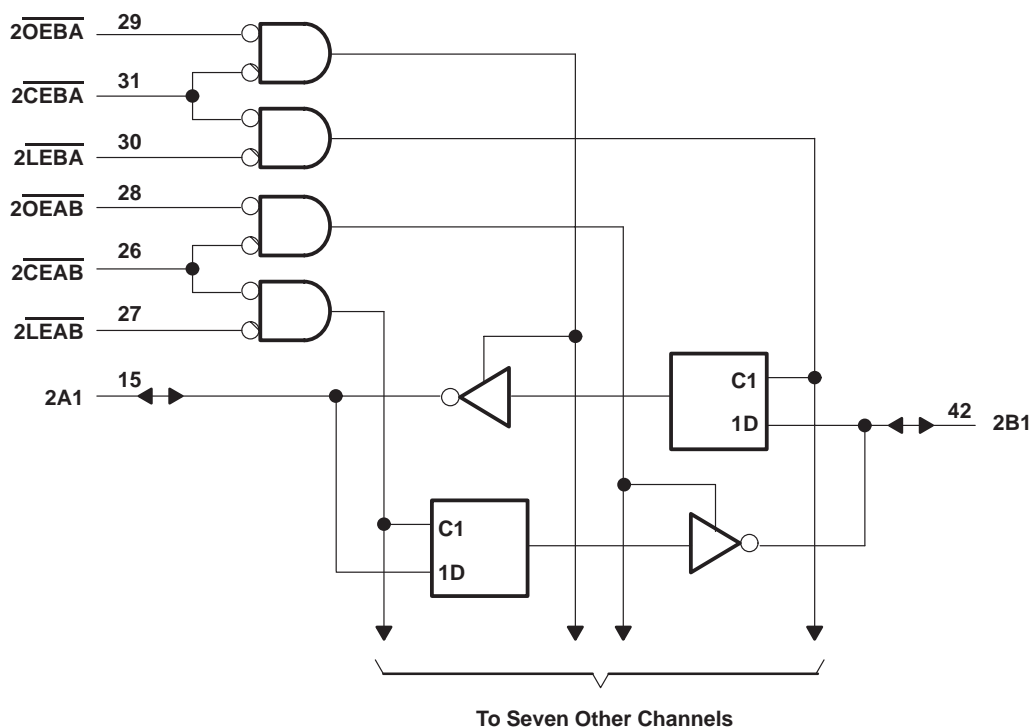
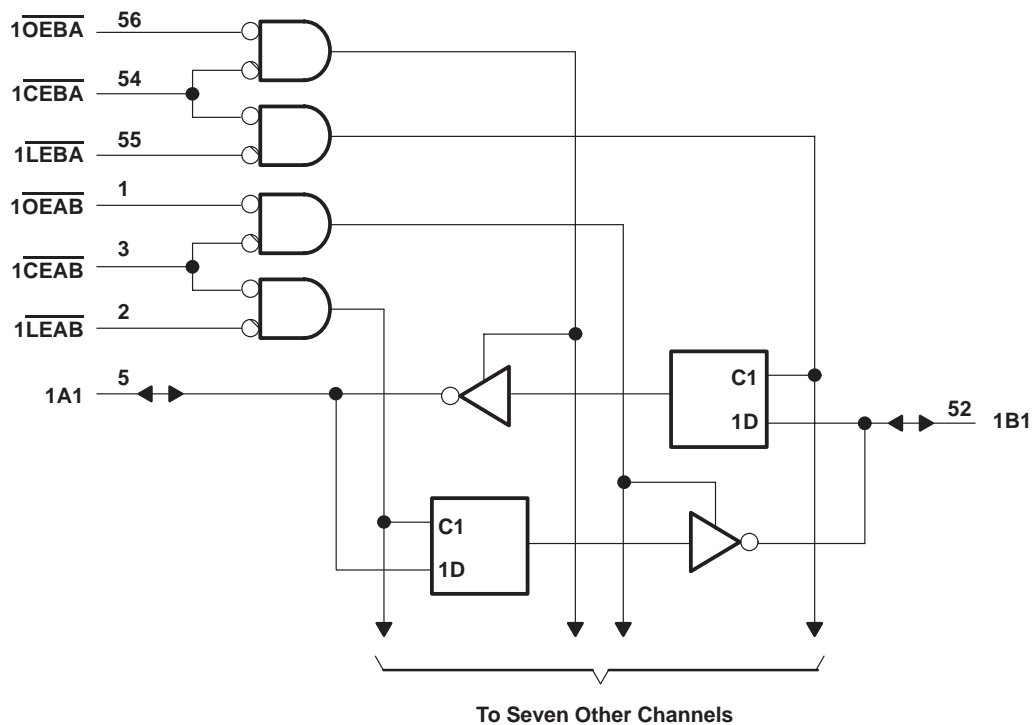
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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 to 7 V
Input voltage range, V_I (see Note 1)	–0.5 to $V_{CC} + 0.5$ V
Input voltage range, V_O (see Note 1)	–0.5 to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Maximum power package dissipation at $T_A = 55^\circ\text{C}$ (see Note 2): DL package	1.4 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

	54ACT16544			74ACT16544			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
V_I Input voltage	0		V_{CC}	0		V_{CC}	V
V_O Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH} High-level output current			–24			–24	mA
I_{OL} Low-level output current			24			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	0		10	ns/V
T_A Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT16544		74ACT16544		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}		I _{OH} = -50 µA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I _{OH} = -24 mA	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		I _{OH} = -75 mA†	5.5 V				3.85		3.85		
V _{OL}		I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I _{OL} = 24 mA	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		I _{OL} = 75 mA†	5.5 V					1.65		1.65	
I _I	Control inputs	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
I _{OZ} ‡	A or B ports	V _O = V _{CC} or GND	5.5 V			±0.5		±5		±5	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80		80	µA
ΔI _{CC} §		One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			0.9		1		1	mA
C _i	Control inputs	V _I = V _{CC} or GND	5 V		4.5						pF
C _{io}	A or B ports	V _O = V _{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		54ACT16544		74ACT16544		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	$\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low	5.5		5.5		5.5		ns
t _{su}	Setup time	Data before $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$	1.5		1.5		1.5		ns
		Data before $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$	1.5		1.5		1.5		
t _h	Hold time	Data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$	3		3		3		ns
		Data after $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$	3		3		3		

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT16544		74ACT16544		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.8	6.7	10	2.8	11.2	2.8	11.2	ns
t_{PHL}			4	7.5	10	4	11.2	4	11.2	
t_{PLH}	\overline{LEBA} or \overline{LEAB}	A or B	2.7	9	13.3	2.7	14	2.7	14	ns
t_{PHL}			2.8	8.5	12.1	2.8	13.5	2.8	13.5	
t_{PZH}	\overline{CEBA} or \overline{CEAB}	A or B	3.2	7.2	10.5	3.2	11.7	3.2	11.7	ns
t_{PZL}			3.8	8.2	12	3.8	13.6	3.8	13.6	
t_{PHZ}	\overline{CEBA} or \overline{CEAB}	A or B	5.8	8.2	10.3	5.8	11.1	5.8	11.1	ns
t_{PLZ}			5	7.4	9.4	5	10.2	5	10.2	
t_{PZH}	\overline{OEBA} or \overline{OEAB}	A or B	2.8	6.9	10.2	2.8	11.4	2.8	11.4	ns
t_{PZL}			3.6	7.9	11.7	3.6	13.3	3.6	13.3	
t_{PHZ}	\overline{OEBA} or \overline{OEAB}	A or B	5.2	7.7	9.8	5.2	10.5	5.2	10.5	ns
t_{PLZ}			3.4	6.8	8.8	3.4	9.6	3.4	9.6	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$		60	pF
		Outputs disabled			13	

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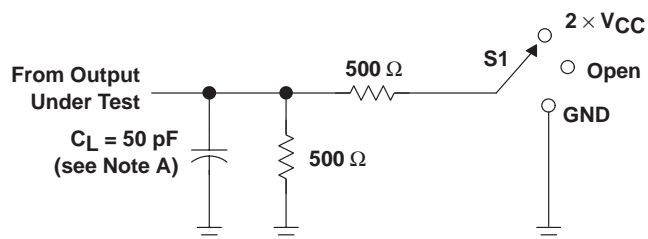
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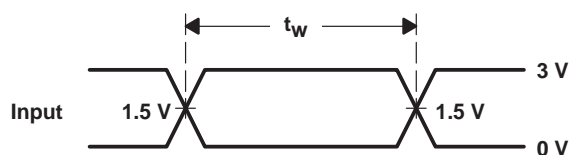
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PARAMETER MEASUREMENT INFORMATION

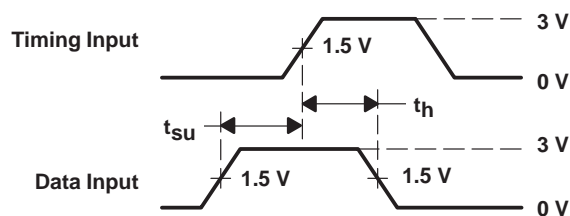


LOAD CIRCUIT

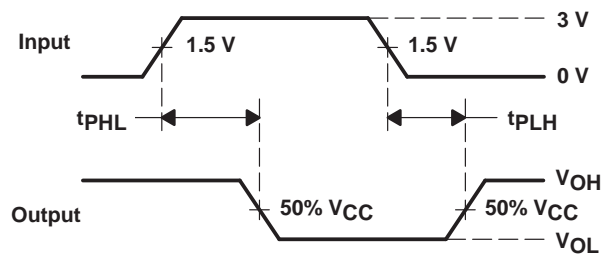
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



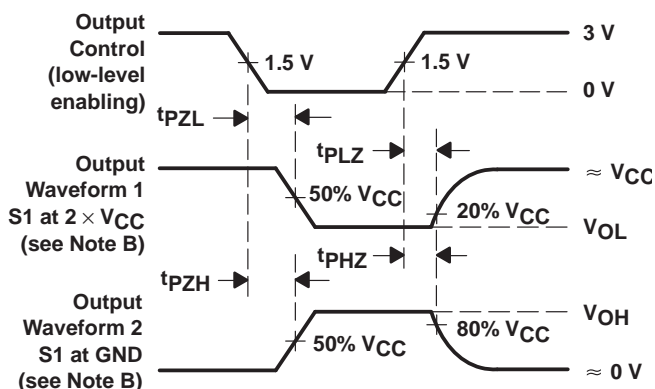
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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