CMOS 1K-bit serial E^2PROM
With memory protection, NS code

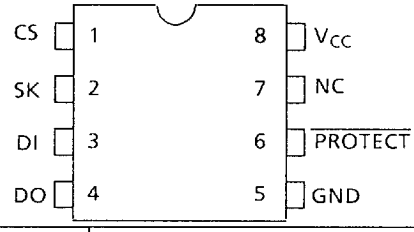
The S-2913CR/I is a high speed, low power 1K-bit E^2PROM that uses the CMOS floating-gate process. The organization is 64-word × 16-bit, and it is read or written serially. Continuous read operation is available, and at that time addresses are incremented bit-sequencially. Memory protection is valid in 512 bits (addresses 0 to 31).

■ Features

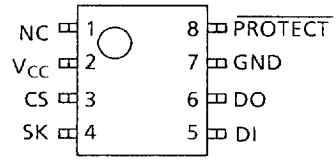
- Low power consumption
  - Operating: 2.0 mA max.
  - Standby: 1.0 μA max.
- Wide operating voltage range
  - Write : 2.7 to 6.5 V
  - Read : 1.8 to 6.5 V
- Write operation with built-in timer
- Word/chip erase operation
- Memory protection
- Rewritings: 10^4 or 10^5 times
- Data retention: 10 years

■ Pin Arrangement

8-pin DIP
Top view



8-pin SOP
Top view



CS	Chip select
SK	Serial clock
DI	Serial data input
DO	Serial data output
GND	Ground (0 V)

V_{CC}	Power supply voltage (+ 5 V)
$\overline{PROTECT}$	Memory protection control* Protection : Connected to GND or open Without protection : Connected to V_{CC}

* Memory protection

This function protects memory contents from erroneous writing when the CPU malfunctions. When the $\overline{PROTECT}$ pin is connected to GND or open, write to BANK1 (addresses 0 to 31) of the memory array is inhibited. Since $\overline{PROTECT}$ pin has a built-in pull-down resistor, a memory protection functions automatically when it is open.

Figure 1

■ Block Diagram

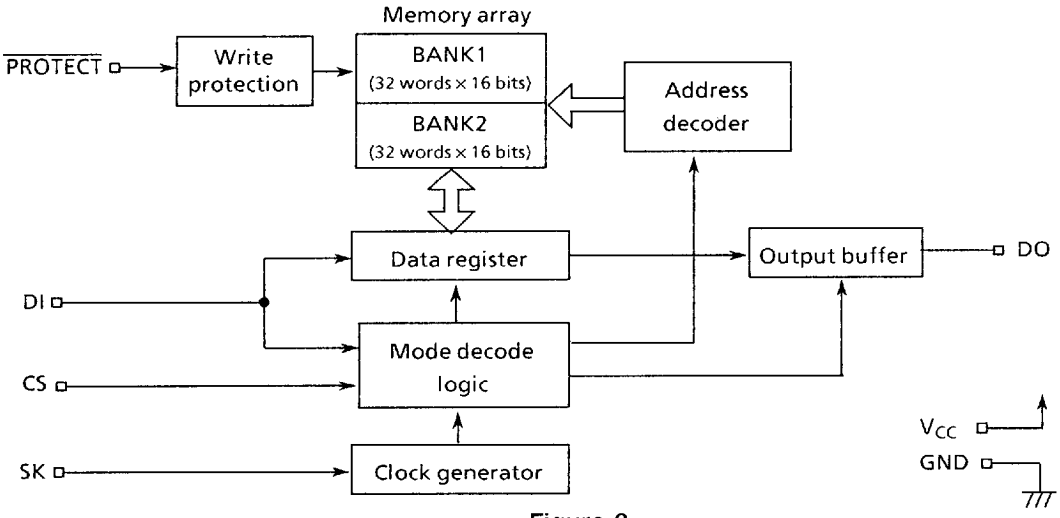


Figure 2

■ Instruction Set

Table 1

Instruction	Start bit	Op code	Address	Data
READ (Read data)	1	10	A_5 to A_0	D_{15} to D_0*
WRITE (Write data)	1	01	A_5 to A_0	D_{15} to D_0
WRAL (Write all)	1	00	01xxxx	D_{15} to D_0
ERASE (Erase data)	1	11	A_5 to A_0	—
ERAL (Erase all)	1	00	10xxxx	—
EWEN (Program enable)	1	00	11xxxx	—
EWDS (Program disable)	1	00	00xxxx	—

x : Don't care

*The 16-bit data in the specified address are read, then the data in the next address are continuously read

■ Absolute Maximum Ratings

Table 2

Item	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC}		-0.3 to +7.0	V
Input voltage	V_{IN}		-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}		-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	S-2913CR	-10 to +85	°C
		S-2913CI	-50 to +95	°C
Storage temperature	T_{stg}	S-2913CR	-65 to +125	°C
		S-2913CI	-65 to +150	°C

■ Recommended Operating Conditions

Table 3

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read	1.8	—	6.5	V
		Write	2.7	—	6.5	V
High level input voltage	V_{IH}	V_{CC} = 5.0 ± 10%	2.0	—	V_{CC}	V
		V_{CC} = 2.7 to 6.5V	0.8 × V_{CC}	—	V_{CC}	V
		V_{CC} = 1.8 to 2.7V	0.8 × V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}	V_{CC} = 5.0 ± 10%	0.0	—	0.8	V
		V_{CC} = 2.7 to 6.5V	0.0	—	0.15 × V_{CC}	V
		V_{CC} = 1.8 to 2.7V	0.0	—	0.2 × V_{CC}	V
Operating temperature	T_{opr}	S-2913CR	0	—	+70	°C
		S-2913CI	-40	—	+85	°C

■ DC Electrical Characteristics

Table 4

(S-2913CR : Ta = 0°C to 70°C, S-2913CI : Ta = -40°C to 85°C)

Item	Smbl	Conditions	Read/write operations						Read operation			Unit
			V_{CC} = 5.0 V ± 10 %			V_{CC} = 3.0 V ± 10 %			V_{CC} = 1.8 to 2.7 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	DO unloaded	—	—	2.0	—	—	1.0	—	—	0.5	mA
Current consumption (PROGRAM)	I_{CC2}	DO unloaded	—	—	5.0	—	—	2.0	—	—	—	mA

Table 5

(S-2913CR : Ta = 0°C to 70°C, S-2913CI : Ta = -40°C to 85°C)

Item	Smbl	Conditions	Read/write operations						Read operation			Unit
			V_{CC} = 5.0 V ± 10 %			V_{CC} = 2.7 to 6.5 V			V_{CC} = 1.8 to 2.7 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	Input: V_{CC} or GND	—	—	1.0	—	—	1.0	—	—	1.0	µA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Low level output voltage	V_{OL}	CMOS I_{OL} = 100 µA	—	—	0.1	—	—	0.1	—	—	0.1	V
		TTL I_{OL} = 2.1 mA	—	—	0.45	—	—	—	—	—	—	V
High level output voltage	V_{OH}	CMOS V_{CC} = 2.7 to 6.5 V: I_{OH} = -100 µA V_{CC} = 1.8 to 2.7 V: I_{OH} = -10 µA	V_{CC}-0.7	—	—	V_{CC}-0.7	—	—	V_{CC}-0.3	—	—	V
		TTL, I_{OH} = -400 µA	2.4	—	—	—	—	—	—	—	—	V
Write enable latch data hold voltage	V_{DH}		1.5	—	—	1.5	—	—	1.5	—	—	V
Pull down current	I_{PD}	$\overline{PROTECT}$ = V_{CC}	15	40	120	4	—	200	1	—	40	µA

■ Rewriting Times

Table 6

(S-2913CR : Ta = 0°C to 70°C, S-2913CI : Ta = -40°C to 85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rewriting times	N_W	S-2913CR/I01	10^4	—	—	times/word
		S-2913CR/I10	10^5	—	—	times/word

■ Pin Capacitance

Table 7

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V	—	—	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V	—	—	10	pF

■ AC Electrical Characteristics

Table 8 Measuring conditions

Input voltage level	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output voltage level	$0.5 \times V_{CC}$
Output load	100pF

Table 9

(S-2913CR : Ta = 0°C to 70°C, S-2913CI : Ta = -40°C to 85°C)

Item	Symbol	Read / Write operations						Read operation			Unit
		V_{CC} = 5.0 ± 10%			V_{CC} = 2.7 to 6.5 V			V_{CC} = 1.8 to 2.7 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS setup time	t_{CSS}	0.2	—	—	0.4	—	—	1.0	—	—	µs
CS hold time	t_{CSH}	0.2	—	—	0.4	—	—	1.0	—	—	µs
CS deselect time	t_{CDS}	0.2	—	—	0.2	—	—	0.4	—	—	µs
Data setup time	t_{DS}	0.2	—	—	0.4	—	—	0.8	—	—	µs
Data hold time	t_{DH}	0.2	—	—	0.4	—	—	0.8	—	—	µs
1 data output delay	t_{PD1}	—	—	0.4	—	—	1.0	—	—	2.0	µs
0 data output delay	t_{PD0}	—	—	0.4	—	—	1.0	—	—	2.0	µs
Clock frequency	f_{SK}	0.0	—	2.0	0.0	—	0.5	0.0	—	0.2	MHz
Clock pulse width	t_{SKH}, t_{SKL}	0.25	—	—	1.0	—	—	2.5	—	—	µs
Output disable time	t_{HZ}	0	50	150	0	500	1000	—	—	—	ns
Output enable time	t_{SV}	0	50	150	0	500	1000	—	—	—	ns
Program time	t_{PR}	2.0	4.0	10	2.0	4.0	10	—	—	—	ms

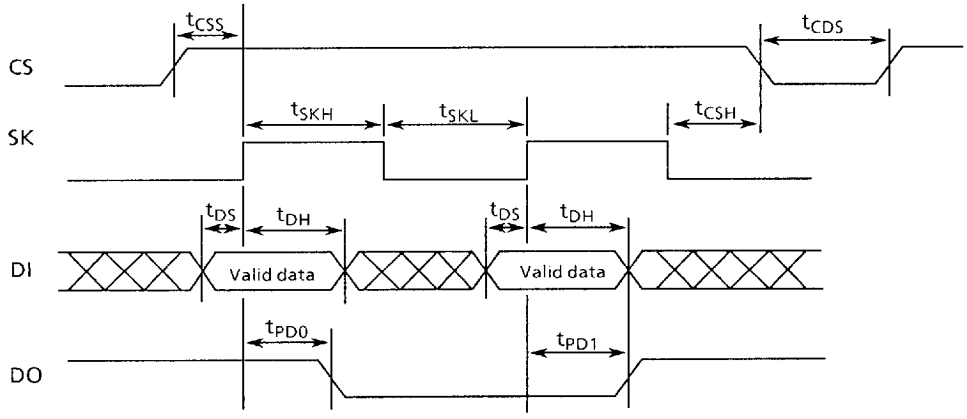


Figure 3 Timing chart

■ Operation

Note

- CS must be "L" between instructions.
- SK and DI must be "L" during verify operation.
- It is not necessary to erase data before WRITE or WRAL operation.

(1) Read mode

This mode reads data from a specified address. By the READ instruction, data is triggered at the rise of SK, and output serially to the DO pin. When the final data in the specified address has been read, an SK is sent and the data in the next address is read at the rise of SK. The READ instruction is executed regardless of program enable or disable mode.

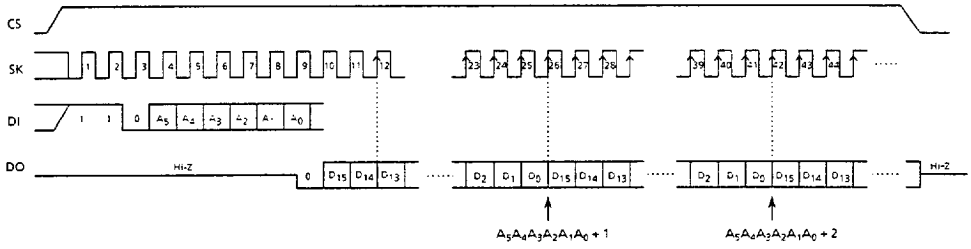


Figure 4 Read mode timing

(2) Write data mode

After the WRITE instruction, address and data are sent in program enable mode, CS must be low once. At the falling edge of its low, data is written into the specified address. This operation is performed by the internal auto-timing generation circuit and SK is not necessary. The READY/$\overline{\text{BUSY}}$ status can be found by CS high level and checking DO pin. During write operation, low level is output to the DO pin, and after operation, high level is output.

Note : When the $\overline{\text{PROTECT}}$ pin is connected to GND or open, the WRITE instruction to BANK1 is invalid and data cannot be written into BANK1.

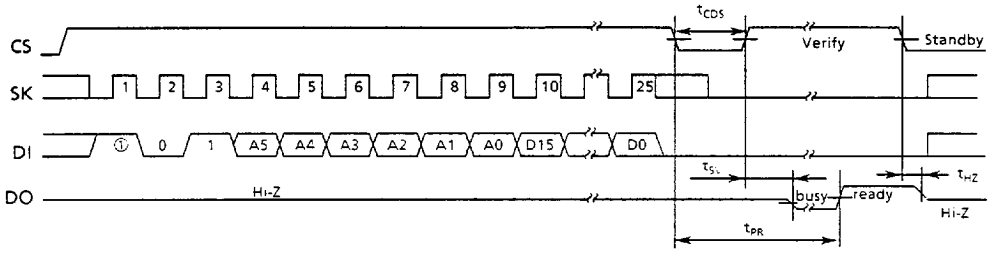


Figure 5 Write data mode timing

(3) Write all (WRAL) mode

After the WRAL instruction is sent, in program enable mode, CS must be low once. At the falling edge of its low, the same data is written into all memory array bits. This operation is performed by the internal auto-timing generation circuit and SK is not necessary. The READY/$\overline{\text{BUSY}}$ status can be found by CS high level and checking DO pin. During write operation, low level is output to the DO pin, and after operation, high level is output.

NOTE : When the $\overline{\text{PROTECT}}$ pin is connected to GND or open, the WRAL instruction to BANK1 is invalid, and data cannot be written into BANK1.

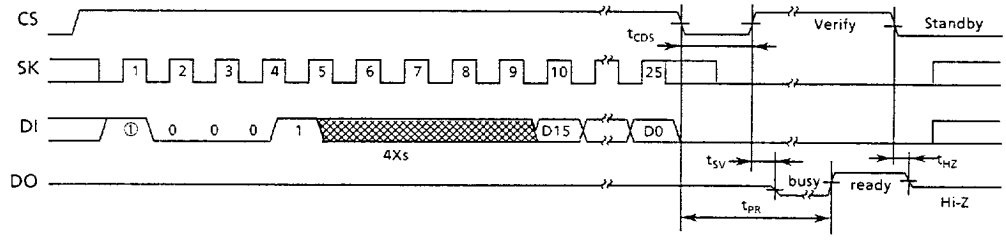


Figure 6 WRAL mode timing

(4) Erase data mode

After the ERASE instruction and address are sent in program enable mode, CS must be low once. At the falling edge of its low, erase operation of data in the specified address is started. This operation is performed by the internal auto-timing generation circuit and SK is not necessary. The READY/$\overline{\text{BUSY}}$ status can be found by CS high level and checking DO pin. During erase operation, low level is output to the DO pin, and after operation, high level is output.

NOTE : When the $\overline{\text{PROTECT}}$ pin is connected to GND or open, the ERASE instruction to BANK1 is invalid and the data in BANK1 cannot be erased.

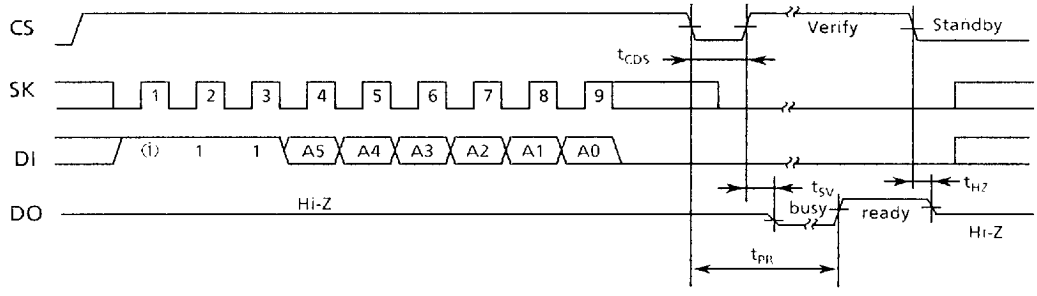


Figure 7 Erase data mode timing

(5) Erase all (ERAL) mode

After the ERAL instruction is sent, in program enable mode, CS must be low once. At the falling edge of its low, erase operation of all memory array bits is started, and set to 1. This operation is performed by the internal auto-timing generation circuit and SK is not necessary. The READY/$\overline{\text{BUSY}}$ status can be found by CS high level and checking DO pin. During erase operation, low level is output to the DO pin, and after operation, high level is output.

NOTE : When the $\overline{\text{PROTECT}}$ pin is connected to GND or open, the ERAL instruction to BANK1 is invalid and the data in BANK1 cannot be erased.

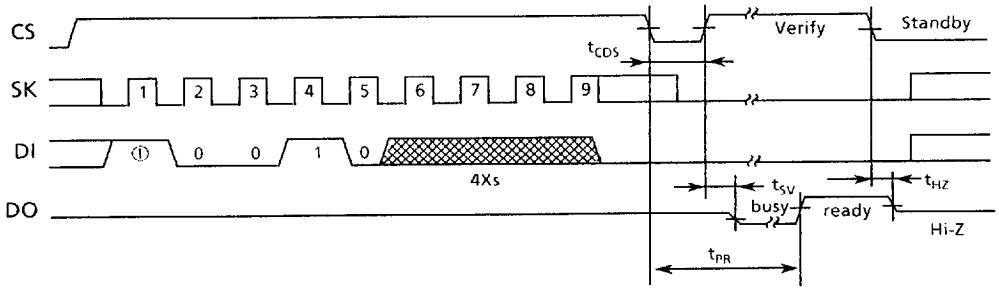


Figure 8 ERAL mode timing

(6) Program enable (EWEN) and program disable (EWDS) modes

The EWEN instruction puts the S-2913CR/I into program enable (EWEN) mode. In this mode, WRITE, WRAL, ERASE and ERAL instructions are enabled. The S-2913CR/I remains in EWEN mode until an EWDS instruction is executed. The EWDS instruction puts the S-2913CR/I into program disable (EWDS) mode. The WRITE, WRAL, ERASE and ERAL instructions are ignored in the EWDS mode; this mode is used to protect data against accidental programming. The S-2913CR/I is in program disable mode when power is turned on.

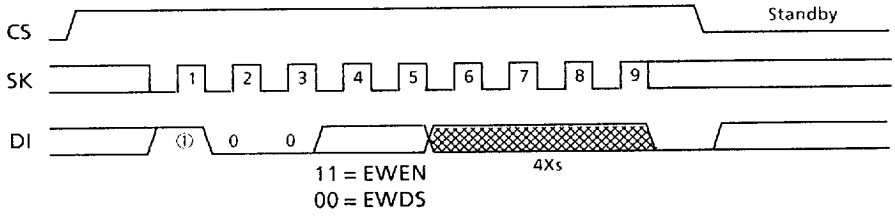


Figure 9 EWEN/EWDS mode timing

■ Dimensions (Unit:mm)

1. S-2913CR/I (8-pin DIP)

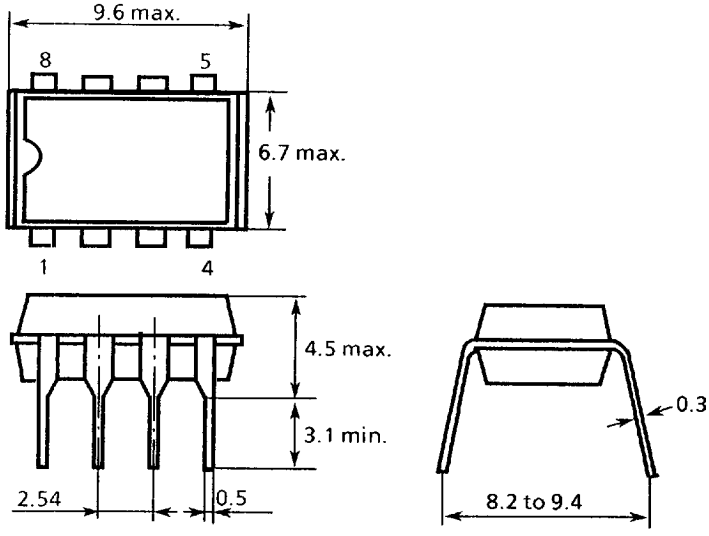


Figure 10

2. S-2913CRF/IF (8-pin SOP)

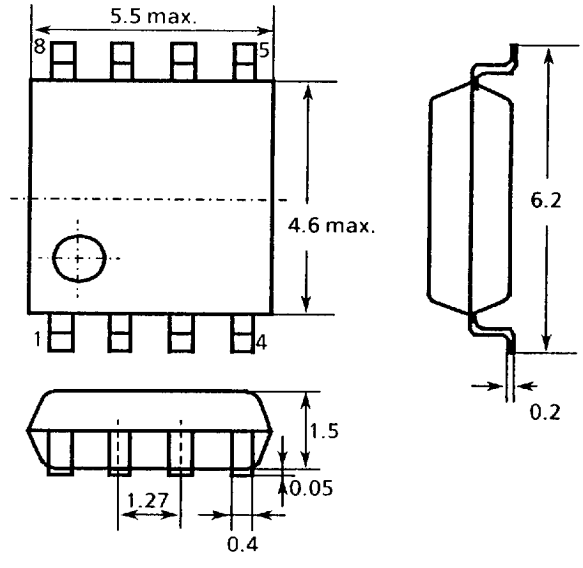


Figure 11

■ Ordering Information

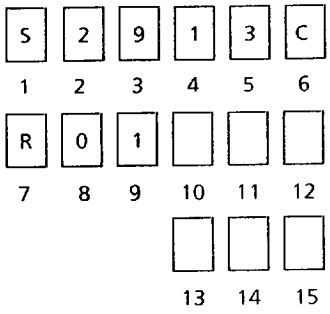
Table 10

Product name	Rewritings / word	Temperature	Package
S-2913CR01	10^4	0°C to 70°C	DIP plastic
S-2913CRF01	10^4	0°C to 70°C	SOP plastic
S-2913CI01	10^4	-40°C to 85°C	DIP plastic
S-2913CIF01	10^4	-40°C to 85°C	SOP plastic
S-2913CR10	10^5	0°C to 70°C	DIP plastic
S-2913CRF10	10^5	0°C to 70°C	SOP plastic
S-2913CI10	10^5	-40°C to 85°C	DIP plastic
S-2913CIF10	10^5	-40°C to 85°C	SOP plastic

Note : Each bit is set to 1 before delivery.

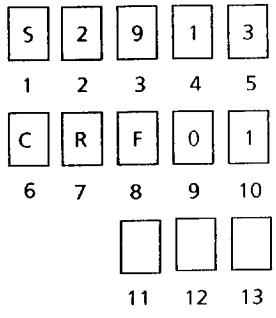
■ Markings

1. S-2913CR/I (8-pin DIP)



1 to 6 : Product name
7 : Temperature : R = 0°C to 70°C, I = -40°C to 85°C
8 to 9 : Min. rewriting time : 01 = 10^4, 10 = 10^5
10 to 12 : Lot No.
13 : Assembly mark
14 : Last column of year
15 : Month of manufacture: January = 1, February = 2, March = 3, April = 4, May = 5, June = 6, July = 7, August = 8, September = 9, October = X, November = Y, December = Z

2. S-2913CRF/IF (8-pin SOP)

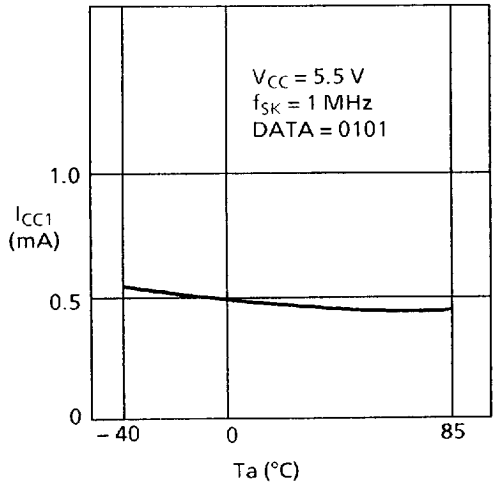


1 to 6 : Product name
7 : Temperature : R = 0°C to 70°C, I = -40°C to 85°C
8 : Package : F = SOP
9 to 10 : Min. rewriting time : 01 = 10^4, 10 = 10^5
11 : Month of manufacture: January = 1, February = 2, March = 3, April = 4, May = 5, June = 6, July = 7, August = 8, September = 9, October = X, November = Y, December = Z
12 to 13 : Lot No.

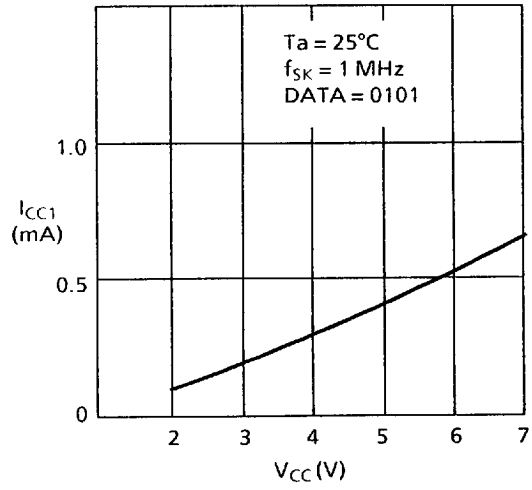
■ Characteristics

1. DC Characteristics

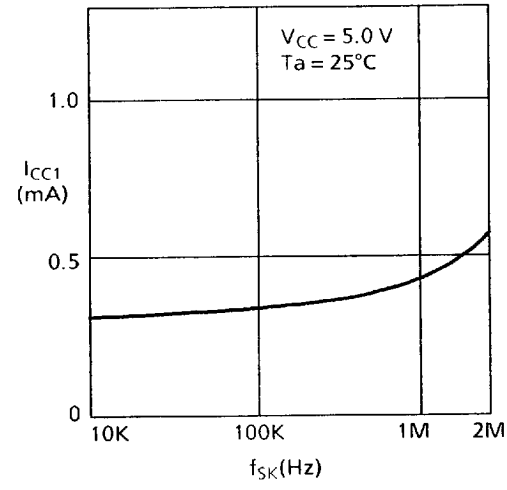
1.1 Current consumption (READ) I_{CC1} — Ambient temperature Ta



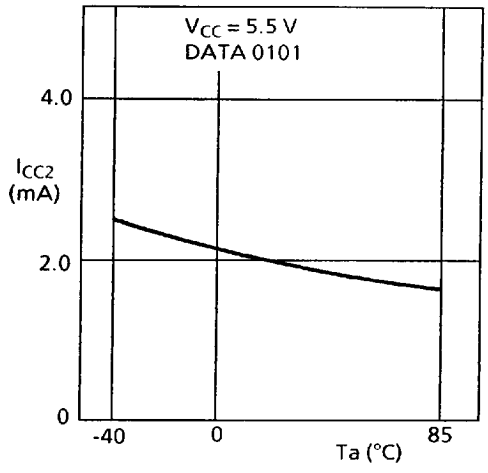
1.2 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



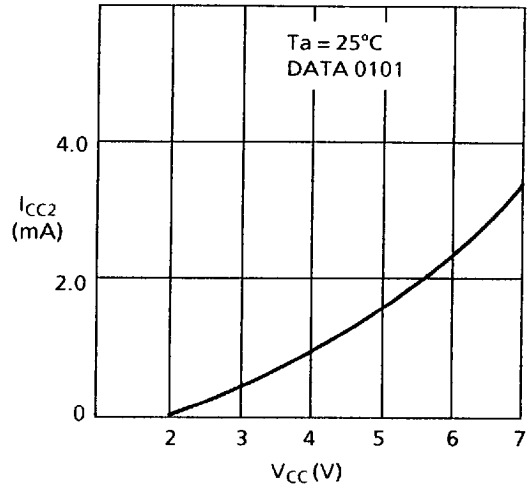
1.3 Current consumption (READ) I_{CC1} — Clock frequency f_{SK}



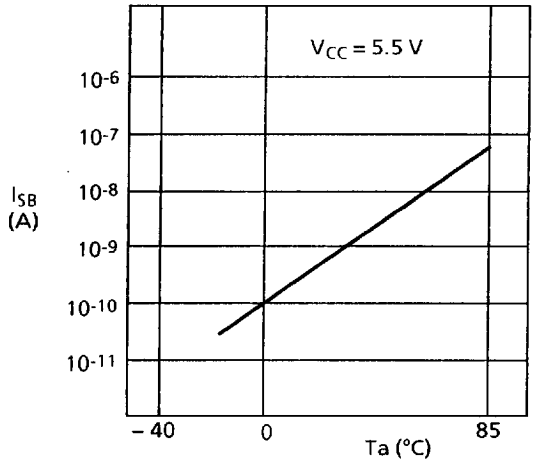
1.4 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



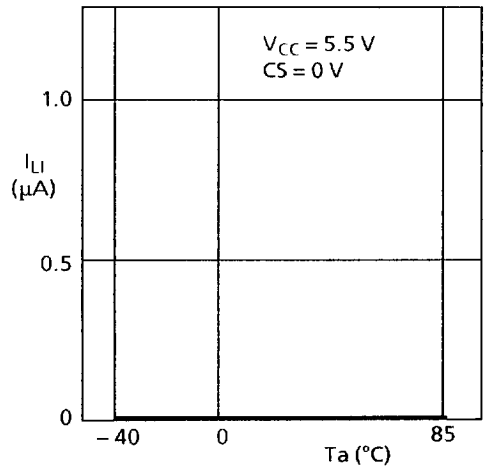
1.5 Current consumption (PROGRAM) I_{CC2} – Power supply voltage V_{CC}



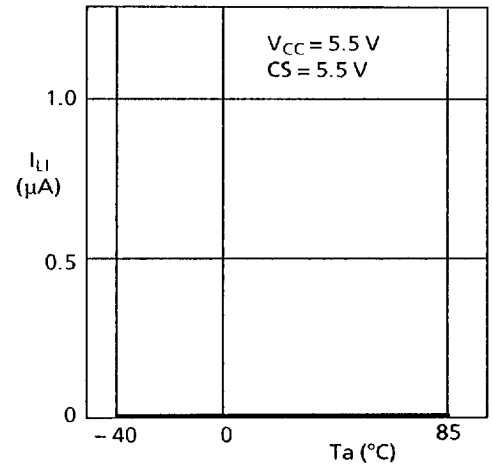
1.6 Standby current consumption I_{SB}— Ambient temperature Ta



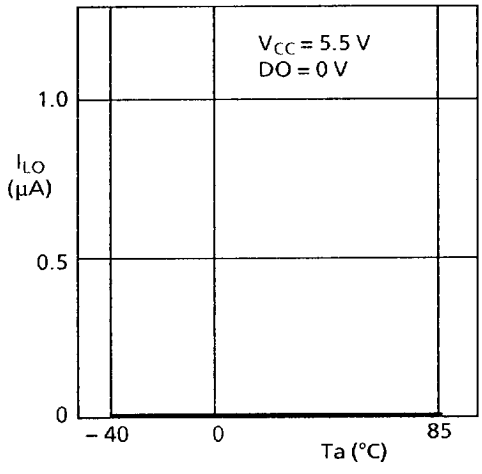
1.7 Input leakage current I_{LI} – Ambient temperature Ta



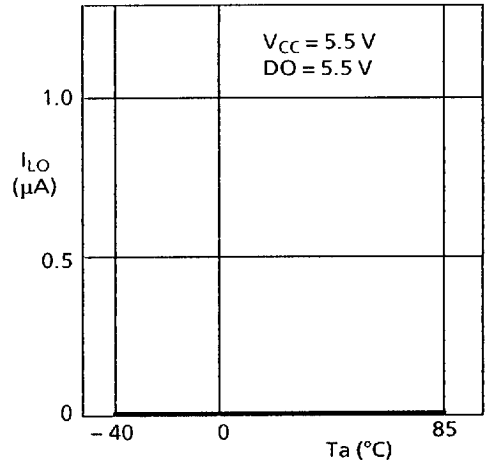
1.8 Input leakage current I_{LI} – Ambient temperature Ta



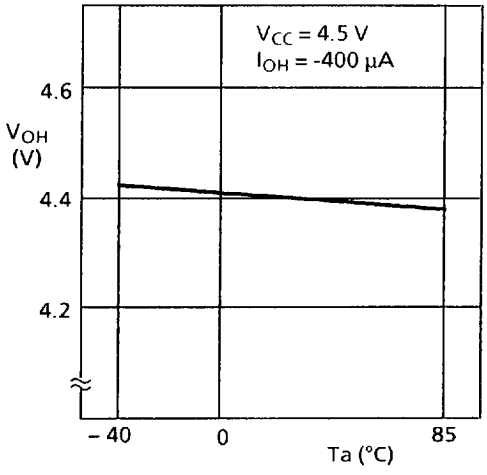
1.9 Output leakage current I_{LO} – Ambient temperatureTa



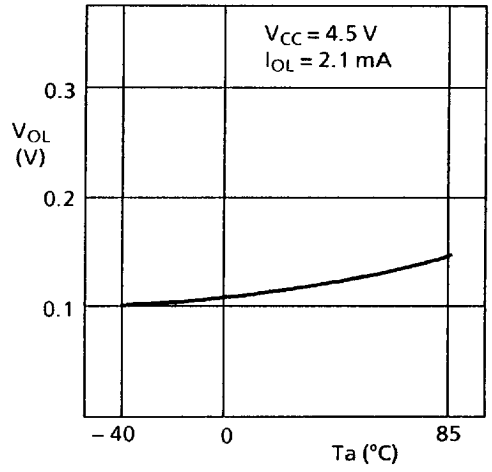
1.10 Output leakage current I_{LO} – Ambient temperature Ta



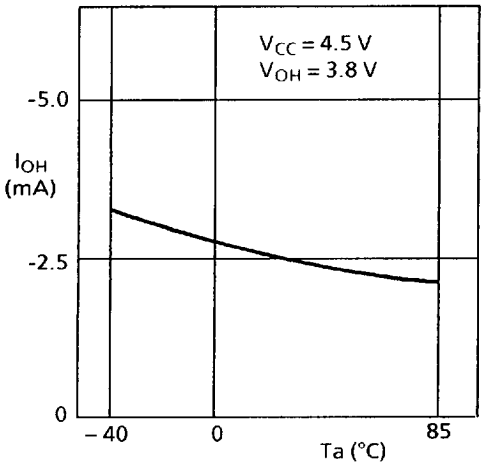
1.11 High level output voltage V_{OH} – Ambient temperature Ta



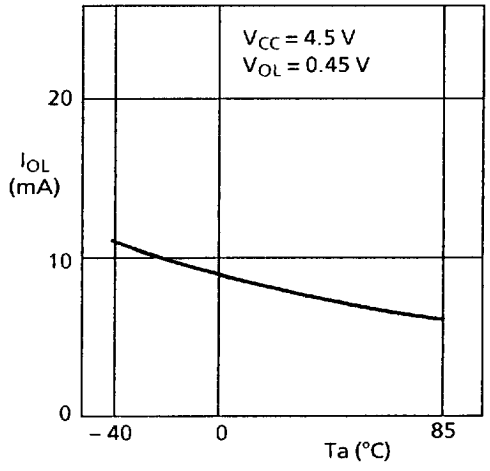
1.12 Low level output voltage V_{OL} – Ambient temperature Ta



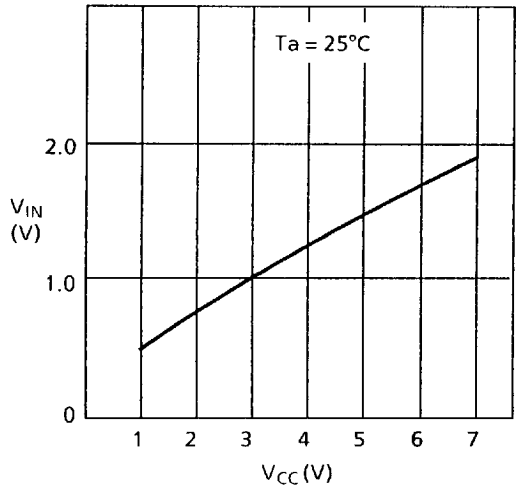
1.13 High level output current I_{OH} – Ambient temperature Ta



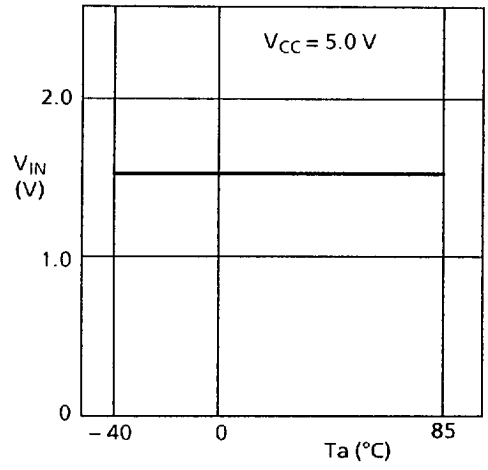
1.14 Low level output current I_{OL} – Ambient temperature Ta



1.15 Input voltage V_{IN} – Power supply voltage V_{CC}

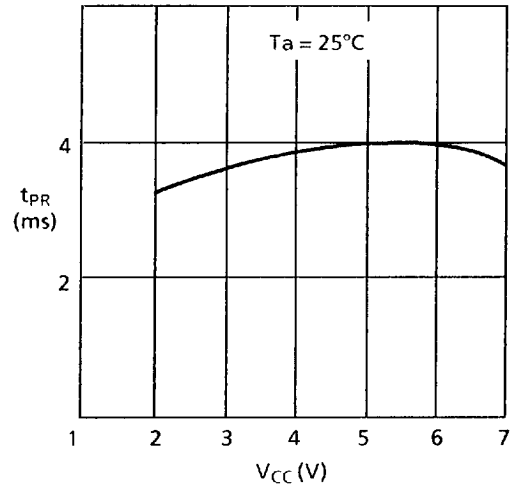


1.16 Input voltage V_{IN} – Ambient temperature Ta

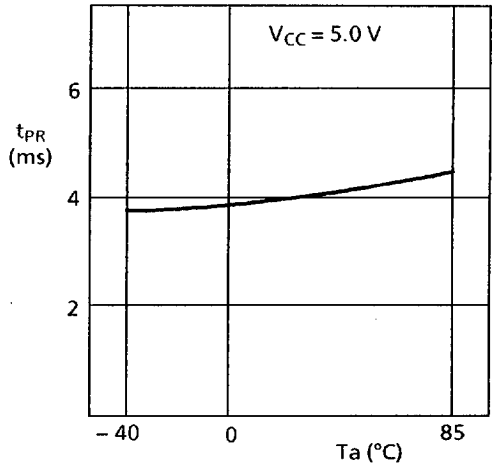


2. AC Characteristics

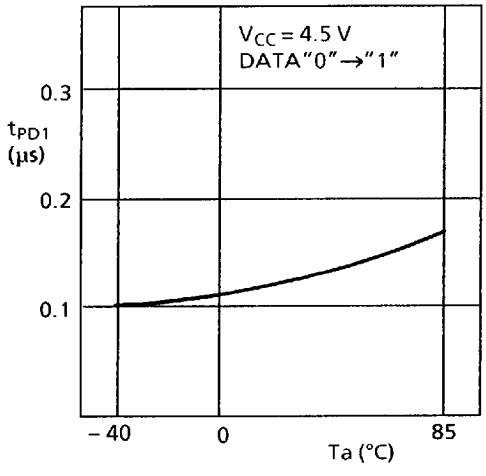
2.1 Program time t_{PR} – Power supply voltage V_{CC}



2.2 Program time t_{PR} – Ambient temperature Ta



2.3 1 data output delay time t_{PD1} – Ambient temperature Ta



2.4 0 data output delay time t_{PD0} – Ambient temperature Ta