

CMOS System Reset Monolithic IC PST4XXAXXXN Series

Outline

This is a reset IC for systems developed using the CMOS process. The CMOS process allows ultra-low current consumption of 1.5 μ A typ. Further, a fixed delay timer is built in, so that power voltage is verified when power is turned on or interrupted for accurate system reset.

Features

- | | |
|---|-------------------------------------|
| 1 Detection voltage precision | $\pm 1.5\%$ (25°C, VDD = VDET + 0.1 |
| 2 Low current consumption | SOT-23 : 1.5 μ A |
| 3 External capacitor for delay timer not required. | |
| Built-in delay timer | SOT-23 : 50/100/200/240/400ms |
| 4 Full line of rank variation available for detection voltage, package, output form, delay timer. | |
| 5 Supports car devices with operating temperature range of | -40 ~ +105°C. |

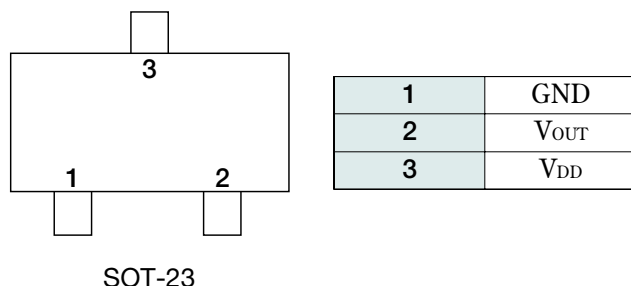
Package

SOT-23

Applications

1. Reset circuits in microcomputers, CPUs and MPUs
2. Logic circuit reset circuits.
3. Battery voltage check circuits.
4. Back-up power supply switching circuits.
5. Level detection circuits.
6. Mechanical reset circuits.

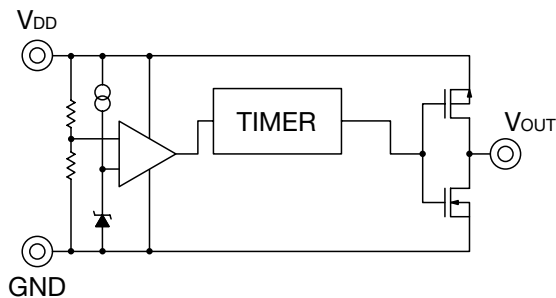
Pin Assignment



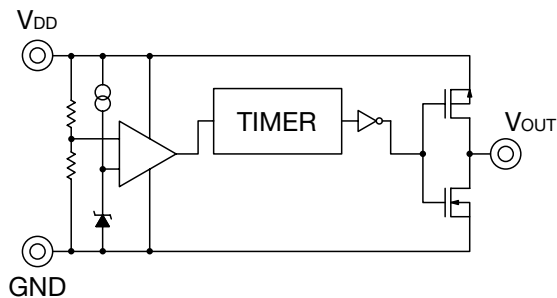
Block Diagram

CMOS Output

PST41□A□□□N□ Active-Low Output

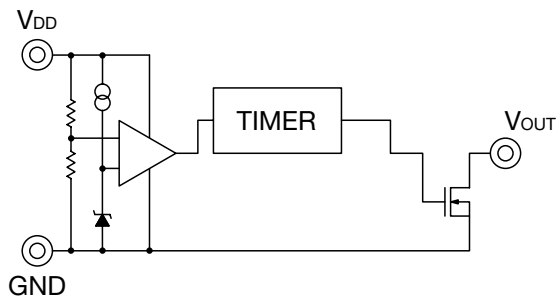


PST43□A□□□N□ Active-High Output

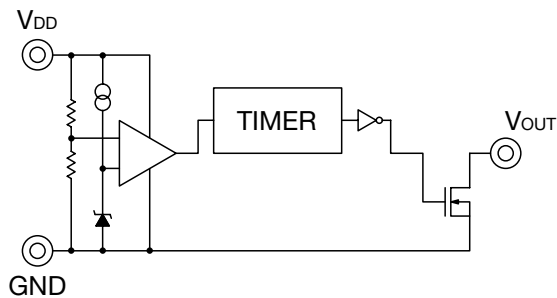


N-ch Open Drain Output

PST42□A□□□N□ Active-Low Output



PST44□A□□□N□ Active-High Output



Pin Explanations

Pin No.	Pin Name	Function	Internal Equivalent Circuit
1	GND	GND Pin	Refer to 4.Block Diagram.
2	V _{OUT}	Reset Signal Output Pin	
3	V _{DD}	Power Supply Pin/Voltage Detect Pin	

Pin Explanations

PST4□□A□□□N□
a b d f

a		b		d		f	
Output Type		T _{DEL} Rank		V _{DET} Rank		Packing Specifications	
1	CMOS Output Active-Low Output	1	50ms	160	V _{DET} =1.60V	R	R Housing
2	N-ch Open Drain Output Active-Low Output	2	100ms	1	1	L	L Housing
3	CMOS Output Active-High Output	3	200ms	480	V _{DET} =4.80V		
4	N-ch Open Drain Output Active-High Output	4	240ms				
		5	400ms				

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Operating Temperature	T _{OPR}	-40~+105	°C
Storage Temperature	T _{STG}	-65~+160	°C
Supply Voltage	V _{DD max.}	6.5	V
Output Voltage	V _{OUT}	GND-0.3~V _{DD max.} +0.3(CMOS Type) GND-0.3~6.5(N-ch Open Drain Type)	V
Output Current	I _{OUT}	20	mA
Power Dissipation	P _D	150	mW

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Operating Temperature	T _{OPR}	-40~+105	°C

Electrical Characteristics (Unless otherwise specified, Ta=25°C)

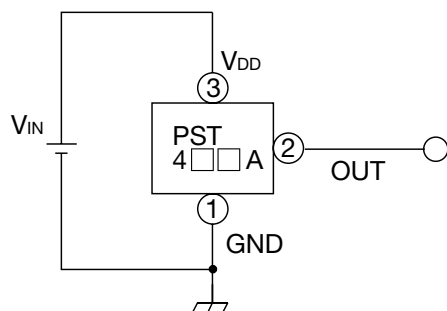
Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V _{DD} Range	V _{DD}	Test Circuit 1	1.0		6.0	V
Detecting Voltage	V _{DET}	Test Circuit 1	-1.5%	1.6V~4.8V (0.1V STEP)	+1.5%	V
Detecting Voltage Temp. Coefficient	V _{DET} /ΔT	-40°C ≤ T _{OPR} ≤ 105°C Test Circuit1		±30		ppm/°C
Supply Current	I _{SS}	V _{DD} =V _{DET} +0.1 Test Circuit 2		1.5	3.5	μA
"H" Out put Voltage (PST41□A /42□A)	V _{OH}	PST4□□□160N□~ PST4□□□230N□ V _{DD} =V _{DET} -0.1V I _{OUT} =150μA	0.8V _{DD}			V
		PST4□□□240N□~ PST4□□□350N□ V _{DD} =V _{DET} -0.1V I _{OUT} =500μA				
		PST4□□□360N□~ PST4□□□480N□ V _{DD} =V _{DET} -0.1V I _{OUT} =800μA				
		Test Circuit 6				
"L" Out put Voltage (PST41□A /42□A)	V _{OL}	PST4□□□160N□~ PST4□□□350N□ V _{DD} =V _{DET} +0.1V I _{OUT} =1.2mA			0.3	V
		PST4□□□360N□~ PST4□□□480N□ V _{DD} =V _{DET} +0.1V I _{OUT} =3.2mA			0.4	V
		Test Circuit 7				
"H" Out put Voltage (PST43□A /44□A)	V _{OH}	PST4□□□160N□~ PST4□□□230N□ V _{DD} =V _{DET} +0.1V I _{OUT} =150μA	0.8V _{DD}			V
		PST4□□□240N□~ PST4□□□350N□ V _{DD} =V _{DET} +0.1V I _{OUT} =500μA				
		PST4□□□360N□~ PST4□□□480N□ V _{DD} =V _{DET} +0.1V I _{OUT} =800μA				
		Test Circuit 6				
"L" Out put Voltage (PST43□A /44□A)	V _{OL}	PST4□□□160N□~ PST4□□□350N□ V _{DD} =V _{DET} -0.1V I _{OUT} =1.2mA			0.3	V
		PST4□□□360N□~ PST4□□□480N□ V _{DD} =V _{DET} -0.1V I _{OUT} =3.2mA			0.4	V
		Test Circuit 7				
Reset Active Timeout Period	T _{DEL}	Test Circuit 8	35	50	65	ms
			70	100	130	
			140	200	260	
			170	240	310	
			280	400	520	
V _{DD} to Reset Delay	T _{DET}	Test Circuit 8		20		μs
Output Leakage Current (PST42□A /44□A)	I _{LEAK}	Test Circuit 5			0.1	μA

Note 1: This device is tested at only normal temperature. Over temperature limit guaranteed by design only.

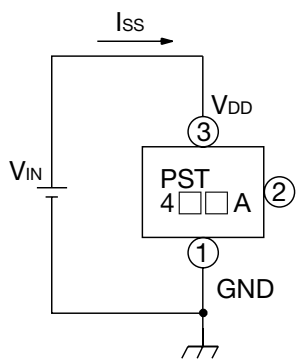
Note 2: This device has no Hysteresis Voltage.

Measuring Circuit

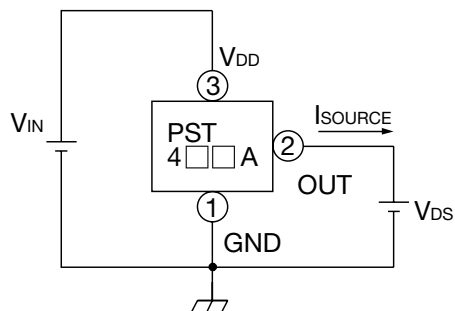
(1)-a PST41□A / 43□A



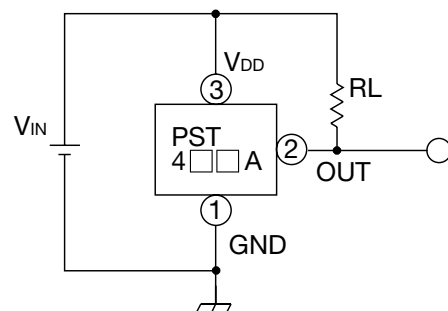
(2)



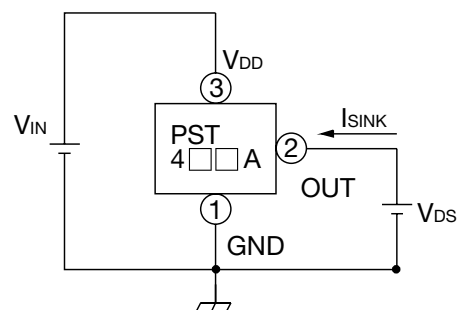
(4)



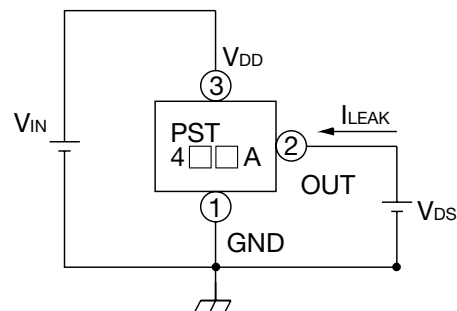
(1)-b PST42□A / 44□A



(3)

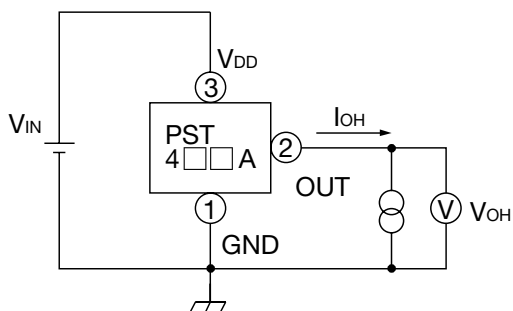


(5)

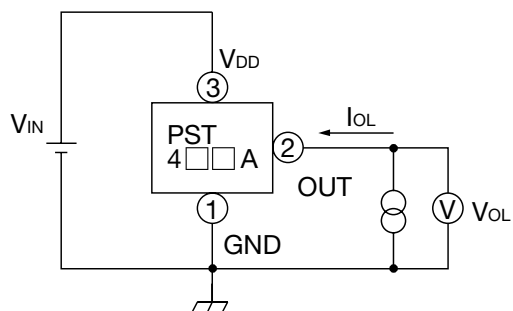


Measuring Circuit

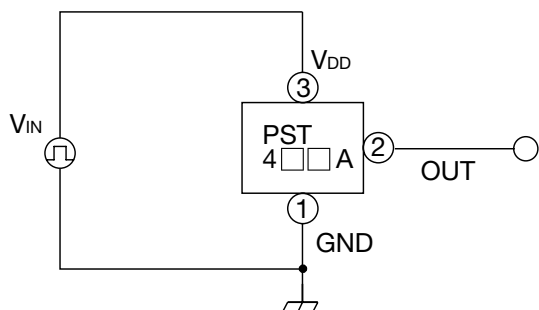
(6)



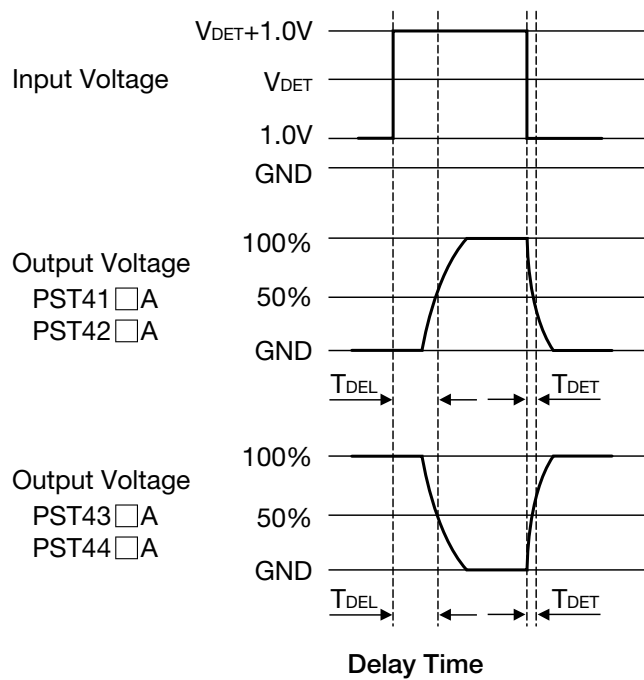
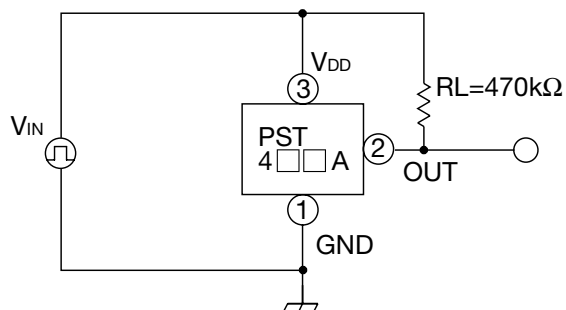
(7)



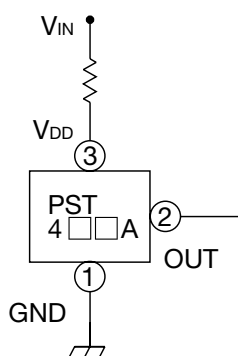
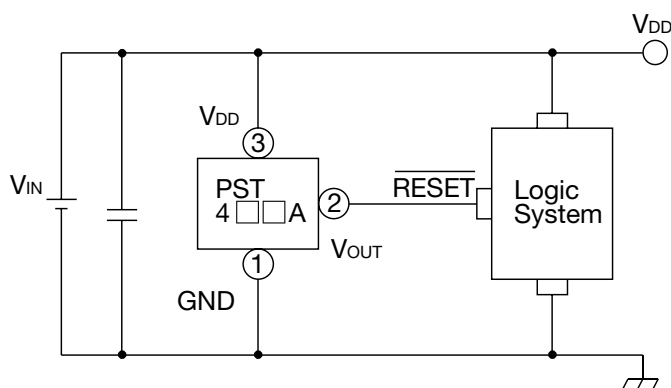
(8) PST41□A / 43□A



(9) PST42□A / 44□A



Application Circuits



Please note that there is any possibility of circuit oscillation when resistance put in the line V_{IN}.

Load current and load resistance should be adjusted, which not over power dissipation level.

$$PD > (V_{DD} - V_{OH}) \cdot I_{OH}$$

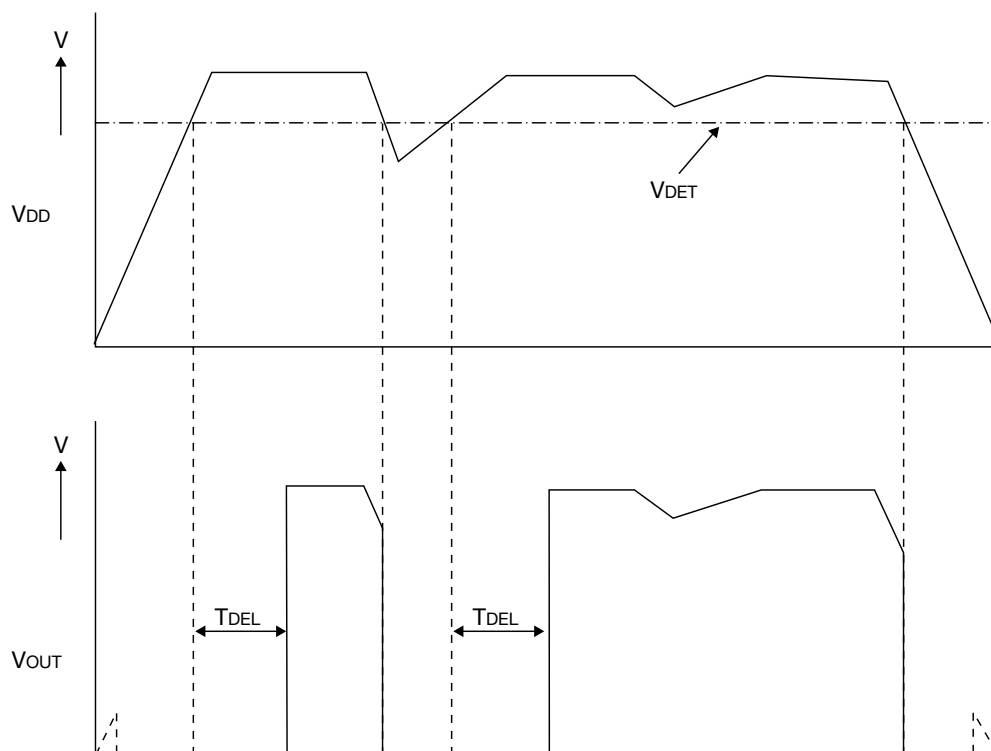
$$PD > V_{OL} \cdot I_{OL}$$

We shall not be liable for any trouble or damage caused by using this circuit.

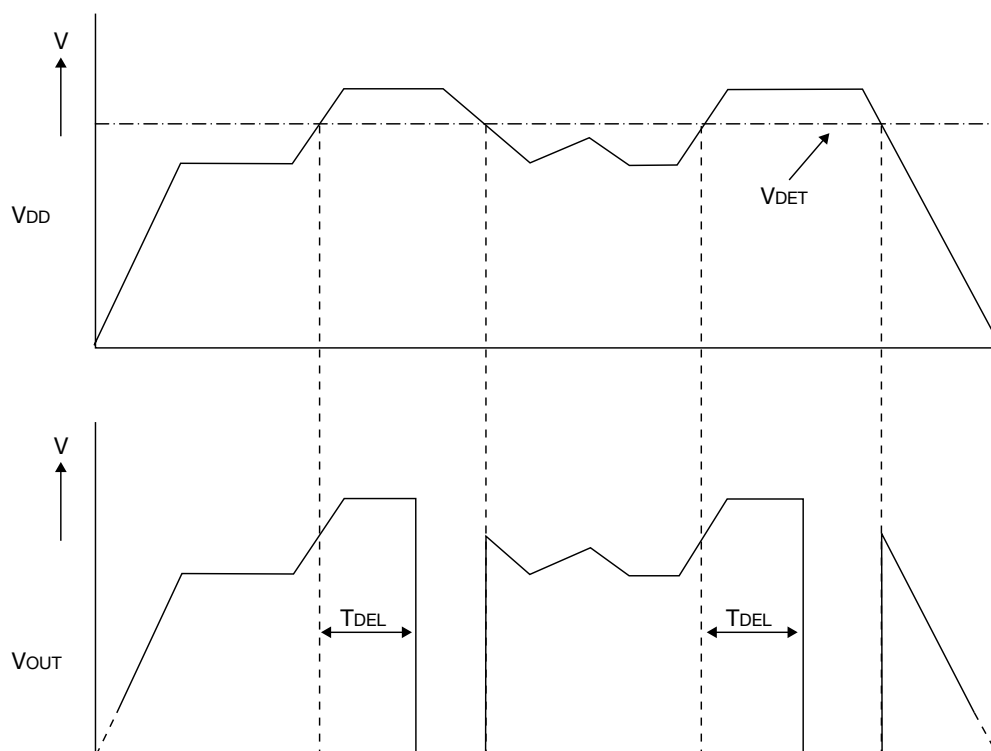
In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi Electric Co., Ltd. shall not be liable for any such problem, nor grant a license therefore.

Timing Chart

■ PST41 □ A / 42 □ A Active-Low Output

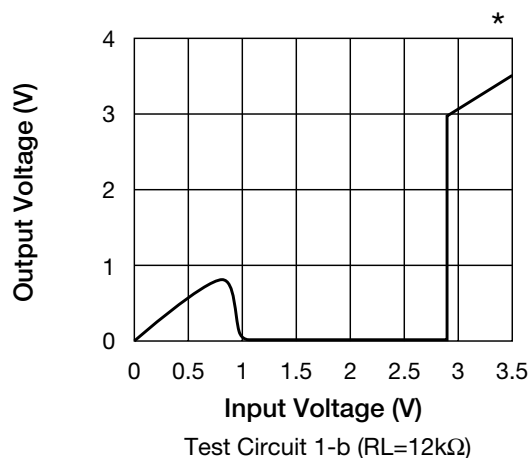


■ PST43 □ A / 44 □ A Active-High Output

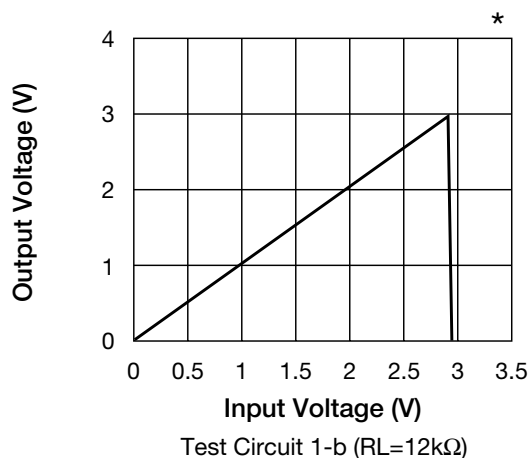


Characteristics

Detecting voltage (PST414A290N□)

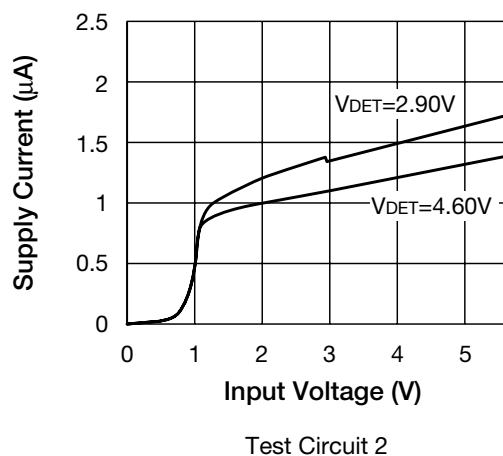


Detecting voltage (PST434A290N□)

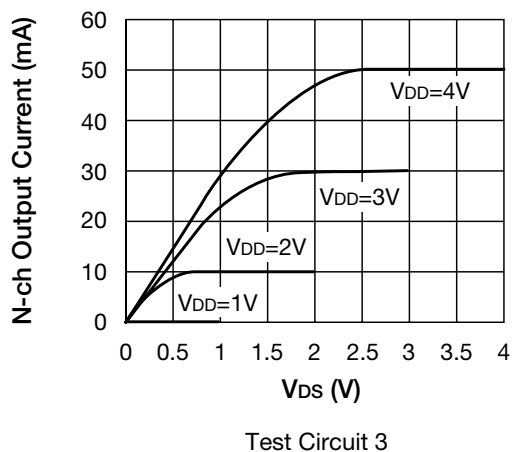


* When Input Voltage is Under 1.0V, Output Voltage is Unstable.

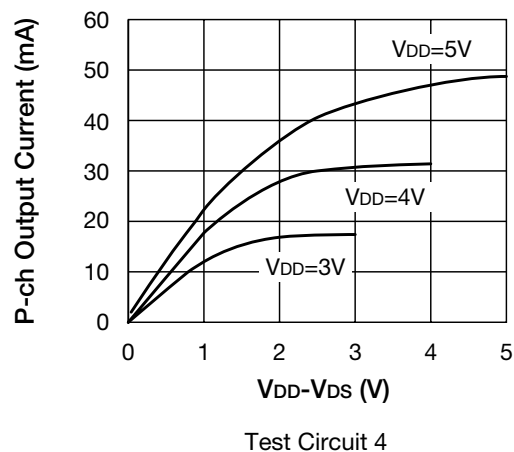
Supply current



N-ch Output current (PST414A460N□)



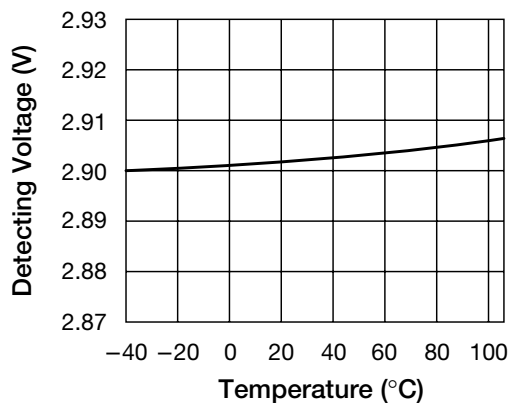
P-ch Output current (PST414A290N□)



Note: These are typical characteristics.

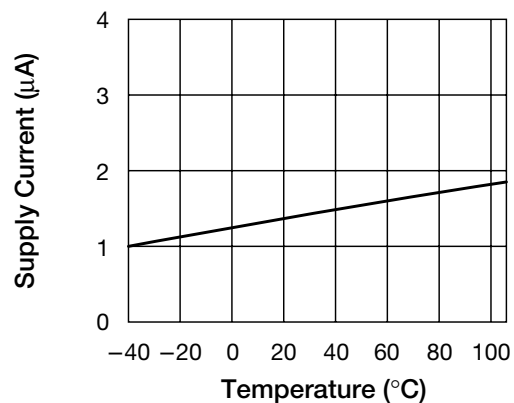
Characteristics

Detecting voltage vs temperature (PST414A290N□)



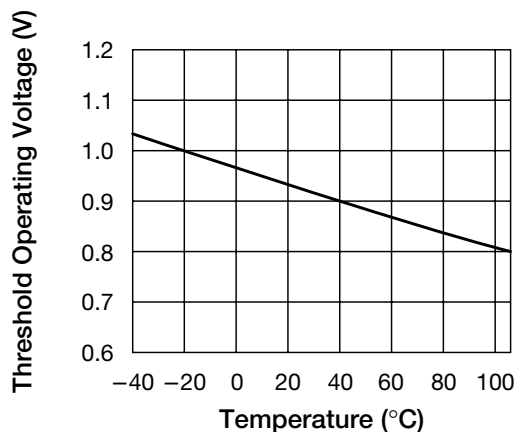
Test Circuit 1-a

Supply current vs temperature (PST414A290N□)



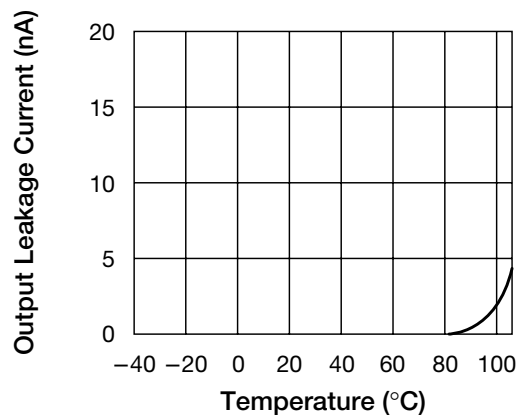
Test Circuit 2

Threshold Operating Voltage Vs temperature



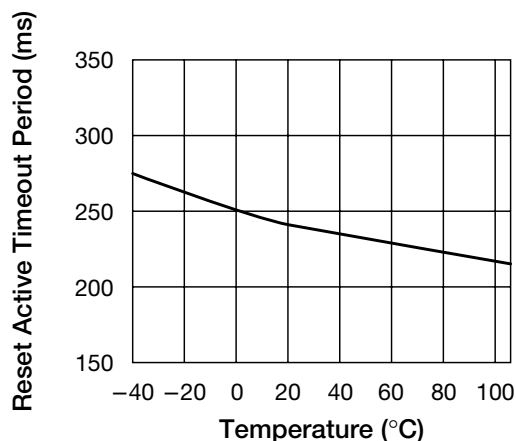
Test Circuit 7

Output leakage current vs temperature



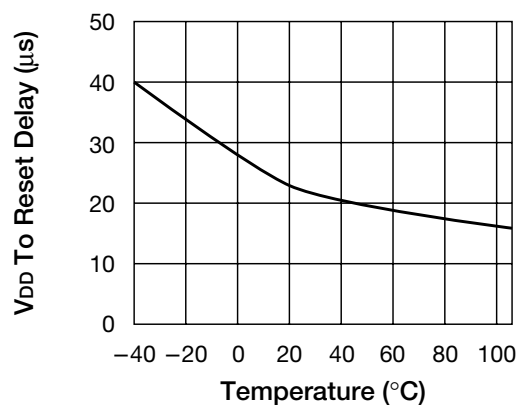
Test Circuit 5

Reset active timeout period vs temperature



Test Circuit 8

VDD to reset delay vs temperature

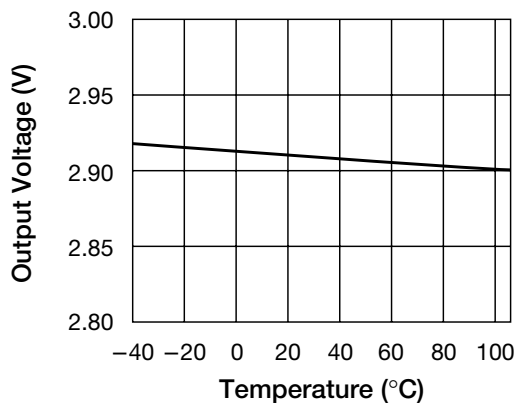


Test Circuit 8

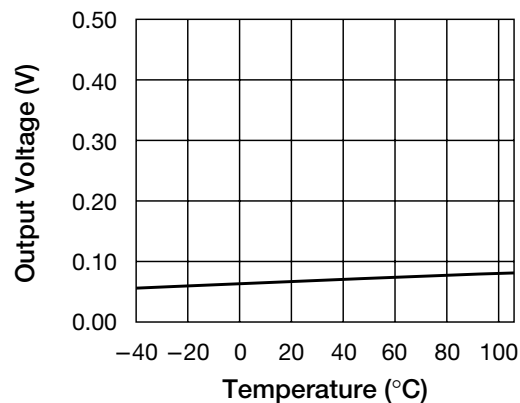
Note: These are typical characteristics.

Characteristics

- "H" Output voltage vs temperature (PST414A290N□)
 ■ "L" Output voltage vs temperature (PST414A290N□)

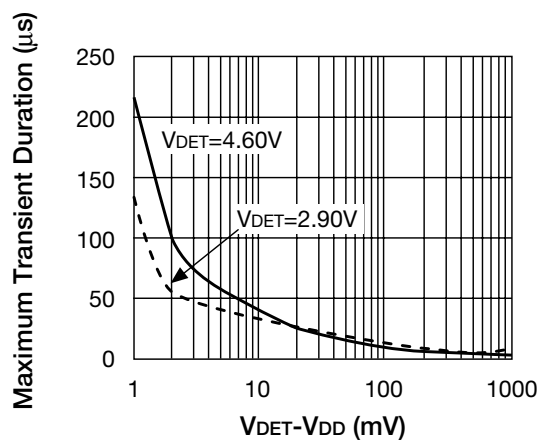


Test Circuit 6



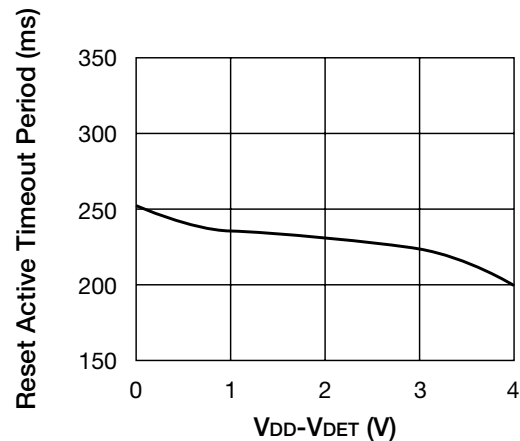
Test Circuit 7

- Maximum transient duration vs $V_{DET}-V_{DD}$



Test Circuit 8

- Reset active timeout period vs $V_{DD}-V_{DET}$ (PST414A290N□)



Test Circuit 8

Note: These are typical characteristics.