

**Description**

The GM71V(S)17800B/BL is the new generation dynamic RAM organized 2,097,152 words x 8 bit. GM71V(S)17800B/BL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V(S)17800B/BL offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71V(S)17800B/BL to be packaged in standard 400 mil 28pin plastic SOJ and standard 400mil 28pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply 3.3V ± 0.3V tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

**Features**

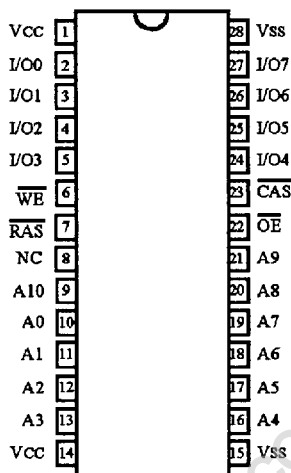
- 2,097,152 Words x 8 Bit Organization
- Fast Page Mode Capability
- Single Power Supply (3.3V ± 0.3V)
- Fast Access Time & Cycle Time (Unit: ns)

|                     | t <sub>TRAC</sub> | t <sub>CAC</sub> | t <sub>RC</sub> | t <sub>PC</sub> |
|---------------------|-------------------|------------------|-----------------|-----------------|
| GM71V(S)17800B/BL-6 | 60                | 15               | 110             | 40              |
| GM71V(S)17800B/BL-7 | 70                | 18               | 130             | 45              |
| GM71V(S)17800B/BL-8 | 80                | 20               | 150             | 50              |

- Low Power  
Active : 432/396/360mW (MAX)  
Standby : 3.6mW ( CMOS level : MAX)  
0.54mW ( L-version : MAX)
- $\overline{\text{RAS}}$  Only Refresh,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 2048 Refresh Cycles/32ms
- 2048 Refresh Cycles/128ms (L-version)
- Battery Back Up Operation (L-version)
- Self Refresh Operation (L-version)

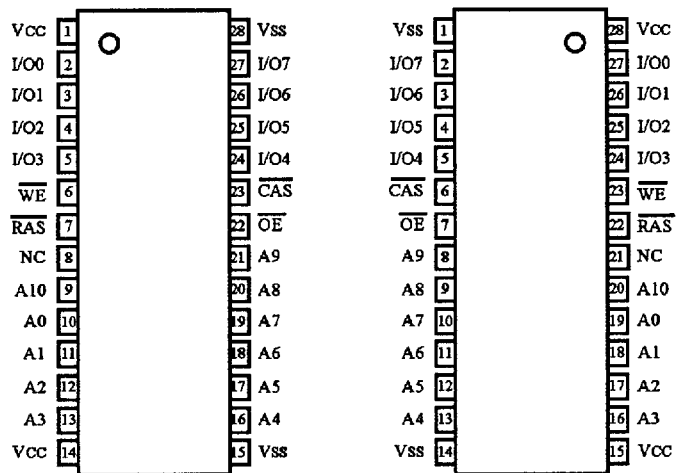
**Pin Configuration**

**28 SOJ**



(Top View)

**28 TSOP II**



(Normal)

(Reverse)

(Top View)

**Pin Description**

| Pin              | Function               | Pin             | Function      |
|------------------|------------------------|-----------------|---------------|
| A0-A10           | Address Inputs         | $\overline{WE}$ | Write Enable  |
| A0-A10           | Refresh Address Inputs | $\overline{OE}$ | Output Enable |
| I/O0-I/O7        | Data Input/Data Output | V <sub>cc</sub> | Power (+3.3V) |
| $\overline{RAS}$ | Row Address Strobe     | V <sub>ss</sub> | Ground        |
| $\overline{CAS}$ | Column Address Strobe  | NC              | No Connection |

**Ordering Information**

| Type No.  | Access Time          | Package  |
|---|----------------------|--|
| GM71V(S)17800BJ/BLJ-6<br>GM71V(S)17800BJ/BLJ-7<br>GM71V(S)17800BJ/BLJ-8 | 60ns<br>70ns<br>80ns | 400 Mil<br>28 Pin<br>Plastic SOJ                       |
| GM71V(S)17800BT/BLT-6<br>GM71V(S)17800BT/BLT-7<br>GM71V(S)17800BT/BLT-8 | 60ns<br>70ns<br>80ns | 400 Mil<br>28 Pin<br>Plastic TSOP II<br>(Normal Type)  |
| GM71V(S)17800BR/BLR-6<br>GM71V(S)17800BR/BLR-7<br>GM71V(S)17800BR/BLR-8 | 60ns<br>70ns<br>80ns | 400 Mil<br>28 Pin<br>Plastic TSOP II<br>(Reverse Type) |

**Absolute Maximum Ratings**

| Symbol           | Parameter                                      | Rating      | Unit |
|------------------|--|-------------|------|
| T <sub>OPR</sub> | Operating Temperature                          | 0 ~ +70     | °C   |
| T <sub>STG</sub> | Storage Temperature (Plastic)                  | -55 ~ +125  | °C   |
| V <sub>T</sub>   | Voltage on any Pin Relative to V <sub>ss</sub> | -0.5 ~ +4.6 | V    |
| V <sub>CC</sub>  | Supply Voltage Relative to V <sub>ss</sub>     | -0.5 ~ +4.6 | V    |
| I <sub>OUT</sub> | Short Circuit Output Current                   | 50          | mA   |
| P <sub>T</sub>   | Power Dissipation                              | 1.0         | W    |

**Recommended DC Operating Conditions (T<sub>A</sub> = 0 ~ +70°C)**

| Symbol          | Parameter          | Min  | Typ | Max                  | Unit |
|-----------------|--------------------|------|-----|----------------------|------|
| V <sub>CC</sub> | Supply Voltage     | 3.0  | 3.3 | 3.6                  | V    |
| V <sub>IH</sub> | Input High Voltage | 2.0  | -   | V <sub>CC</sub> +0.3 | V    |
| V <sub>IL</sub> | Input Low Voltage  | -0.3 | -   | 0.8                  | V    |

\*Note: All voltage referred to V<sub>ss</sub>.

**DC Electrical Characteristics** ( $V_{CC} = 3.3V \pm 0.3$ ,  $V_{SS} = 0V$ ,  $T_A = 0 \sim 70^\circ C$ )

| Symbol     | Parameter   | Min   | Max      | Unit    | Note |      |
|------------|---|-------|----------|---------|------|------|
| $V_{OH}$   | Output Level<br>Output "H" Level Voltage ( $I_{OUT} = -2mA$ )   | 2.4   | $V_{CC}$ | V       |      |      |
| $V_{OL}$   | Output Level<br>Output "L" Level Voltage ( $I_{OUT} = 2mA$ )  | 0     | 0.4      | V       |      |      |
| $I_{CC1}$  | Operating Current<br>Average Power Supply Operating Current<br>( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC} = t_{RC\ min}$ )              | 60 ns | -        | 120     | mA   | 1, 2 |
|            |   | 70 ns | -        | 110     |      |      |
|            |   | 80 ns | -        | 100     |      |      |
| $I_{CC2}$  | Standby Current (TTL)<br>Power Supply Standby Current<br>( $\overline{RAS}$ , $\overline{CAS} = V_{IH}$ , $D_{OUT} = High-Z$ )                      | -     | 2        | mA      |      |      |
| $I_{CC3}$  | $\overline{RAS}$ Only Refresh Current<br>Average Power Supply Current<br>$\overline{RAS}$ Only Refresh Mode<br>( $t_{RC} = t_{RC\ min}$ )           | 60 ns | -        | 120     | mA   | 2    |
|            |   | 70 ns | -        | 110     |      |      |
|            |   | 80 ns | -        | 100     |      |      |
| $I_{CC4}$  | Fast Page Mode Current<br>Average Power Supply Current<br>Fast Page Mode<br>( $t_{RC} = t_{RC\ min}$ )  | 60 ns | -        | 100     | mA   | 1, 3 |
|            |   | 70 ns | -        | 90      |      |      |
|            |   | 80 ns | -        | 85      |      |      |
| $I_{CC5}$  | Standby Current (CMOS)<br>Power Supply Standby Current<br>( $\overline{RAS}$ , $\overline{CAS} \geq V_{CC} - 0.2V$ , $D_{OUT} = High-Z$ )           | -     | 1        | mA      |      |      |
|            |   | -     | 150      | $\mu A$ | 5    |      |
| $I_{CC6}$  | $\overline{CAS}$ -before- $\overline{RAS}$ Refresh Current<br>( $t_{RC} = t_{RC\ min}$ )  | 60 ns | -        | 120     | mA   |      |
|            |   | 70 ns | -        | 110     |      |      |
|            |   | 80 ns | -        | 100     |      |      |
| $I_{CC7}$  | Standby Current $\overline{RAS} = V_{IH}$<br>$\overline{CAS} = V_{IL}$<br>$D_{OUT} = Enable$  | -     | 5        | mA      | 1    |      |
| $I_{CC8}$  | Battery Back Up Operating Current(C-MOS)<br>(Standby with CBR Refresh)<br>( $t_{RC} = 62.5 \mu s$ , $t_{RAS} \leq 0.3 \mu s$ , $D_{OUT} = High-Z$ ) | -     | 500      | $\mu A$ | 4,5  |      |
| $I_{CC9}$  | Self-Refresh Mode Current<br>( $\overline{RAS}$ , $\overline{CAS} \leq 0.2V$ , $D_{OUT} = High-Z$ )   | -     | 300      | $\mu A$ | 5    |      |
| $I_{L(O)}$ | Input Leakage Current<br>Any Input ( $0V \leq V_{IN} \leq 4.6V$ )   | -10   | 10       | $\mu A$ |      |      |
| $I_{L(O)}$ | Output Leakage Current<br>( $D_{OUT}$ is Disabled, $0V \leq V_{OUT} \leq 4.6V$ )  | -10   | 10       | $\mu A$ |      |      |

Note: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC(max)}$  is specified at the output open condition.

2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{CAS} = V_{IH}$ .

4.  $\overline{CAS} = L$  ( $\leq 0.2V$ ) while  $\overline{RAS} = L$  ( $\leq 0.2V$ ).

5. L-version.

**Capacitance** ( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = 25^\circ C$ )

| Symbol    | Parameter                        | Min | Max | Unit | Note |
|-----------|----------------------------------|-----|-----|------|------|
| $C_{I1}$  | Input Capacitance (Address)      | -   | 5   | pF   | 1    |
| $C_{I2}$  | Input Capacitance (Clocks)       | -   | 7   | pF   | 1    |
| $C_{I/O}$ | Output Capacitance (Data-In/Out) | -   | 7   | pF   | 1, 2 |

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2.  $CAS = V_{IH}$  to disable  $D_{OUT}$ .

**AC Characteristics** ( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_A = 0 \sim +70^\circ C$ ,  $V_{SS} = 0V$ , Note 1, 2, 18)

**Test Conditions**

Input level :  $V_{IL}=0V$ ,  $V_{IH}=3.0V$

Input rise and fall times: 2ns

Input timing reference levels:  $V_{IL}=0.8V$ ,  $V_{IH}=2.0V$

Output timing reference levels:  $V_{OL}=0.8V$ ,  $V_{OH}=2.0V$

Output load : 1 TTL gate +  $C_L$  (100pF)

(Including scope and jig)

**Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)**

| Symbol    | Parameter   | GM71V(S)17800<br>B/BL-6 |        | GM71V(S)17800<br>B/BL-7 |        | GM71V(S)17800<br>B/BL-8 |        | Unit | Note |
|-----------|---|-------------------------|--------|-------------------------|--------|-------------------------|--------|------|------|
|           |   | Min                     | Max    | Min                     | Max    | Min                     | Max    |      |      |
| $t_{RC}$  | Random Read or Write Cycle Time                     | 110                     | -      | 130                     | -      | 150                     | -      | ns   |      |
| $t_{RP}$  | $\overline{RAS}$ Precharge Time                     | 40                      | -      | 50                      | -      | 60                      | -      | ns   |      |
| $t_{CP}$  | $\overline{CAS}$ Precharge Time                     | 10                      | -      | 10                      | -      | 10                      | -      | ns   |      |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width                        | 60                      | 10,000 | 70                      | 10,000 | 80                      | 10,000 | ns   |      |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width                        | 15                      | 10,000 | 18                      | 10,000 | 20                      | 10,000 | ns   |      |
| $t_{ASR}$ | Row Address Set up Time                             | 0                       | -      | 0                       | -      | 0                       | -      | ns   |      |
| $t_{RAH}$ | Row Address Hold Time                               | 10                      | -      | 10                      | -      | 10                      | -      | ns   |      |
| $t_{ASC}$ | Column Address Set-up Time                          | 0                       | -      | 0                       | -      | 0                       | -      | ns   |      |
| $t_{CAH}$ | Column Address Hold Time                            | 10                      | -      | 15                      | -      | 15                      | -      | ns   |      |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time     | 20                      | 45     | 20                      | 52     | 20                      | 60     | ns   | 3    |
| $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time       | 15                      | 30     | 15                      | 35     | 15                      | 40     | ns   | 4    |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time                          | 15                      | -      | 18                      | -      | 20                      | -      | ns   |      |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time                          | 60                      | -      | 70                      | -      | 80                      | -      | ns   |      |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5                       | -      | 5                       | -      | 5                       | -      | ns   |      |
| $t_{ODD}$ | $\overline{OE}$ to $D_{IN}$ Delay Time              | 15                      | -      | 18                      | -      | 20                      | -      | ns   | 5    |
| $t_{DZO}$ | $\overline{OE}$ Delay Time from $D_{IN}$            | 0                       | -      | 0                       | -      | 0                       | -      | ns   | 6    |
| $t_{DZC}$ | $\overline{CAS}$ Delay Time from $D_{IN}$           | 0                       | -      | 0                       | -      | 0                       | -      | ns   | 6    |
| $t_T$     | Transition Time (Rise and Fall)                     | 3                       | 50     | 3                       | 50     | 3                       | 50     | ns   | 7    |
| $t_{REF}$ | Refresh Period                                      | -                       | 32     | -                       | 32     | -                       | 32     | ms   |      |
|           | Refresh Period (L-version)                          | -                       | 128    | -                       | 128    | -                       | 128    | ms   |      |

**Read Cycle**

| Symbol           | Parameter                                      | GM71V(S)17800<br>B/BL-6 |     | GM71V(S)17800<br>B/BL-7 |     | GM71V(S)17800<br>B/BL-8 |     | Unit | Note    |
|------------------|--|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|---------|
|                  |  | Min                     | Max | Min                     | Max | Min                     | Max |      |         |
| t <sub>RAC</sub> | Access Time from $\overline{RAS}$              | -                       | 60  | -                       | 70  | -                       | 80  | ns   | 8,9     |
| t <sub>CAC</sub> | Access Time from $\overline{CAS}$              | -                       | 15  | -                       | 18  | -                       | 20  | ns   | 9,10,17 |
| t <sub>AA</sub>  | Access Time from Address                       | -                       | 30  | -                       | 35  | -                       | 40  | ns   | 9,11,17 |
| t <sub>OAC</sub> | Access Time from $\overline{OE}$               | -                       | 15  | -                       | 18  | -                       | 20  | ns   | 9       |
| t <sub>RCS</sub> | Read Command Setup Time                        | 0                       | -   | 0                       | -   | 0                       | -   | ns   |         |
| t <sub>RCH</sub> | Read Command Hold Time to $\overline{CAS}$     | 0                       | -   | 0                       | -   | 0                       | -   | ns   | 12      |
| t <sub>RRH</sub> | Read Command Hold Time to $\overline{RAS}$     | 0                       | -   | 0                       | -   | 0                       | -   | ns   | 12      |
| t <sub>RAL</sub> | Column Address to $\overline{RAS}$ Lead Time   | 30                      | -   | 35                      | -   | 40                      | -   | ns   |         |
| t <sub>CAL</sub> | Column Address to $\overline{CAS}$ Lead Time   | 30                      | -   | 35                      | -   | 40                      | -   | ns   |         |
| t <sub>CLZ</sub> | $\overline{CAS}$ to Output in Low-Z            | 0                       | -   | 0                       | -   | 0                       | -   | ns   |         |
| t <sub>OH</sub>  | Output Data Hold Time                          | 3                       | -   | 3                       | -   | 3                       | -   | ns   |         |
| t <sub>OHO</sub> | Output Data Hold Time from $\overline{OE}$     | 3                       | -   | 3                       | -   | 3                       | -   | ns   |         |
| t <sub>OFF</sub> | Output Buffer Turn-off Time                    | -                       | 15  | -                       | 15  | -                       | 15  | ns   | 13      |
| t <sub>OEZ</sub> | Output Buffer Turn-off Time to $\overline{OE}$ | -                       | 15  | -                       | 15  | -                       | 15  | ns   | 13      |
| t <sub>CDD</sub> | $\overline{CAS}$ to D <sub>IN</sub> Delay Time | 15                      | -   | 18                      | -   | 20                      | -   | ns   | 5       |

**Write Cycle**

| Symbol           | Parameter                                   | GM71V(S)17800<br>B/BL-6 |     | GM71V(S)17800<br>B/BL-7 |     | GM71V(S)17800<br>B/BL-8 |     | Unit | Note |
|------------------|---|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|------|
|                  |   | Min                     | Max | Min                     | Max | Min                     | Max |      |      |
| t <sub>WCS</sub> | Write Command Setup Time                    | 0                       | -   | 0                       | -   | 0                       | -   | ns   | 14   |
| t <sub>WCH</sub> | Write Command Hold Time                     | 10                      | -   | 15                      | -   | 15                      | -   | ns   |      |
| t <sub>WP</sub>  | Write Command Pulse Width                   | 10                      | -   | 10                      | -   | 10                      | -   | ns   |      |
| t <sub>RWL</sub> | Write Command to $\overline{RAS}$ Lead Time | 15                      | -   | 18                      | -   | 20                      | -   | ns   |      |
| t <sub>CWL</sub> | Write Command to $\overline{CAS}$ Lead Time | 15                      | -   | 18                      | -   | 20                      | -   | ns   |      |
| t <sub>DS</sub>  | Data-in Setup Time                          | 0                       | -   | 0                       | -   | 0                       | -   | ns   | 15   |
| t <sub>DH</sub>  | Data-in Hold Time                           | 10                      | -   | 15                      | -   | 15                      | -   | ns   | 15   |

### Read-Modify-Write Cycle

| Symbol           | Parameter  | GM71V(S)17800<br>B/BL-6 |     | GM71V(S)17800<br>B/BL-7 |     | GM71V(S)17800<br>B/BL-8 |     | Unit | Note |
|------------------|--|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|------|
|                  |  | Min                     | Max | Min                     | Max | Min                     | Max |      |      |
| t <sub>RWC</sub> | Read-Modify-Write Cycle Time                                 | 155                     | -   | 181                     | -   | 205                     | -   | ns   |      |
| t <sub>RWD</sub> | $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time | 85                      | -   | 98                      | -   | 110                     | -   | ns   | 14   |
| t <sub>CWD</sub> | $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time | 40                      | -   | 46                      | -   | 50                      | -   | ns   | 14   |
| t <sub>AWD</sub> | Column Address to $\overline{\text{WE}}$ Delay Time          | 55                      | -   | 63                      | -   | 70                      | -   | ns   | 14   |
| t <sub>OEH</sub> | $\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$ | 15                      | -   | 18                      | -   | 20                      | -   | ns   |      |

### Refresh Cycle

| Symbol           | Parameter   | GM71V(S)17800<br>B/BL-6 |     | GM71V(S)17800<br>B/BL-7 |     | GM71V(S)17800<br>B/BL-8 |     | Unit | Note |
|------------------|---|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|------|
|                  |   | Min                     | Max | Min                     | Max | Min                     | Max |      |      |
| t <sub>CSR</sub> | $\overline{\text{CAS}}$ Setup Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle) | 5                       | -   | 5                       | -   | 5                       | -   | ns   |      |
| t <sub>CHR</sub> | $\overline{\text{CAS}}$ Hold Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)  | 10                      | -   | 10                      | -   | 10                      | -   | ns   |      |
| t <sub>WRP</sub> | $\overline{\text{WE}}$ Setup Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)  | 0                       | -   | 0                       | -   | 0                       | -   | ns   |      |
| t <sub>WRH</sub> | $\overline{\text{WE}}$ Hold Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)   | 10                      | -   | 10                      | -   | 10                      | -   | ns   |      |
| t <sub>RPC</sub> | $\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time  | 0                       | -   | 0                       | -   | 0                       | -   | ns   |      |

### Fast Page Mode Cycle

| Symbol            | Parameter  | GM71V(S)17800<br>B/BL-6 |         | GM71V(S)17800<br>B/BL-7 |         | GM71V(S)17800<br>B/BL-8 |         | Unit | Note |
|-------------------|--|-------------------------|---------|-------------------------|---------|-------------------------|---------|------|------|
|                   |  | Min                     | Max     | Min                     | Max     | Min                     | Max     |      |      |
| t <sub>PC</sub>   | Fast Page Mode Cycle Time  | 40                      | -       | 45                      | -       | 50                      | -       | ns   |      |
| t <sub>RASP</sub> | Fast Page Mode $\overline{\text{RAS}}$ Pulse Width                       | -                       | 100,000 | -                       | 100,000 | -                       | 100,000 | ns   | 16   |
| t <sub>ACP</sub>  | Access Time from $\overline{\text{CAS}}$ Precharge                       | -                       | 35      | -                       | 40      | -                       | 45      | ns   | 9,17 |
| t <sub>RHCP</sub> | $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | 35                      | -       | 40                      | -       | 45                      | -       | ns   |      |

**Fast Page Mode Read-Modify-Write Cycle**

| Symbol            | Parameter  | GM71V(S)17800<br>B/BL-6 |     | GM71V(S)17800<br>B/BL-7 |     | GM71V(S)17800<br>B/BL-8 |     | Unit | Note |
|-------------------|--|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|------|
|                   |  | Min                     | Max | Min                     | Max | Min                     | Max |      |      |
| t <sub>PRWC</sub> | Fast Page Mode Read-Modify-Write Cycle Time                              | 85                      | -   | 96                      | -   | 105                     | -   | ns   |      |
| t <sub>CPW</sub>  | $\overline{\text{WE}}$ Delay Time from $\overline{\text{CAS}}$ Precharge | 60                      | -   | 68                      | -   | 75                      | -   | ns   | 14   |

**Self Refresh Mode(L-version)**

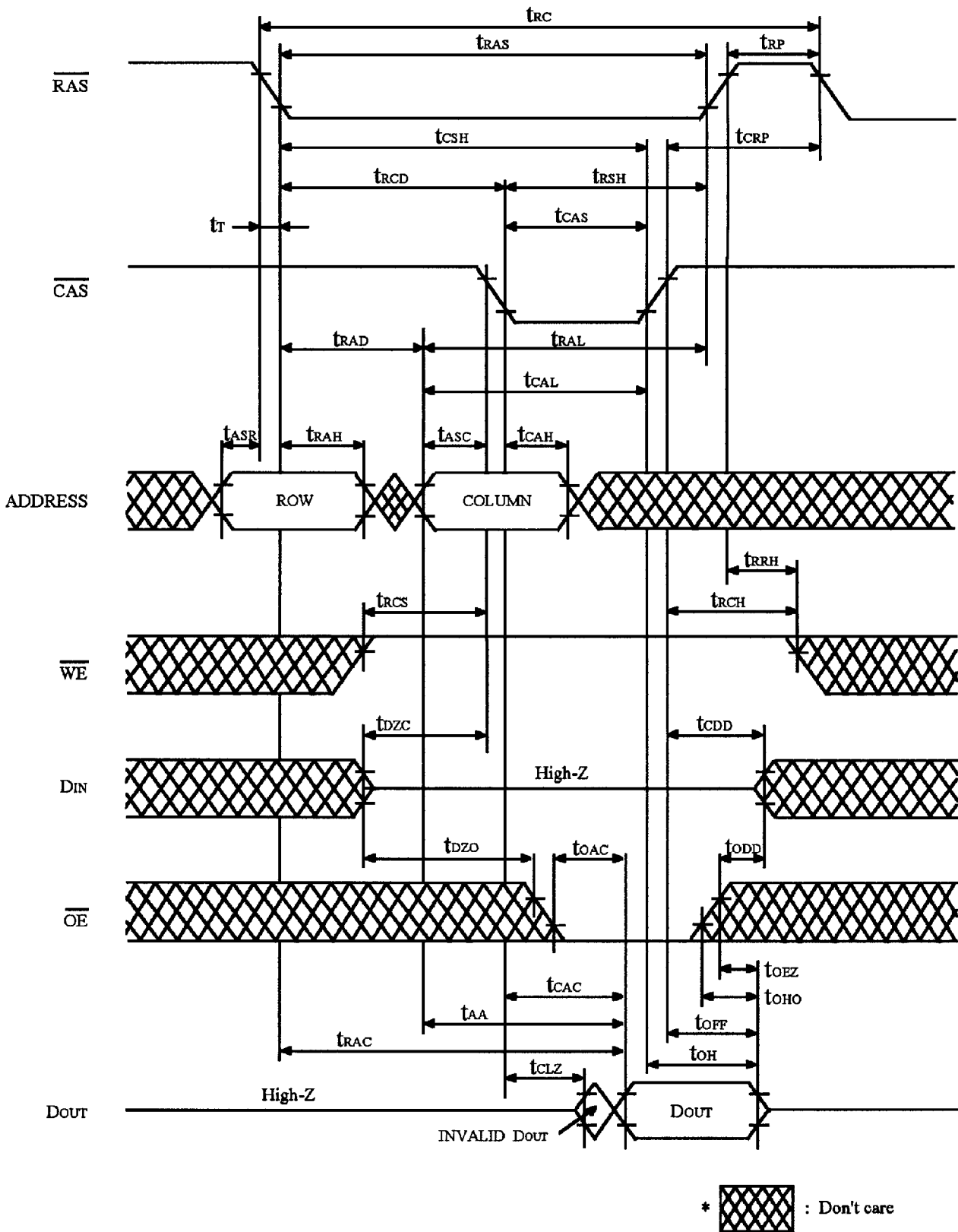
| Symbol            | Parameter   | GM71VS17800<br>BL-6 |     | GM71VS17800<br>BL-7 |     | GM71VS17800<br>BL-8 |     | Unit          | Note |
|-------------------|---|---------------------|-----|---------------------|-----|---------------------|-----|---------------|------|
|                   |   | Min                 | Max | Min                 | Max | Min                 | Max |               |      |
| t <sub>RASS</sub> | $\overline{\text{RAS}}$ Pulse Width (Self-Refresh)    | 100                 | -   | 100                 | -   | 100                 | -   | $\mu\text{s}$ |      |
| t <sub>RPS</sub>  | $\overline{\text{RAS}}$ Precharge Time (Self-Refresh) | 110                 | -   | 130                 | -   | 150                 | -   | ns            |      |
| t <sub>CHS</sub>  | $\overline{\text{CAS}}$ Hold Time (Self-Refresh)      | -50                 | -   | -50                 | -   | -50                 | -   | ns            |      |

**Notes:**

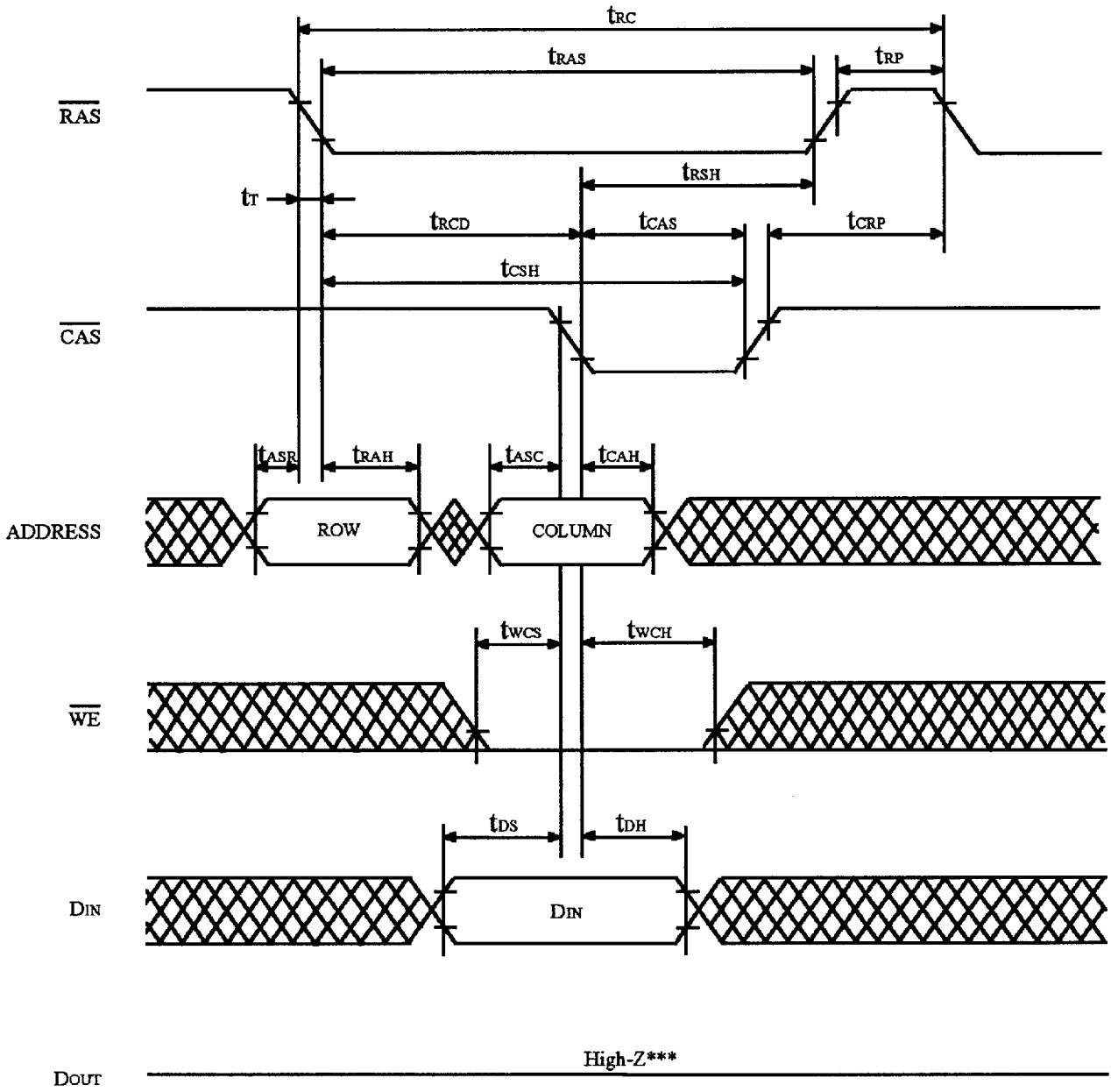
1. AC Measurements assume  $t_r = 5\text{ ns}$ .
2. An initial pause of  $200\ \mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles are required.
3. Operation with the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
4. Operation with the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
5. Either  $t_{\text{ODD}}$  or  $t_{\text{CDD}}$  must be satisfied.
6. Either  $t_{\text{DZO}}$  or  $t_{\text{DZC}}$  must be satisfied.
7.  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$ .
8. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
9. Measured with a load circuit equivalent to 1TTL loads and  $100\text{pF}$ . ( $V_{\text{OH}}=2.0\text{V}$ ,  $V_{\text{OL}}=0.8\text{V}$ )
10. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ .
11. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ .
12. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
13.  $t_{\text{OFF}}(\text{max})$  and  $t_{\text{OEZ}}(\text{max})$  define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$  and  $t_{\text{AWD}}$  and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ , and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$  or  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , and  $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to  $\overline{\text{CAS}}$  leading edge in early write cycle and to  $\overline{\text{WE}}$  leading edge in a delayed write or a read modify write cycle.
16.  $t_{\text{RASP}}$  defines  $\overline{\text{RAS}}$  pulse width in fast page mode cycles.
17. Access time is determined by the longer of  $t_{\text{AA}}$  or  $t_{\text{CAC}}$  or  $t_{\text{ACP}}$ .
18. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device. After  $\overline{\text{RAS}}$  is reset, if  $t_{\text{OEH}} \geq t_{\text{CWL}}$ , the I/O pin will remain open circuit (high impedance); if  $t_{\text{OEH}} \leq t_{\text{CWL}}$ , invalid data will be out at each I/O.



**Timing Waveforms**



**FIGURE 1. READ CYCLE**




- \*  : Don't care
- \*\*  $\overline{OE}$  : Don't care
- \*\*\*  $t_{wcs} \geq t_{wcs}(\text{min})$

FIGURE 2. EARLY WRITE CYCLE

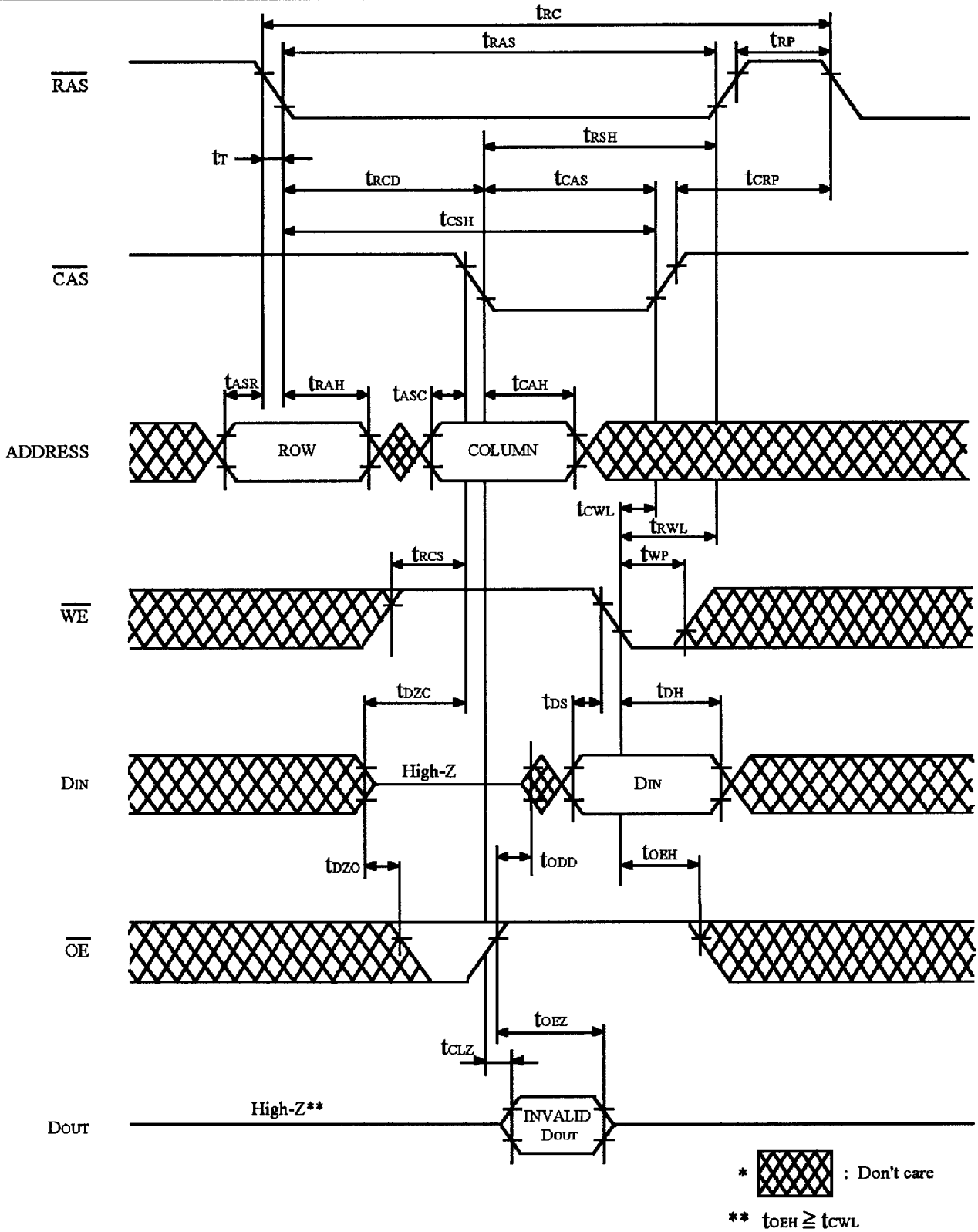
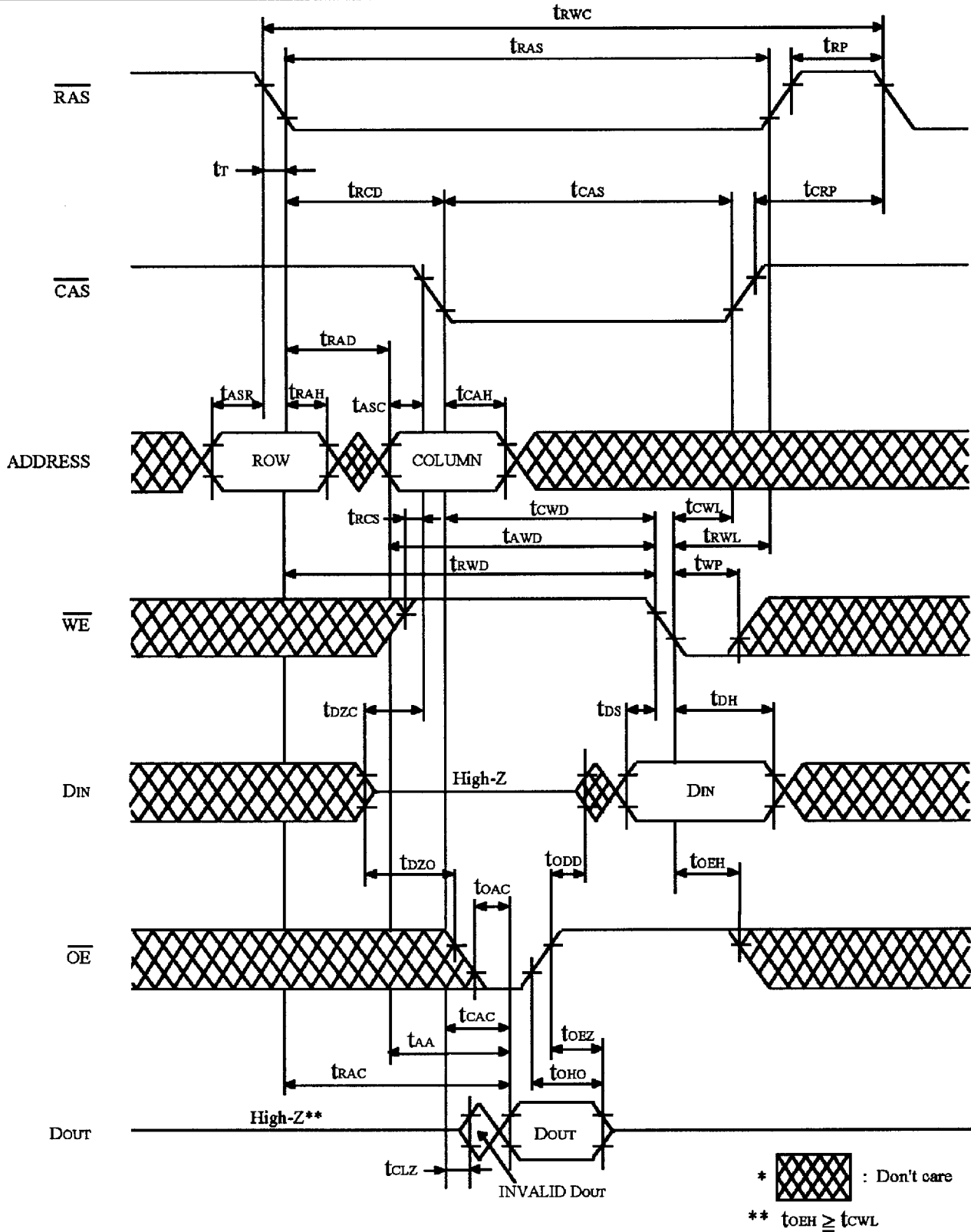
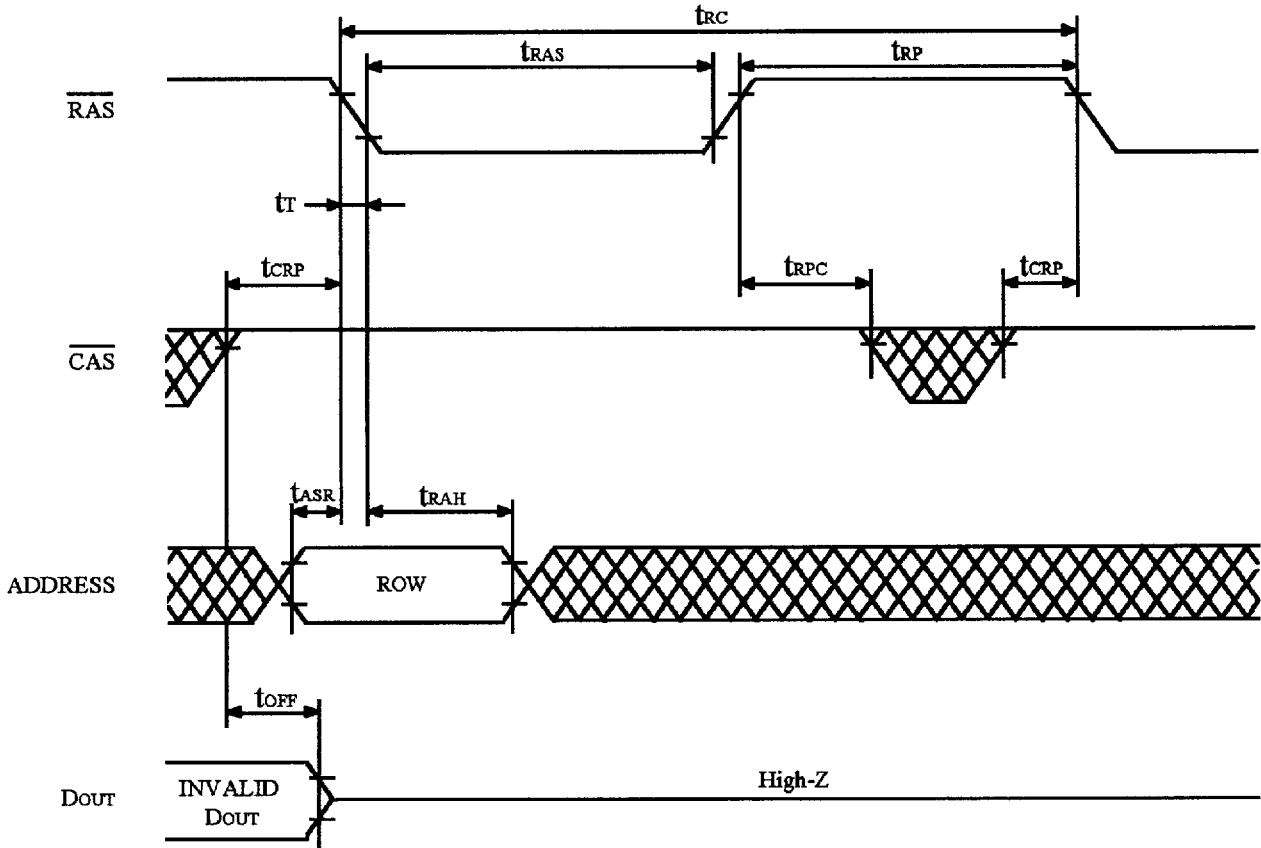


FIGURE 3. DELAYED WRITE CYCLE <sup>+18</sup>



**FIGURE 4. READ MODIFY WRITE CYCLE<sup>\*18</sup>**



\*  : Don't care

\*\*  $\overline{\text{OE}}, \overline{\text{WE}}$  : Don't care

\*\*\* Refresh Address :  
A0 - A10 (RA0 - RA10)

**FIGURE 5.  $\overline{\text{RAS}}$  ONLY REFRESH CYCLE**

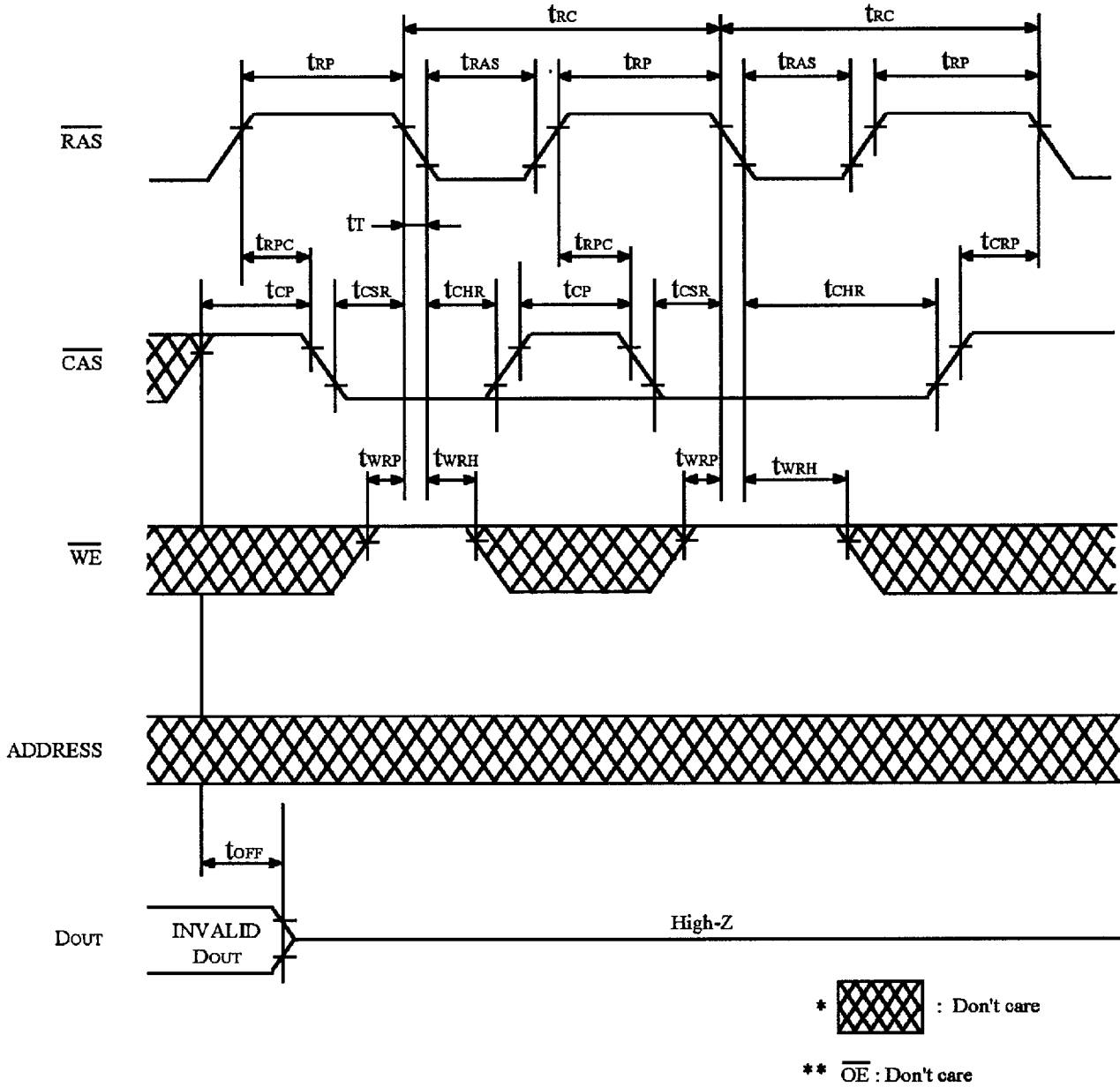
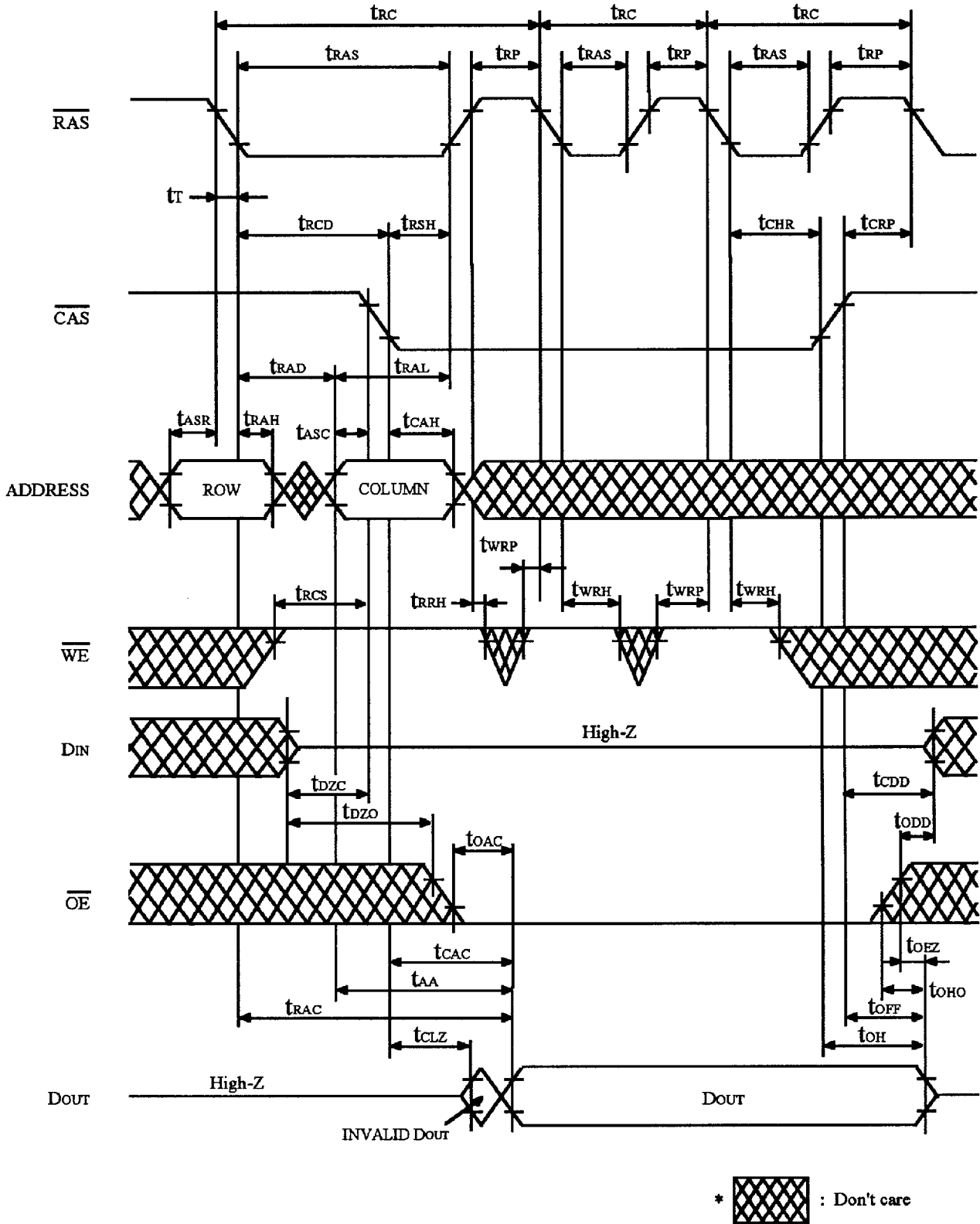


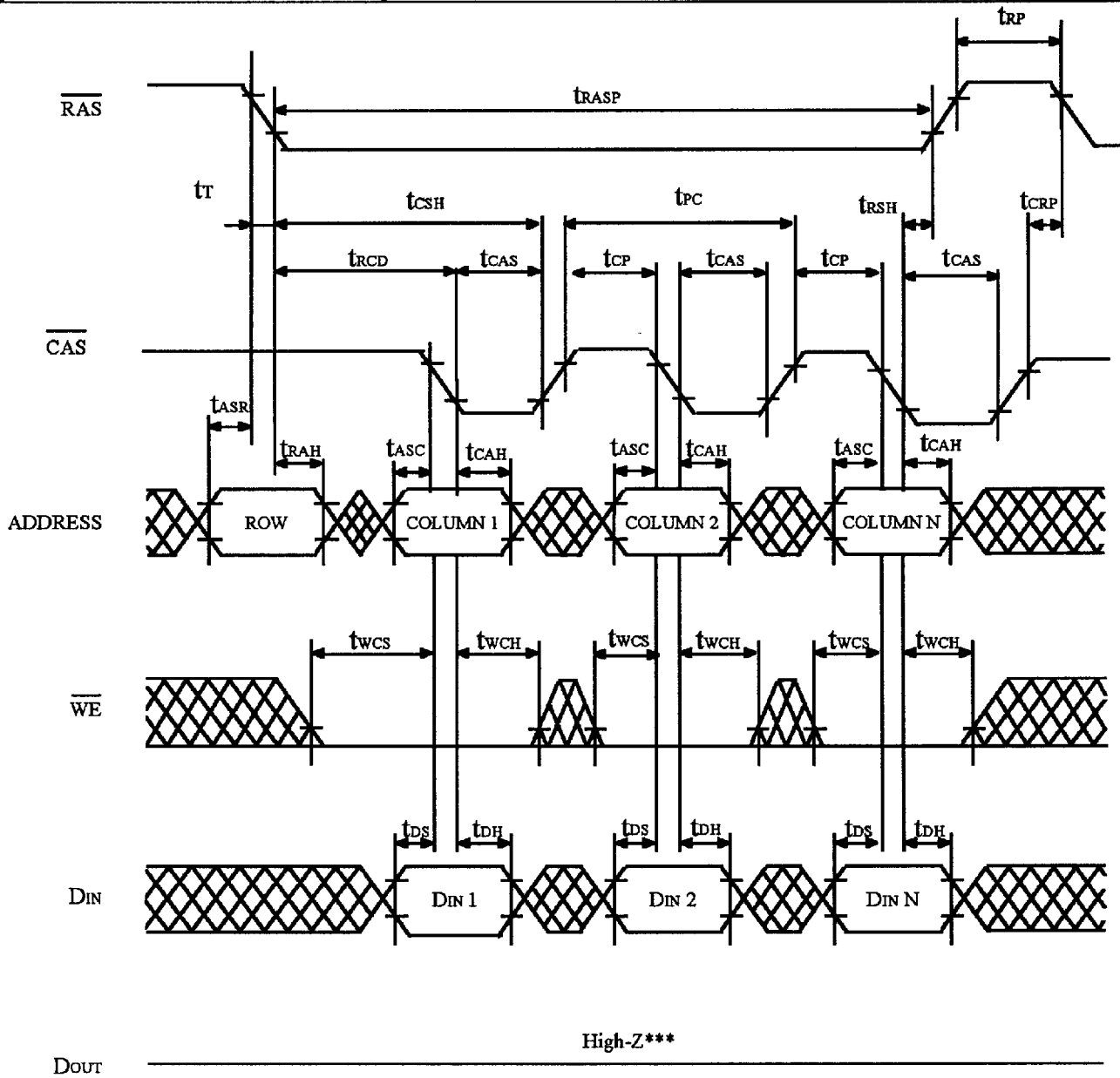
FIGURE 6.  $\overline{CAS}$  BEFORE  $\overline{RAS}$  REFRESH CYCLE




**FIGURE 7. HIDDEN REFRESH CYCLE**

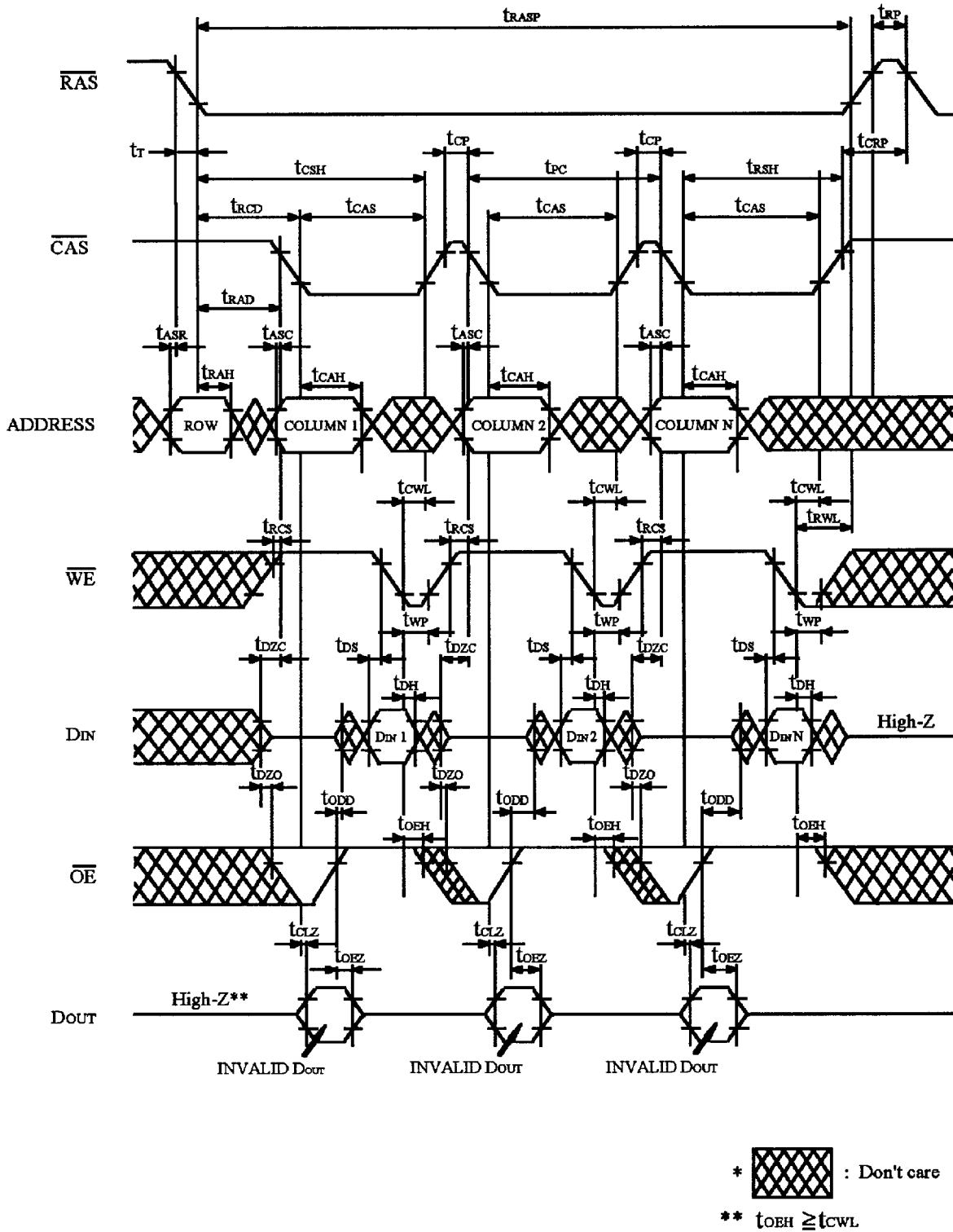






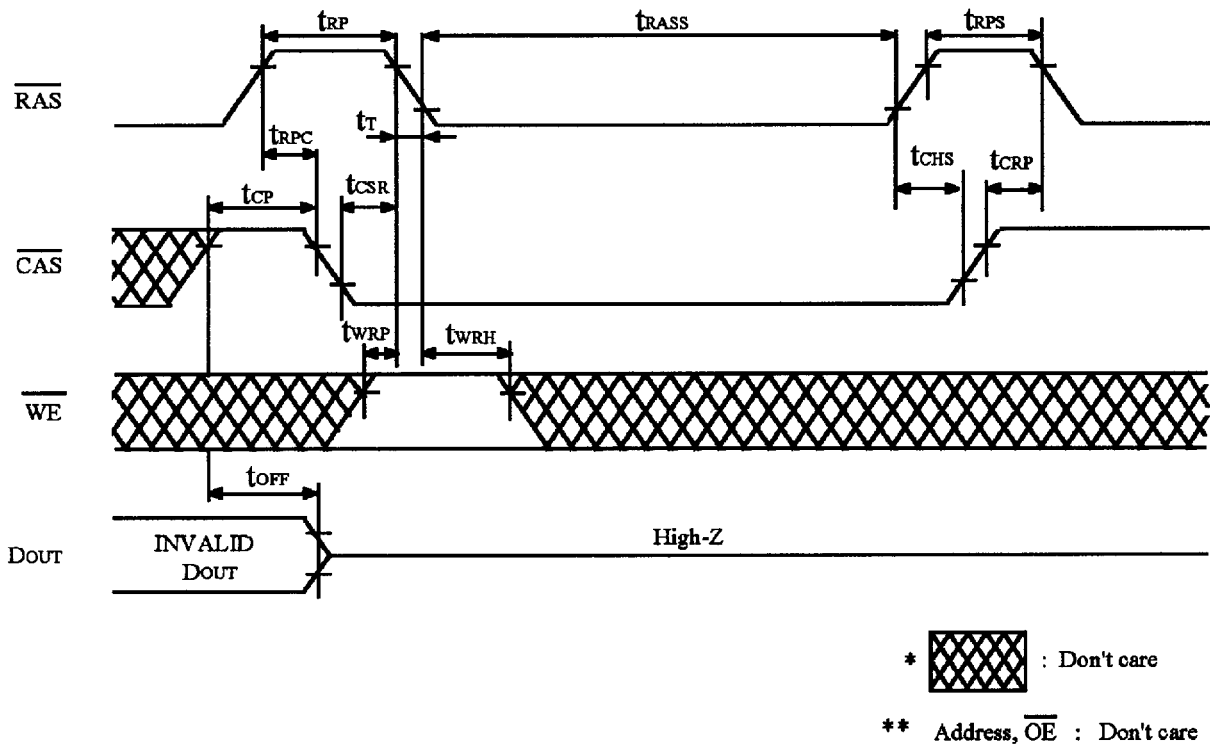
- \*  : Don't care
- \*\*  $\overline{OE}$  : Don't care
- \*\*\*  $t_{wcs} \geq t_{wcs}(\text{min})$

**FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE**



**FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE<sup>\*18</sup>**





The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

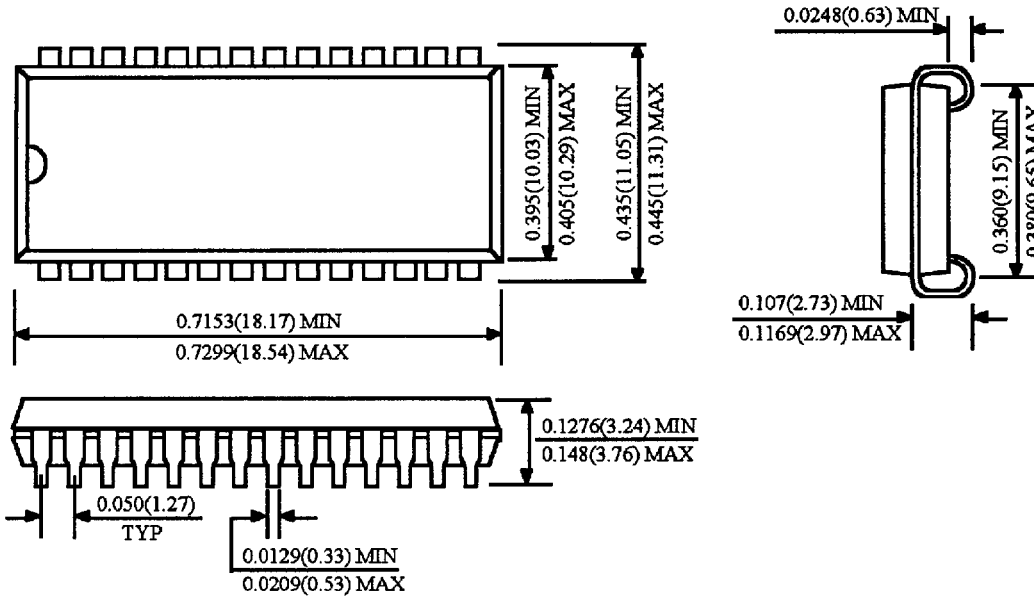
1. Please do not use  $t_{TRASS}$  timing,  $10\mu\text{s} \leq t_{TRASS} \leq 100\mu\text{s}$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{TRASS} \geq 100\mu\text{s}$ , then  $\overline{\text{RAS}}$  precharge time should use  $t_{RPS}$  instead of  $t_{RP}$ .
2. If you use  $\overline{\text{RAS}}$  only refresh or CBR burst refresh mode in normal read/write cycle, 2048 cycles of distributed CBR refresh with  $15.6\mu\text{s}$  interval should be executed within 32ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with  $15.6\mu\text{s}$  interval in normal read/write cycle, CBR refresh should be executed within  $15.6\mu\text{s}$  immediately after exiting from and before entering into the self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

FIGURE 12. SELF REFRESH CYCLE

**Package Dimensions**

Unit: Inches (mm)

**28 SOJ**



**28 TSOP II**

