CX20470

CDMA Baseband Analog Processor

The CX20470 is a dual-mode Baseband Analog Processor (BAP) for use in Code Division Multiple Access (CDMA) and Frequency Modulated (FM) portable telephones. The device is designed to interface between the RF section and the digital processing circuitry of the telephone. The CX20470 CDMA BAP includes all of the circuitry needed to support baseband signal processing and conversions between analog and digital signals in a dual mode CDMA and FM phone.

The receive section accepts analog baseband in-phase (I) and quadrature-phase (Q) signals, performs channel selection lowpass filtering, and converts the analog baseband signals into digital signals. The transmit section function provides the reverse conversions for digital input signals. In addition, the transmit section also accepts differential analog I and Q signals from baseband.

The CX20470 CDMA BAP also includes digital and Phase Locked Loop (PLL) clock synthesis for 19.2 MHz, 19.68 MHz, and 19.8 MHz system clocks, general purpose Analog-to-Digital (A/D) conversions for battery and signal strength monitoring, and two PLL synthesizers

The CX20470 CDMA BAP integrates an audio Coder/Decoder (CODEC) that provides signal translation between an analog voice band signal and a Pulse Code Modulation (PCM) digital signal. The CODEC is designed to perform the transmit encoding A/D conversion, together with transmit and receive filtering, for voice-band communication systems. The CODEC's audio interface consists of 3 microphone inputs, 3 audio speaker outputs, and DTMF/tone(s)/ring/side tone generation. The CODEC operation and configuration registers can be programmed by a microcontroller via an Inter-Integrated Circuit (I2C) compatible or 3-wire bus interface at any time. The CODEC also integrates the microphone amplifier and speaker post amplifier on-chip. The post amplifier is capable of driving a 32 Ω load directly.

The device is available in 100-pin μBGA and 56-pin Land Grid Array (LGA) packages:

- 100-pin μBGA – CDMA, FM, dual VHF synthesizers, 7-input monitor ADC, audio CODEC
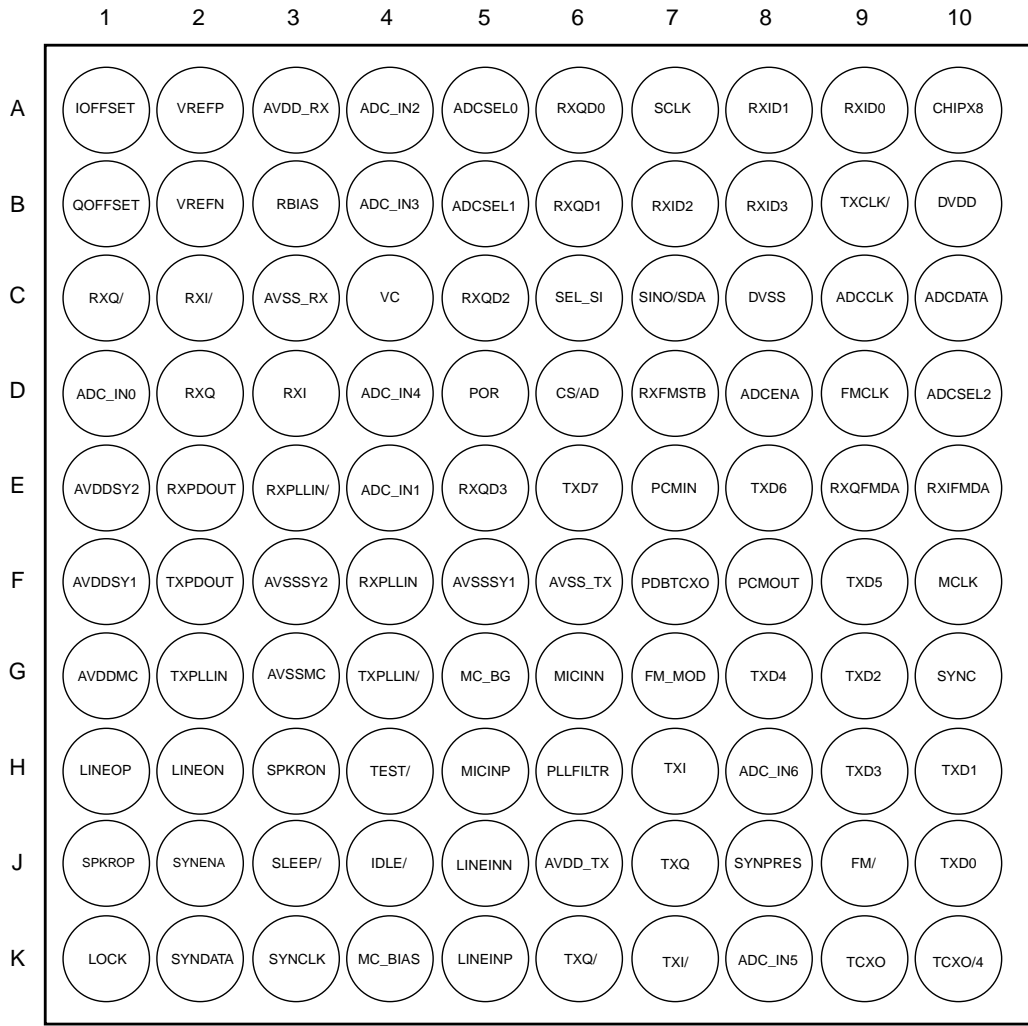- 56-pin LGA – CDMA, single VHF synthesizer, 2-input monitor ADC.

The device package pinout for each of these are shown in Figures 1 and 2. A general block diagram of the CX20470 BAP is shown in Figure 3.

Distinguishing Features

- Dual mode for CDMA and FM operation.
- Receive signal path includes:
  – Separate CDMA, and FM filters and ADCs
  – Offset control loop
- Transmit signal path includes:
  – Configurable input interface to either digital or analog I/Q signals from the baseband modem
  – Selectable conversion of digital I-Q data to analog signals
  – Separate CDMA filters and FM filters
- Two VHF PLL synthesizers:
  – Programmable charge pump current
  – Lock detector output
  – Operate in concert with CDMA mode operation
- System clock generation and support includes:
  – 19.2/19/68/19.8 MHz system clock support
  – External CHIPx8 clocks (input to BAP)
  – TCXO/4 and CHIPx8 clocks powerdown capability
- Audio CODEC includes:
  – 14-bit linear CODEC with on-chip filters meet ITU-T G.712 requirements
  – Switchable 3 microphone inputs with pre-amplifier gain control from –4 to 40 dB in 2 dB steps
  – Switchable 3 speaker outputs with programmable post-amplifiers from 0 to –30 dB in 2 dB steps, and capable of driving 32 Ω load directly.
  – Programmable frequency and gain for DTMF/Tone(s)/Ring/Sidetone generation
  – Separate ringer output with gain control
- 8-bit general purpose ADC with 7 input channels
- Independent mode and operation controls for BAP and CODEC functions
- Low power consumption in all operation modes
- Baseband modem interface compatibility includes:
  – MSM2300/MSM3000
  – MSM3100
- Single supply voltage from 2.7 V to 3.6 V
- Operating temperature of –40 °C to +85
- Package options include:
  – 100-pin μBGA
  – 56-pin LGA

Applications

- Cellular and Advanced Mobile Phone System (AMPS) band phones
- Dual band PCS/cellular CDMA
- Dual mode/dual band

	1	2	3	4	5	6	7	8	9	10
A	IOFFSET	VREFP	AVDD_RX	ADC_IN2	ADCSEL0	RXQD0	SCLK	RXID1	RXID0	CHIPX8
B	QOFFSET	VREFN	RBIAS	ADC_IN3	ADCSEL1	RXQD1	RXID2	RXID3	TXCLK/	DVDD
C	RXQ/	RXI/	AVSS_RX	VC	RXQD2	SEL_SI	SINO/SDA	DVSS	ADCCLK	ADCDATA
D	ADC_IN0	RXQ	RXI	ADC_IN4	POR	CS/AD	RXFMSTB	ADCENA	FMCLK	ADCSEL2
E	AVDDSY2	RXPDOUT	RXPLLIN/	ADC_IN1	RXQD3	TXD7	PCMIN	TXD6	RXQFMDA	RXIFMDA
F	AVDDSY1	TXPDOUT	AVSSSY2	RXPLLIN	AVSSSY1	AVSS_TX	PDBTCXO	PCMOUT	TXD5	MCLK
G	AVDDMC	TXPLLIN	AVSSMC	TXPLLIN/	MC_BG	MICINN	FM_MOD	TXD4	TXD2	SYNC
H	LINEOP	LINEON	SPKRON	TEST/	MICINP	PLLFILTR	TXI	ADC_IN6	TXD3	TXD1
J	SPKROP	SYNENA	SLEEP/	IDLE/	LINEINN	AVDD_TX	TXQ	SYNPRES	FM/	TXD0
K	LOCK	SYNDATA	SYNCLK	MC_BIAS	LINEINP	TXQ/	TXI/	ADC_IN5	TCXO	TCXO/4

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Figure 1. CX20470 BAP Pinout – 100-Pin μBGA Package

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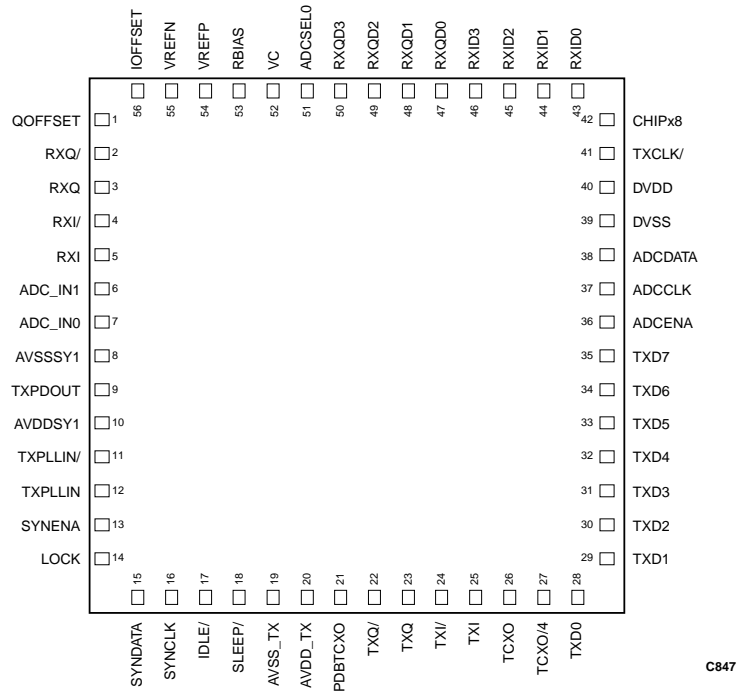Proprietary Information and Specifications are Subject to Change

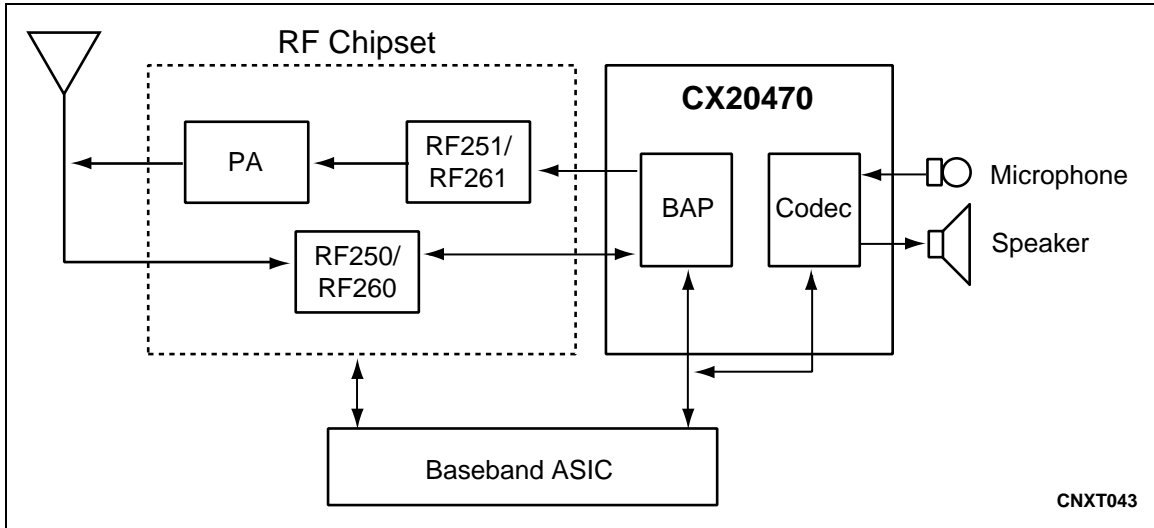Figure 2. CX20470 BAP Pinout – 56-Pin LGA Package

Figure 3. CX20470 General Block Diagram

Technical Description

The CX20470 consists of a CDMA transmit and receive path, FM transmit and receive path, Intermediate Frequency (IF) PLL synthesizer section, an auxiliary control section, and an audio CODEC section. Each of these functional sections is detailed in the complete CX20470 system block diagram shown in Figure 4.

CDMA Transmit Path

The CDMA transfer signal path accepts two different interface formats from the baseband ASIC: analog signal and digital data. The interface format configuration can be controlled through BAP control register.

For analog signal interface, the BAP accepts I and Q analog transmit signals from the digital modem and performs transmit low-pass filters with a bandwidth of 1 MHz for image rejection. The I and Q filtered signals are then output to the transmitter.

For digital signal interface, the BAP transmit signal path accepts digital I and Q data baseband signals form the baseband modem and outputs analog I and Q components to the IF transmitter. Eight bits of I and Q transmit data are input to the CDMA Digital-to-Analog Converters (DACs) by multiplexing over and 8-bit input port on the BAP.

At the falling edge of the transmit clock input (TxCLK/), the 8-bit parallel transmit data is registered into I DAC, and, at the rising edge, registered into Q DAC. The outputs from I DAC and Q DAC are followed by transmit low-pass reconstruction filters with a bandwidth of 630 kHz for removal of unwanted frequency components. The precise I and Q signals are output to the transmitter.

CDMA Receive Path

The BAP receive path is designed to accept I and Q baseband analog components. These signals are input into lowpass filters specifically designed for CDMA. These filters, when combined with the external IF bandpass filtering, provide the necessary receiver passband, rejection band amplitude, and phase response.

The control of DC offset is made to the I and Q signals from the inputs IOFFSET and QOFFSET. Analog voltages at these inputs adjust the offset before the A/D conversion. Two identical 4-bit flash ADCs sample the I and Q signals at a rate of 9.8304 MHz (CHIPx8) and output the four bits each in parallel to a baseband device.

FM Transmit Path

The FM transmit signal path accepts two different interface formats from the baseband ASIC: analog signal and digital data. The interface format configuration can be controlled through BAP control register.

For the analog signal interface, the BAP accepts I and Q analog signals from the digital modem and perform transmit low-pass

filters. The I and Q transmit filters are then output to the transmitter.

For the digital signal interface, the FM modulation signal is created from an 8-bit DAC, which is the Q signal DAC re-used from the CDMA section. The DAC rate is determined from the transmit clock input (TXCLK/) and the digital input is 8-bit parallel. The DAC analog output is the analog output FM modulation signal used to directly control a transmit VCO using external components.

FM Receive Path

The receive path for FM operation is similar to that for CDMA operation. The differences are that the receive path uses 15 kHz bandwidth low-pass filters and provides 8-bit serial output ADCs. These ADCs sample the analog I and Q signals at a rate determined by the strobe (RXFMSTB). The digital data is output serially and determined by the FMCLK beginning with the Most Significant Bit (MSB) of the result.

IF PLL Synthesizer Section

Two identical and independent PLL synthesizers are provided to synthesize the transmit and receive IF frequencies. Each contains a dual modulus divide by 16/17 prescaler, a 13-bit R counter, a 17-bit N counter, a phase detector, and a charge pump current and lock detector configuration. The synthesizers accept differential VCO inputs up to 640 MHz and a shared TCXO reference input.

CDMA Auxiliary Section

The auxiliary section of the CDMA BAP includes mode control logic, a general purpose ADC, and clock generation.

Mode Control Logic. The BAP has several operating modes, each one selected by one of three digital inputs: FM, IDLE, and SLEEP.

- CDMA RxTx or FM RxTx mode: When a call is in progress.
- IDLE mode: When a call is not in progress but the telephone is ready to answer a call.
- SLEEP mode (low-power mode): Calls cannot be received but the digital processor and keypad are enabled.
- CDMA slotted paging mode: IDLE mode only for paging slot, other time SLEEP mode.
- Power-down mode: Device is in standby mode (leakage current consumption only).

General Purpose ADC. The BAP provides an 8-bit resolution ADC that can be applied to monitor battery level, temperature, and/or sensors.

Clock Generation. The CDMA BAP provides a digital and/or PLL clock synthesis network to generate TCXO/4 and CHIPx8 signals from a 19.2 MHz, 19.68 MHz, or 19.8 MHz system clock. The clock generation configuration can be programmed via the synthesizer's three-wire serial interface.

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Audio CODEC Section

The CODEC serves as an interface between a voice device and a digital processor system. The CODEC provides a bi-directional interface between voice/audio and a digital system processor. It receives audio signals from sources such as microphones, digitizes the signals, and outputs them to a host processing system. The CODEC receives digital signals from the digital processing system (MSM ASIC or equivalent), converts the signal to analog, and outputs the signal to a device such as an earpiece or a speaker.

As shown in Figure 5, CODEC operations can be divided into four groups: transmit (ADC) channel, receive (DAC) channel, timing and control, and power control.

CODEC Transmit Section. The transmit section is designed to interface directly with a microphone and/or an external audio source at the same time. The microphone input or external source signal can be selected as the audio input signal.

The input signal is buffered and amplified with a provision to set the amplifier gain to accommodate a range of signal input levels. The amplified signal is then anti-aliased and bandpass filtered and applied to the input of a 14-bit linear A/D converter. The digital converted data is then clocked out as a serial data stream (PCMOUT) to the digital system processor.

CODEC Receive Section. The receive section collects a frame of serial data on the PCMIN and converts it to the analog signal through a linear D/A converter. The analog converted signal is then lowpass filtered to provide out-of-band rejection and smoothing. The filtered signal is sent to the speaker or the line driver amplifier. Both amplifiers have a differential output with adjustable gain control.

CODEC Configuration and Control Interface Section. CODEC operation mode and configuration control registers can be easily programmed directly from a digital system processor through an I²C -bus compatible or three-wire serial bus interface. The serial interface types are pin-selectable between 3-wire bus or I²C-bus interface.

Electrical and Mechanical Specifications

Signal pin assignments and functional pin descriptions are described in Table 1 (100-pin μBGA) and Table 2 (56-pin LGA). The absolute maximum ratings of the CX20470 are provided in Table 3. The recommended operating conditions are specified in Table 4. Electrical specifications are provided in Table 5.

Tables 6 through 9 specify input and output signal levels and electrical characteristics. A system block diagram is provided in Figure 4 and an audio CODEC block diagram is presented in Figure 5.

Package dimensions for the CX20470 are shown in Figure 6 (100-pin μBGA) and Figure 7 (56-pin LGA).

Electrostatic Discharge (ESD) Sensitivity

The CX20470 is a Class 1 device. The following ESD precautions are required:

- Protective outer garments.
- Handle device in ESD safeguarded work area.
- Transport device in ESD shielded containers.
- Monitor and test all ESD protection equipment.

Treat the CX20470 BAP as extremely sensitive to ESD since ESD sensitivity has not yet been determined for this device.
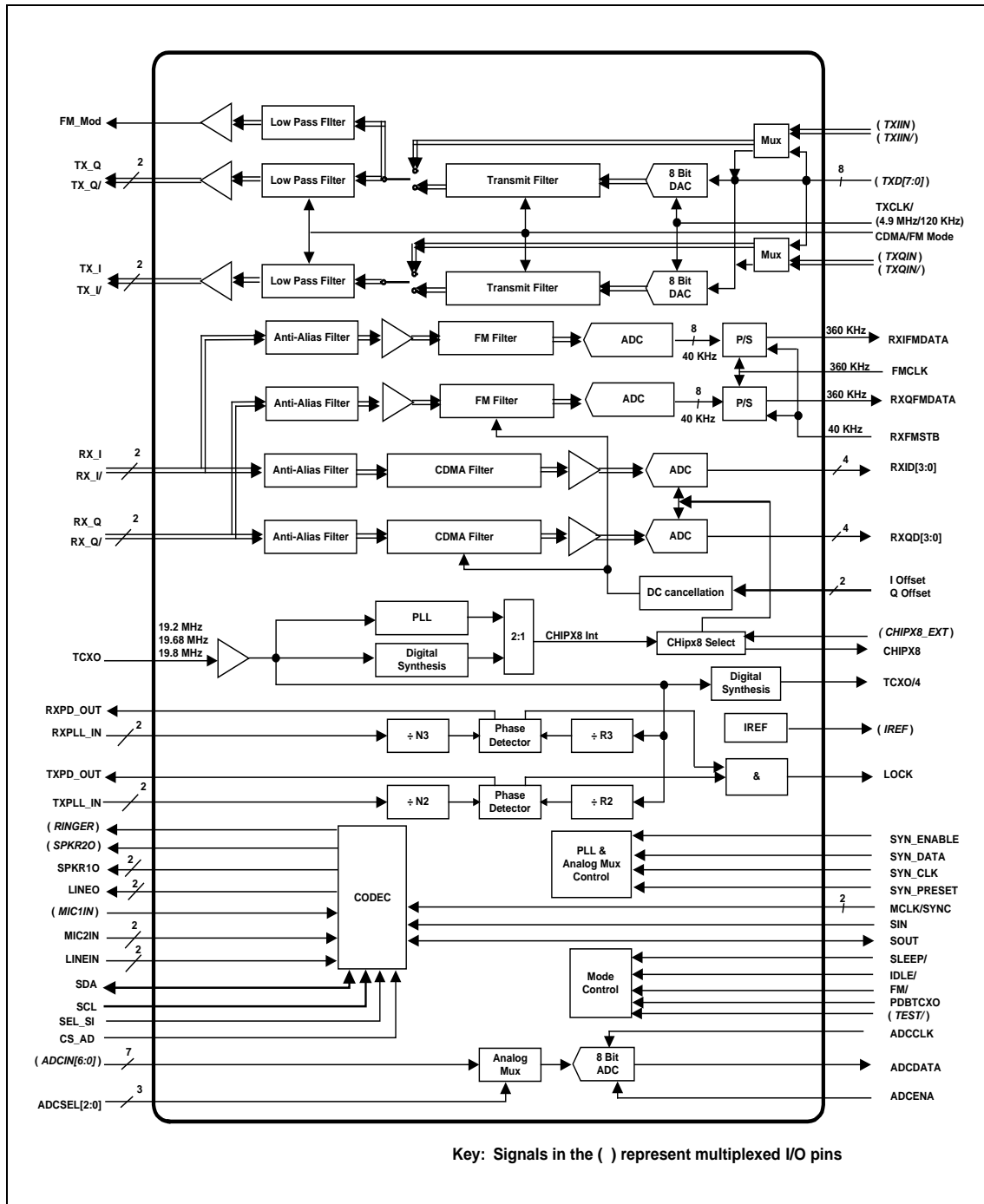
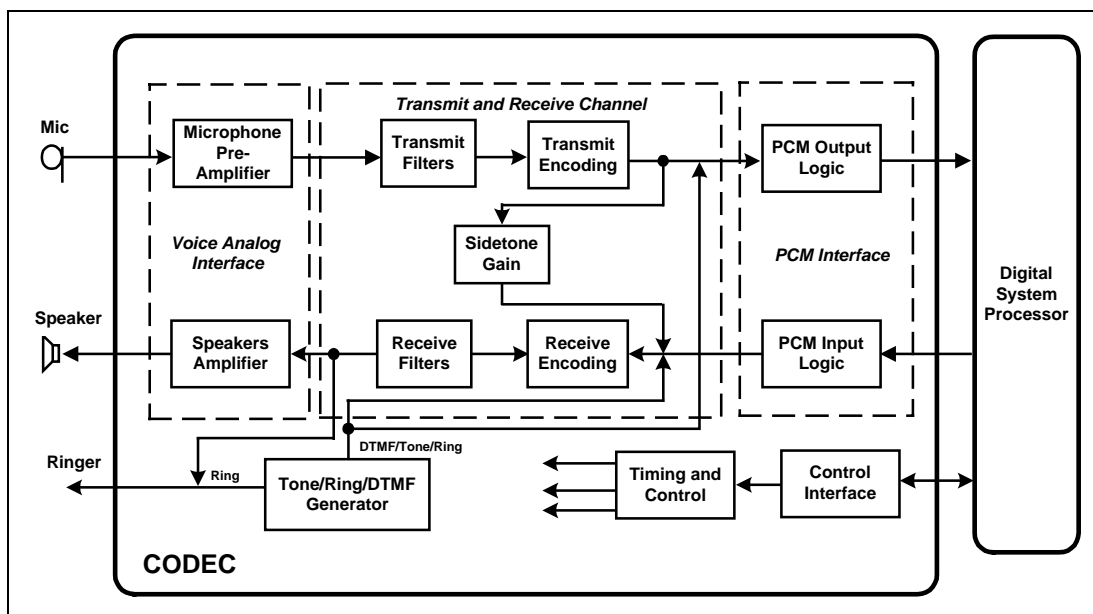Figure 4. CX20470 System Block Diagram (100-Pin μBGA Package)

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Figure 5. CX20470 BAP Audio CODEC Block Diagram (100-Pin µBGA Package)

Table 1. CX20470 BAP Signal Description: 100-Pin µBGA Package (1 of 4)

Pin #	Name	I/O Type	Description
			Receive Signal Path
D3	RXI	A,I,Z	Baseband receive in-phase analog differential input (+).
C2	RXI/	A,I,Z	Baseband receive in-phase analog differential input (–).
D2	RXQ	A,I,Z	Baseband receive quadrature analog differential input (+).
C1	RXQ/	A,I,Z	Baseband receive quadrature analog differential input (–).
B8	RXID3	D,O,L	Receive CDMA in-phase 4-bit A/D output (bit 3)
B7	RXID2	D,O,L	Receive CDMA in-phase 4-bit A/D output (bit 2)
A8	RXID1	D,O,L	Receive CDMA in-phase 4-bit A/D output (bit 1)
A9	RXID0	D,O,L	Receive CDMA in-phase 4-bit A/D output (bit 0)
E5	RXQD3	D,O,L	Receive CDMA quadrature 4-bit A/D output (bit 3)
C5	RXQD2	D,O,L	Receive CDMA quadrature 4-bit A/D output (bit 2)
B6	RXQD1	D,O,L	Receive CDMA quadrature 4-bit A/D output (bit 1)
A6	RXQD0	D,O,L	Receive CDMA quadrature 4-bit A/D output (bit 0)
D7	RXFMSTB	D,I,Z	Receive FM data strobe input.
D9	FMCLK	D,I,Z	Receive FM data clock input.
E10	RXIFMDA	D,O,L	Receive FM I serial data output.
E9	RXQFMDA	D,O,L	Receive FM Q serial data output.
			Transmit Signal Path
E6	TXD7 or IREF	D,I or A,O	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 7) for digital transmit data input mode, or IREF current output for MSM3100 interface mode
E8	TXD6 or TXIIN	D,I or A,I	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 6) for digital TX data input, or TX I channel analog differential input (+) for MSM3100 interface mode.

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Table 1. CX20470 BAP Signal Description: 100-Pin μBGA Package (2 of 4)

Pin #	Name	I/O Type	Description
Receive Signal Path (continued)			
F9	TXD5 or TXIIN/	D,I or A,I	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 5) for digital TX data input, or TX I channel analog differential input (–) for MSM3100 interface mode.
G8	TXD4 or TXQIN	D,I or A,I	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 4) for digital TX data input or TX Q channel analog differential input (+) for MSM3100 interface mode.
H9	TXD3 or TXQIN/	D,I or A,I	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 3) for digital TX data input or TX Q channel analog differential input (–) for MSM3100 interface mode.
G9	TXD2	D,I,Z	Transmit digital 8-bit data from MSM (bit 2)
H10	TXD1	D,I,Z	Transmit digital 8-bit data from MSM (bit 1)
J10	TXD0	D,I,Z	Transmit digital 8-bit data from MSM (bit 0)
B9	TXCLK/ or CHIPx8IN	D,I,Z	Configurable pin. Can be configured to be negative differential transmit clock input or CHIPx8 clock input.
H7	TXI	A,O,Z	Baseband transmit in-phase analog differential output.
K7	TXI/	A,O,Z	Baseband transmit in-phase analog differential output.
J7	TxQ	A,O,Z	Baseband transmit quadrature analog differential output (+).
K6	TxQ/	A,O,Z	Baseband transmit quadrature analog differential output (–).
G7	FM_MOD	A,O,S	FM modulation analog output signal.
Dual VHF and Clock Synthesizers			
F4	RXPLLIN	A,I,Z	Receive synthesizer divider differential input (+).
E3	RXPLLIN/	A,I,Z	Receive synthesizer divider differential input (–).
E2	RXPDOUT	A,O,Z	Receiver synthesizer (RX PLL) phase detector charge pump output.
H6	PLLFILTR	A,O,Z	Loop filter for clock PLL when enabled.
F2	TXPDOUT	A,O	Transmit synthesizer (TX PLL) phase detector charge pump output.
G2	TXPLLIN	A,I,Z	Transmit synthesizer divider differential input (+) from the external VCO buffer.
G4	TXPLLIN/	A,I,Z	Transmit synthesizer divider differential input (–) from the external VCO buffer.
J8	SYNPRES	D,I,Z	When high, disables the synthesizers.
J2	SYNENA	D,I,Z	Synthesizer three-wire serial interface enable.
K2	SYNDATA	D,I,Z	Synthesizer three-wire serial interface data input.
K3	SYNCLK	D,I,Z	Synthesizer three-wire serial interface clock input.
K1	LOCK	A,O,L	Lock detect indicator for the receive and transmit VHF synthesizers.
Mode Control			
J9	FM/	D,I,Z	FM or CDMA mode select input.
J3	SLEEP/	D,I,Z	CDMA sleep mode is enabled when this input pin is low and FM/ is high.
J4	IDLE/	D,I,Z	CDMA idle or FM idle modes are enabled when this input is low and SLEEP/ is high.
F7	PDBTCXO	D,I,Z	When this signal is activated, the BAP will power-down its TCXO buffer input clock.
H4	TEST/ or SPKR2O	D,I or A,O	Configurable pin. Can be configured to be test purposes control pin or single-ended speaker output
System Clock and Synthesized Clock			
K9	TCXO	A,I,Z	TCXO 19.2/19.68/19.8 MHz clock input.
A10	CHIPx8	D,O,L	9.8304 MHz digital clock output.
K10	TCXO/4	D,O,L	This signal, typically 4.92 MHz, is digitally synthesized from the TCXO input clock.

Table 1. CX20470 BAP Signal Description: 100-Pin µBGA Package (3 of 4)

Pin #	Name	I/O Type	Description
General Purpose ADC
D8	ADCENA	D,I,Z	Monitor A/D enable input.
C10	ADCDATA	D,O,Z	Monitor A/D data output to MSM.
C9	ADCCLK	D,O,Z	Monitor A/D clock output to MSM.
D10	ADCSEL2	D,I,Z	Monitor A/D digital 3-bit input that controls the input MUX selection (bit 2).
B5	ADCSEL1	D,I,Z	Monitor A/D digital 3-bit input that controls the input MUX selection (bit 1).
A5	ADCSEL0	D,I,Z	Monitor A/D digital 3-bit input that controls the input MUX selection (bit 0).
H8	ADC_IN6 or RINGER	A,I or D,O,Z	Configurable pin. Can be configured to be monitor A/D analog independent input for voltage sense input or RINGER output signal
K8	ADC_IN5 or MIC2IN	A,I,Z	Configurable pin. Can be configured to be monitor A/D analog independent input for voltage sense input or second single-ended microphone input.
D4	ADC_IN4	A,I,Z	Monitor A/D analog independent input for voltage sense input
B4	ADC_IN3	A,I,Z	Monitor A/D analog independent input for voltage sense input
A4	ADC_IN2	A,I,Z	Monitor A/D analog independent input for voltage sense input
E4	ADC_IN1	A,I,Z	Monitor A/D analog independent input for voltage sense input
D1	ADC_IN0	A,I,Z	Monitor A/D analog independent input for voltage sense input
Offset and Bias
A1	IOFFSET	A,I,Z	I ADC input offset adjust signal input.
B1	QOFFSET	A,I,Z	Q ADC input offset adjust signal input.
A2	VREFP	Decoupling	Positive reference bypass line.
B3	RBIAS	Decoupling	Analog input sets the system bias current via an external resistor.
B2	VREFN	Decoupling	Negative reference bypass line.
Audio CODEC
F10	MCLK	D,I,Z	CODEC master clock input, typically 2.048 MHz.
G10	SYNC	D,I,L	Frame synchronization clock input, typically 8 kHz.
F8	PCMOUT	D,O,L	Serial PCM data output.
E7	PCMIN	D,I,Z	Serial PCM data input.
A7	SCLK	D,I,Z	I2C bus or three-wire serial clock used to synchronize data transfer from and to CODEC.
C7	SINO/SDA	D,B,L	Three-wire or I2C input data path.
C6	SEL_SI	D,I,Z	User generated signal pin to select either I2C bus or three-wire interface configuration.
D6	CS/AD	D,I,Z	When in I2C bus configuration, this signal is used as bit 0 of the CODEC's device address.
D5	POR	D,I,Z	CODEC power-down signal.
G6	MICINN	A,I,Z	First negative high-impedance input to transmit pre-amplifier for microphone connection.
H5	MICINP	A,I,Z	First positive high-impedance input to transmit pre-amplifier for microphone connection
J5	LINEINN	A,I,Z	Third negative high-impedance input to transmit pre-amplifier for audio line input connection.
K5	LINEINP	A,I,Z	Third positive high-impedance input to transmit pre-amplifier for audio line input connection.
G5	MC_BG	Decoupling	MIC band gap.
K4	MC_BIAS	A,O,Z	Microphone bias voltage.
H3	SPKRON	A,O,Z	Earpiece differential (–) output.
J1	SPKROP	A,O,Z	Earpiece differential (+) output.
H2	LINEON	A,O,Z	Secondary differential (–) output.
H1	LINEOP	A,O,Z	Secondary differential (+) output.

Table 1. CX20470 BAP Signal Description: 100-Pin μBGA Package (4 of 4)

Pin #	Name	I/O Type	Description
center: **Power and Ground**			
G1	AVDDMC	PG	Power supply voltage.
G3	AVSSMC	PG	Ground.
F5	AVSSSY1	PG	Analog ground VSS input.
F3	AVSSSY2	PG	Analog ground VSS input.
F1	AVDDSY1	PG	Analog VDD input.
E1	AVDDSY2	PG	Analog VDD input.
F6	AVSS_TX	PG	Analog ground input.
J6	AVDD_TX	PG	Analog VDD input.
C8	DVSS	PG	Digital ground VSS input.
B10	DVDD	PG	Digital VDD input.
A3	AVDD_RX	PG	Analog VDD input.
C3	AVSS_RX	PG	Analog ground VSS input.
C4	VC	Decoupling	Analog ground bypass line.

I/O Type Descriptions:

    A: Analog   O: Output
    B: Bi-directional   PG: Power and ground
    D: Digital   Z: High impedance
    H: Logic high level   R: Forced to VREF
    I: Input   S: Forced to AVSS
    L: Logic low level

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Table 2. CX20470 BAP Signal Description: 56-Pin LGA Package (1 of 2)

Pin #	Name	I/O Type	Description
1	QOFFSET	A,I,Z	Q ADC input offset adjust signal input.
2	RXQ/	A,I,Z	Baseband receive quadrature analog differential input.
3	RXQ	A,I,Z	Baseband receive quadrature analog differential input.
4	RXI/	A,I,Z	Baseband receive analog differential input.
5	RXI	A,I,Z	Baseband receive analog differential input.
6	ADC_IN1	A,I,Z	Monitor A/D analog independent input for voltage sense input.
7	ADC_IN0	A,I,Z	Monitor A/D analog independent input for voltage sense input.
8	AVSSSY1	PG	Analog ground VSS input.
9	TXPDOUT	A,O	Transmit synthesizer (TX PLL) phase detector charge pump output.
10	AVDDSY1	P,G	Analog VDD input.
11	TXPLLIN/	A,I,Z	Transmit synthesizer divider differential input (–) from the external VCO buffer.
12	TXPLLIN	A,I,Z	Transmit synthesizer divider differential input (+) from the external VCO buffer.
13	SYNENA	D,I,Z	Synthesizer three-wire serial interface enable.
14	LOCK	A,O,L	Lock detect indicator for the receive and transmit VHF synthesizers.
15	SYNDATA	D,I,Z	Synthesizer three-wire serial interface data input.
16	SYNCLK	D,I,Z	Synthesizer three-wire serial interface clock input.
17	IDLE/	D,I,Z	CDMA idle or FM idle modes are enabled when this input is low and SLEEP/ is high.
18	SLEEP/	D,I,Z	CDMA sleep mode is enabled when this input pin is low and FM/ is high.
19	AVSS_TX	PG	Analog ground input.
20	AVDD_TX	PG	Analog VDD input.
21	PDBTCXO	D,I,Z	When this signal is activated, the BAP will power-down its TCXO buffer input clock.
22	TXQ/	A,O,Z	Baseband transmit quadrature analog differential output (–).
23	TXQ	A,O,Z	Baseband transmit quadrature analog differential output (+).
24	TXI/	A,O,Z	Baseband transmit in-phase analog differential output.
25	TXI	A,O,Z	Baseband transmit in-phase analog differential output.
26	TCXO	A,I,Z	TCXO 19.2/19.68/19.8 MHz clock input.
27	TCXO/4	D,O,L	This signal, typically 4.92 MHz, is digitally synthesized from the TCXO input clock.
28	TXD0	D,I,Z	Transmit digital 8-bit data from MSM (bit 0).
29	TXD1	D,I,Z	Transmit digital 8-bit data from MSM (bit 1).
30	TXD2	D,I,Z	Transmit digital 8-bit data from MSM (bit 2).
31	TXD3 or TXQIN/	D,I or AI	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 3) for digital TX data input or TX Q channel analog differential input (–) for MSM3100 interface mode.
32	TXD4 or TXQIN	D,I or A,I	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 4) for digital TX data input or TX Q channel analog differential input (+) for MSM3100 interface mode.
33	TXD5 or TXIIN/	D,I or A,I	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 5) for digital TX data input, or TX I channel analog differential input (–) for MSM3100 interface mode.
34	TXD6 or TXIIN	D,I or A,I	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 6) for digital TX data input, or TX I channel analog differential input (+) for MSM3100 interface mode.
35	TXD7 or IREF	D,O or A,O	Configurable pin. Can be configured to be transmit digital 8-bit data from MSM (bit 7) for digital transmit data input mode, or IREF current output for MSM3100 interface mode

Table 2. CX20470 BAP Signal Description: 56-Pin LGA Package (2 of 2)

Pin #	Name	I/O Type	Description
36	ADCENA	A,I,Z	Monitor A/D enable input.
37	ADCCLK	A,O,Z	Monitor A/D clock output to MSM.
38	ADCDATA	A,O,Z	Monitor A/D data output to MSM.
39	DVSS	PG	Digital ground VSS input.
40	DVDD	PG	Digital VDD input.
41	TXCLK/ or CHIPx8IN	D,I,Z	Configurable pin. Can be configured to be negative differential transmit clock input or CHIPx8 clock input.
42	CHIPx8	D,O,L	9.8304 MHz digital clock output.
43	RXID0	D,O,L	Receive CDMA in-phase 4-bit A/D output (bit 0).
44	RXID1	D,O,L	Receive CDMA in-phase 4-bit A/D output (bit 1).
45	RXID2	D,O,L	Receive CDMA in-phase 4-bit A/D output (bit 2).
46	RXID3	D,O,L	Receive CDMA in-phase 4-bit A/D output (bit 3).
47	RXQD0	D,O,L	Receive CDMA quadrature 4-bit A/D output (bit 0).
48	RXQD1	D,O,L	Receive CDMA quadrature 4-bit A/D output (bit 1).
49	RXQD2	D,O,L	Receive CDMA quadrature 4-bit A/D output (bit 2).
50	RXQD3	D,O,L	Receive CDMA quadrature 4-bit A/D output (bit 3).
51	ADCSEL0	D,I,Z	Monitor A/D digital 3-bit input that controls the input MUX selection (bit 1).
52	VC	Decoupling	Analog ground bypass line.
53	RBIAS	Decoupling	Analog input sets the system bias current via an external resistor.
54	VREFP	Decoupling	Positive reference bypass line.
55	VREFN	Decoupling	Negative reference bypass line.
56	IOFFSET	A,I,Z	I ADC input offset adjust signal input.

I/O Type Descriptions:

    A: Analog   O: Output
    B: Bi-directional   PG: Power and ground
    D: Digital   Z: High impedance
    H: Logic high level   R: Forced to VREF
    I: Input   S: Forced to AVSS
    L: Logic low level

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Proprietary Information and Specifications are Subject to Change

Table 3. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Power supply	−0.3	3.6	V
Analog input voltage	−0.3	VDD+0.3	V
Digital input voltage	−0.3	VDD+0.3	V
Input current per pin	−10	+10	mA
Output current per pin	−50	+50	mA
Short circuit duration, to GND or VDD		1	sec
Ambient temperature (power applied)	−55	+125	°C
Storage temperature	−65	+150	°C

Table 4. Recommended Operating Conditions

Parameter	Min	Typical	Max	Units
Power supply for full performance	2.7	3.0	3.6	V
Operating junction temperature	−40		+100	°C
Operating ambient temperature	−40		+85	°C

Table 5. CX20470 BAP Electrical Specifications (1 of 2)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Power Supply Current (BAP only, Without CODEC)						
Supply current - CDMA RxTx	$I_{DD}1$			12 (Note 1)		mA
Supply current - CDMA idle	$I_{DD}2$			8 (Note 1)		mA
Supply current - CDMA sleep	$I_{DD}3$			0.5		mA
Supply current - FM RxTx	$I_{DD}4$			7 (Note 1)		mA
Supply current -FM idle	$I_{DD}5$			4 (Note 1)		mA
Supply current - power down	$I_{DD}6$			15		µA
Power Supply Current (CODEC only, Without BAP)						
Supply current - RxTx	$I_{DD}7$			0.7		mA
Supply current - CODEC standby	$I_{DD}10$			<1		µA
Supply current - CODEC power down	$I_{DD}11$			<1		µA

Table 5. CX20470 BAP Electrical Specifications (2 of 2)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
AC/DC						
Logic high input voltage	V$_{IH}$		0.7X			V
Logic low input voltage	V$_{IL}$				0.3X	V
Logic high output voltage	V$_{OH}$		2.7			V
Logic low output voltage	V$_{OL}$				0.4	V
Logic input leakage current	I$_{IL}$	VDD = Maximum, VIN = GND to VDD	−100		+100	μA
Digital input capacitance	C$_{ID}$				10	pF
Digital output load capacitance	C$_{LD}$				15	pF
Digital output load resistance	R$_{LD}$		100			kΩ
Offset adjust input impedance (IOFFSET, QOFFSET)	Z$_{IOA}$		100			kΩ
TCXO input capacitance					10	pF
TCXO input resistance			5			kΩ
TCXO input signal level			0.5			Vp-p
RxI, RxQ single-ended input resistance		CDMA mode	28	40	52	kΩ
RxI, RxQ single-ended input capacitance		CDMA mode		5		pF
RxI, RxQ single-ended input resistance		FM mode	140	200	260	kΩ
RxI, RxQ single-ended input capacitance		FM mode		5		pF
TxI, TxQ single-ended output resistance			0.7	1	1.3	kΩ
TxI, TxQ single-ended output capacitance				5		pF
FM_MOD output resistance			0.7	1	1.3	kΩ
FM_MOD output capacitance				5		pF

Note 1: Supply current also includes two VHF synthesizers operating in the highest frequency mode. For lower frequency modes, the current consumption of each VHF synthesizer is reduced by 0.5 mA.

Table 6. Absolute Input Signal Levels at MICIN/LINEIN

Amplifier Output	Condition	Min	Typical	Max	Units
0 dBm0 level Overload level	Transmit amplifier is programmed for 0 dB gain		492.6 707.1		mV$_{rms}$
0 dBm0 level Overload level	Transmit amplifier is programmed for 40 dB gain		3.694 5.302		mV$_{rms}$

Table 7. CODEC Analog Input Interface Electrical Characteristics

Description	Min	Typical	Max	Units
Input offset voltage at MIC1IN, MIC2IN, and LINEIN audio inputs	−5		+5	mV
Input bias current at MIC1IN, MIC2IN, and LINEIN audio inputs	−200		+200	nA
Input capacitance at MIC1IN, MIC2IN, and LINEIN audio inputs		1.5		pF
Output source current	1			mA
Microphone bias supply voltage		2.0		V
Input impedance (fully differential)	50			kΩ
Microphone mute attenuation	−80			dB
Isolation between MICIN and LINEIN inputs	74			dB

Table 8. Absolute Output Signal Levels at SPKRO/LINEO

Amplifier Input	Condition	Min	Typical	Max	Units
0 dBm0 level	Receive amplifier is programmed for 0 dB gain		1.06		mVrms
0 dBm0 level	Transmit amplifier is programmed for –30 dB gain		61.85		mVrms

Table 9. CODEC Analog Output Interface Electrical Characteristics

Description	Min	Typical	Max	Units
AC voltage output (peak-to-peak)			4	Vp-p
Output offset voltage (single ended) relative to ground at SPKR1O, SPKR2O, and LINEO	–30		+30	mV
Output offset voltage (fully differential) relative to ground at speaker output (SPKRO) and line output (LINEO)	-50		+50	mV
Maximum output current for SPKR1O output (rms)			10	mA
Maximum output current for SPKR2O output (rms)			10	mA
Maximum output current for LINEO output (rms)			46	mA
Output resistance at SPKR1O, LINEO		1		Ω
Output resistance at SPKR2O		0.5		Ω
Output load resistance	30			Ω
Output load capacitance		50		pF
Gain change (when power-down mode, max level when muted)	–60			dB
Speaker mute attenuation	–80			dB
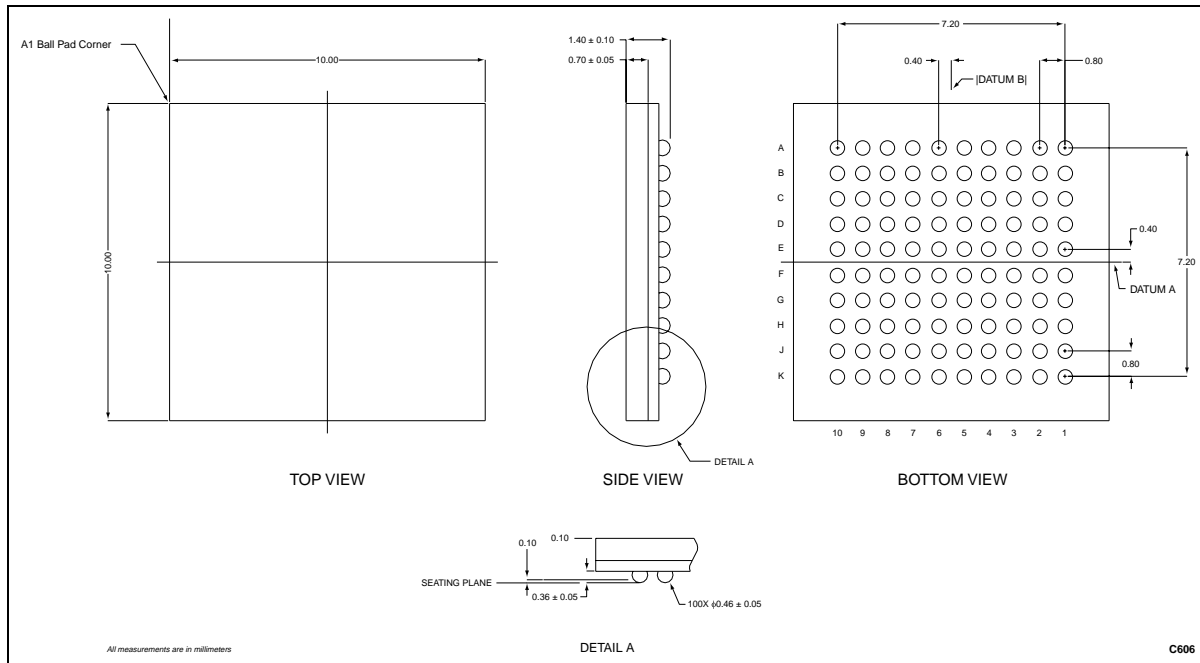
Figure 6. CX20470 BAP Package Dimensions – 100-Pin μBGA
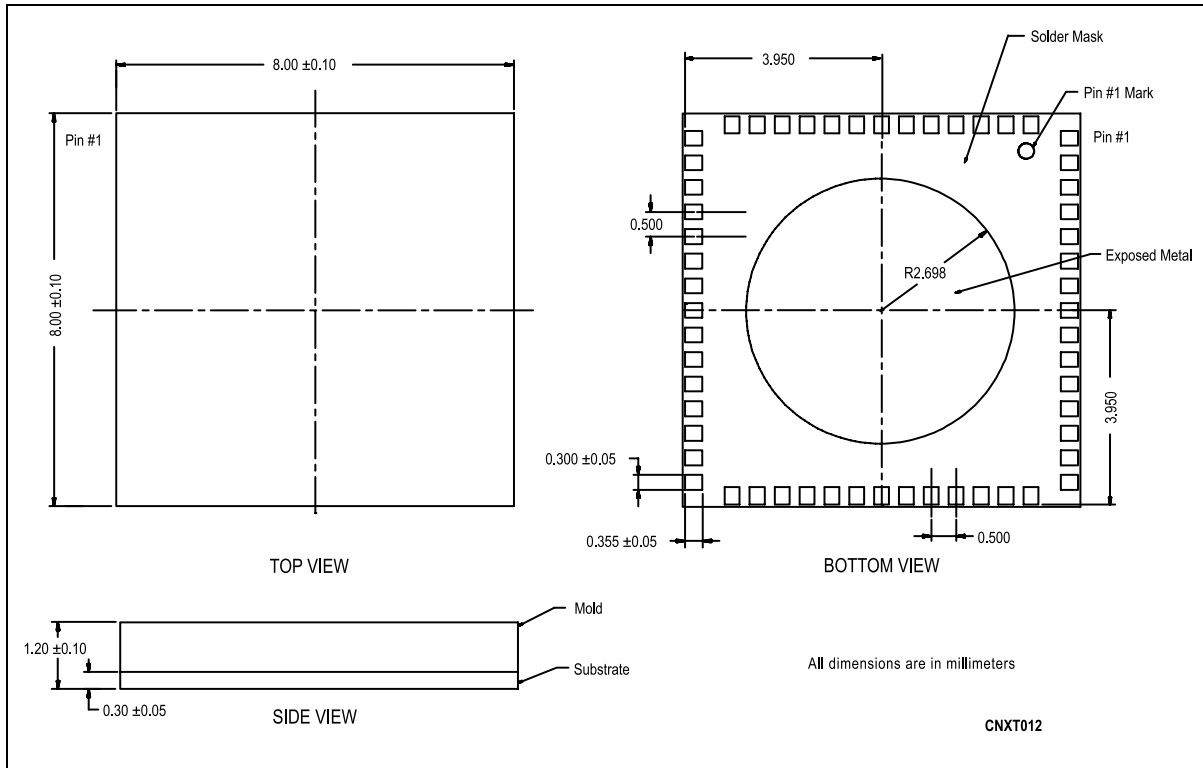
Figure 7. CX20470 BAP Package Dimensions - 56-Pin LGA

Ordering Information

Model Name	Manufacturing Part Number	Product Revision
CX20470 100-pin μBGA CX20470 56-pin LGA		

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