Data Sheet
June 1995

AT&T Microelectronics

ATT20C490, 16M Color
ATT20C493, 256K Color
True-Color CMOS RAMDACs

Features

- Similar functionality and footprint to ATT20C491/492
- 110/100/80/66 speed grades
- 16M, 256K, 64K, 32K, 256 on-screen colors
- Five software selectable color modes:
  — 24- (18-), 16-, 15-bit true-color bypass
  — 15-bit dual-clock edge true-color bypass
  — 8-bit pseudocolor
- True color eliminates window color corruption
- True color helps eliminate aliasing
- *XGA**, *TARGA*†, HICOLOR formats
- VGA accessible control register
- ATT20C490/493 powers down to 3 mA typical while retaining palette updates
- Low power dissipation: 0.5 W typical
- Internal V_{REF} accuracy better than ±3%
- External V_{REF} option with powerdown disable
- On-chip output comparators for monitor detection
- Antisparkle circuitry
- Program DACs to 8 bits or 6 bits
- 256 x 24 (18) color RAM
- 15 x 24 (18) overlay RAM
- RS-343A, RS-170, and *PS/2** compatible
- 44-pin PLCC industry-standard compatible footprints

Note: Numbers in parentheses indicate ATT20C493 functionality.

* *XGA* and *PS/2* are registered trademarks of International Business Machines Corporation.
† *TARGA* is a trademark of Truevision Corporation.
‡ *Microsoft* is a registered trademark and *Windows* is a trademark of Microsoft Corporation.

Applications

- True-color desktop, laptop, and notebook PCs
- True-color add-in card or motherboard PC designs
- Screen resolutions:
  — 1280 x 1024, 60 Hz noninterlaced
  — 1024 x 768, 85 Hz noninterlaced

Application Differences
(From ATT20C491/492)

- The ATT20C490/493 do not offer the following:
  — Gamma-corrected true-color modes
  — True control pin
  — Test register
- See page 7 for additional details on the differences between the ATT20C490/493 and the ATT20C491/492.

Description

The ATT20C490/493 CMOS RAMDACs support 24- (18-), 16-, 15-bit true color along with 8-bit pseudocolor applications. The ATT20C490/493 support *XGA*, *Microsoft* Windows‡, *TARGA*, and HICOLOR graphics. The ATT20C490/493 ensure correct window colors for multiapplication displays. True color enables software to antialias by color dithering.

True-color graphics allow multiple applications simultaneous use of 16M colors. Multiple software applications no longer contend for control of 256 colors. Each application's window has the desired colors. True-color graphics help eliminate aliasing by providing a full range of colors for each pixel. Each pixel in a stair-stepped diagonal line can be color blended with surrounding pixels to create a smooth diagonal line.

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Description (continued)

This device can replace the ATT20C491/492 RAMDAC when used in bypass modes and is pin and function compatible. Software has the ability to differentiate between all ATT20C49X devices. This function is embedded in a read operation. The ATT20C490/493 powers down to ≤3 mA total current while retaining palette data and read/write capability. It is designed to work with an internal or external voltage reference only.

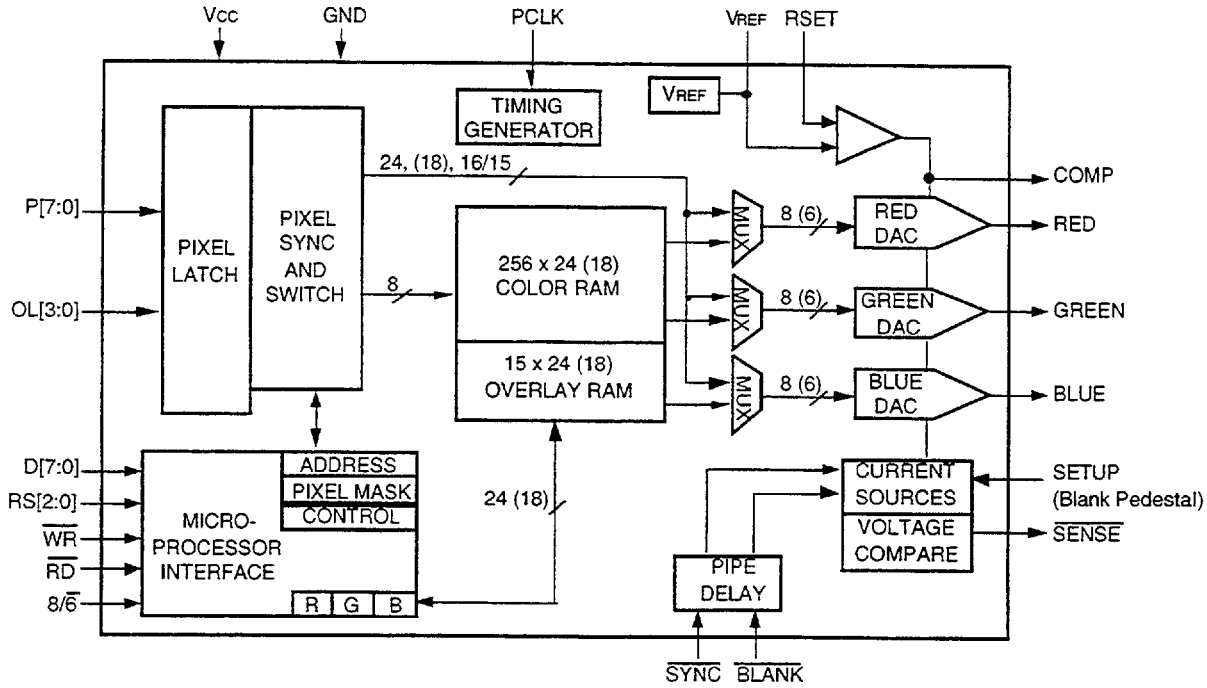
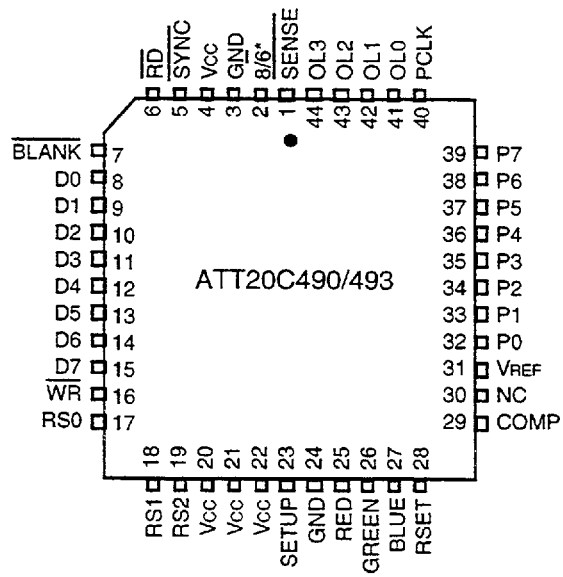


Figure 1. Block Diagram

Pin Information



* This pin is not used on the ATT20C493. Tie to Vcc or GND.

Figure 2. 44-Pin PLCC Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

ATT20C490/493 Pin #	Symbol	Type	Name/Function
1	$\overline{\text{SENSE}}$	O	**$\overline{\text{SENSE}}$ (Active-Low).** TTL compatible. Monitor detection signal. $\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level of 340 mV. $\overline{\text{SENSE}}$ may not be stable while SYNC is toggling.
2	8/$\overline{6}$ (Not used 493)	I	**8/$\overline{6}$ -bit Switch (Active-Low).** TTL compatible. Color resolution select. This control input specifies whether the MPU is reading and writing 8 bits (logic 1) or 6 bits (logic 0) of color information each cycle. It also determines whether the DACs display 6 bits or 8 bits of data. This pin is ORed with CR1 in the control register. This pin is not used on the ATT20C493. **Note:** Tie to Vcc or GND.
3, 24	GND	—	**Ground.**
4, 20—22	Vcc	—	**Power.**
5	$\overline{\text{SYNC}}$	I	**$\overline{\text{SYNC}}$ (Active-Low).** TTL compatible. Latched on the rising edge of PCLK. SYNC removes a 7.62 mA (RS-343A) current source from each RGB. For $\overline{\text{SYNC}}$ to operate properly, it should be asserted only during blanking. For systems having a sync signal separate from the RAMDAC, $\overline{\text{SYNC}}$ should be tied low to turn off the sync current source.
6	$\overline{\text{RD}}$	I	**Read (Active-Low).** TTL compatible. When $\overline{\text{RD}}$ is low, data transfers from the selected internal register to the data bus. RS[2:0] is latched on the falling edge of $\overline{\text{RD}}$.
7	$\overline{\text{BLANK}}$	I	**$\overline{\text{BLANK}}$ (Active-Low).** TTL compatible. $\overline{\text{BLANK}}$ is latched on the rising edge of PCLK. When $\overline{\text{BLANK}}$ is low, the 1.44 mA current source on the analog outputs will be turned off. The DACs ignore digital input from memory. The RAMDAC and overlay memory can be updated during blanking.
8—15	D[7:0]	I/O	**Data Bus.** TTL compatible. Data is transferred between the data bus and the internal registers under control of the $\overline{\text{RD}}$ / $\overline{\text{WR}}$ signals. In an MPU write operation, D[7:0] is latched on the rising edge of $\overline{\text{WR}}$. To read data D[7:0] from the device, $\overline{\text{RD}}$ must be active. The rising edge of the $\overline{\text{RD}}$ signal indicates the end of a read cycle. Following the read cycle, the data bus will go to a high-impedance state. For 6-bit operation, color data is contained in the lower 6 bits of the data bus. D0 is the LSB, and D5 is the MSB. When the MPU writes color data, D6 and D7 are ignored. During MPU read cycles, D6 and D7 are a logic 0.
16	$\overline{\text{WR}}$	I	**Write (Active-Low).** TTL compatible. $\overline{\text{WR}}$ controls the data transfer from the data bus to the selected internal register. D[7:0] data is latched at the rising edge of $\overline{\text{WR}}$, and RS[2:0] data is latched at the falling edge of $\overline{\text{WR}}$.
17—19	RS[2:0]	I	**Register Select.** TTL compatible. These inputs are sampled on the falling edge of the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to determine which one of the internal registers is to be accessed. RS2 is not needed to access the control register. See the Control Register section under Functional Description.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

ATT20C490/493 Pin #	Symbol	Type	Name/Function
23	SETUP	I	**Pedestal Setup.** TTL compatible. A logic high will cause a blanking pedestal of 1.44 mA on an RS-343A output.
25 26 27	RED GREEN BLUE	O	**Color Signals.** These pins are analog outputs. These high-impedance current sources are capable of driving a double-terminated 75 Ω coaxial cable.
28	RSET	I	**Reference Resistor.** An external resistor (RSET) is connected between the RSET pin and GND to control the magnitude of the full-scale current. Refer to DAC Gain section under Functional Description.
29	COMP	—	**Compensation Pin.** Bypass this pin with an external 0.1 µF capacitor to Vcc.
30	NC	—	**No Connect.** No internal connection to the chip.
31	V_{REF}	I	**Voltage Reference.** If an external voltage is used, supply this input with a 1.235 V reference. This node is disabled internally during powerdown.
32—39	P[7:0]	I	**Pixel Address.** TTL compatible. These pins are latched on the rising edge of PCLK except in HICOLOR1 mode when they are latched with both the rising and falling edges of PCLK. Pixels can be presented to the DACs as color data or used as addresses to look up color data in the color RAM. Unused inputs should be connected to GND.
40	PCLK	I	**Pixel Clock.** TTL compatible. The duty cycle of the clock should be between 40% and 60%. The rising edge of the pixel clock latches the pixel address and BLANK and SYNC inputs. The pixel clock controls the four-stage video pipelined operation.
41—44	OL[3:0]	I	**Overlay Address.** TTL compatible. These pins are latched on the rising edge of PCLK. These inputs are used to specify one of the 15 addresses of the color overlays. When the overlay address is non-zero, the pixel address inputs are ignored. Unused inputs should be connected to GND.

Table 2. Register Map

RS2	RS1	RS0	Addressed by the MPU
0	0	0	Address register (color RAM write mode)
0	1	1	Address register (color RAM read mode)
0	0	1	RAMDAC color RAM
0	1	0	Pixel read mask register (RMR)
1	0	0	Address register (overlay write mode)
1	1	1	Address register (overlay read mode)
1	0	1	Overlay color RAM
1	1	0	Control register (CR)*

* The control register can be accessed by reading the read mask register four times. Refer to the Control Register Access Using the RMR section under Functional Description (page 10).

Functional Description

***Table 3.* Control Register**

This register is operational on powerup. It can be read or written to by the MPU at any time and is not initialized. This register can be written to by using RS[2:0] as address pins or read by first reading the read mask register.

Bit	Name/Description
CR[7:5]	**Color Mode.** These bits are used to control the various color modes as shown in Table 5. These bits are also used to identify the ATT20C490/493 from other RAMDACs.
CR[4:2]	**Sync Enable.** Logic 0: Sync disabled. Logic 1: Sync enabled. Bits CR4, CR3, and CR2, respectively, specify whether the blue, green, or red outputs will have sync offset current. A logic 1 specifies sync current. The sync currents enabled by CR4, CR3, and CR2 are controlled by the $\overline{\text{SYNC}}$ pin. For noncomposite sync, tie the $\overline{\text{SYNC}}$ pin to logic 0.
CR1	**8-/6-bit Select.** Logic 0: 6 bit. Logic 1: 8 bit. A logic 1 specifies 8-bit color operation (16M possible colors). A logic 0 specifies 6-bit color operation (256K possible colors). This bit is ORed with the 8/$\overline{6}$ pin.
CR0	**Sleep Enable.** Logic 0: Normal operation. Logic 1: Sleep mode. If this bit is logic 0, the device will be in normal operation. If this bit is logic 1, the DAC is turned off and the palette RAM is powered down. The RAM retains data and will wake up to accept inputs from the MPU port. After accepting MPU data, the RAM returns to the sleep state. After programming the device for normal operation, valid data will appear at the DAC outputs in about one second.

Functional Description (continued)

Table 4. Differences Between ATT20C490/493 and ATT20C491/492 RAMDACs

Feature	ATT20C491/492*	ATT20C490/493
■ True-color gamma correction	■ Yes. Modes 1, 2, and 3.	■ No. True-color bypass operation only.
■ True control pin	■ Yes. For hardware select of true-color modes.	■ No. True-color modes controlled by control register bits CR[7:5] only.
■ Test register	■ Yes. PSA signature analysis register in overlay location 0.	■ No test register.
■ Variable pipeline delay	■ Yes. Different pipeline delay when between gamma corrected and bypass true-color modes.	■ No. Pipeline delay fixed at four pixel clocks.
■ Powerdown	■ Yes (491). No (492).	■ Yes (490/493).

* For details on operation, refer to the *ATT20C491/492 CMOS RAMDACs* Data Sheet.

Table 5. Color Modes

The following table details the five color modes of the ATT20C490/493. These modes are set by bits CR[7:5] of the control register.

Mode	CR[7:5]	Description	Rising Clock Edges	LUT Access	Pipe Delay	R[7:0]	G[7:0]	B[7:0]	Comment
0	0XX	8-bit pseudo-color	1	Yes	4	P[7:0]	P[7:0]	P[7:0]	Default
4*	100	15-bit bypass	1	No	4	P[14:0] rrrrr000	P[9:5] ggggg000	P[4:0] bbbbb000	HICOLOR1
5	101	15-bit bypass	2	No	4	P[14:0] rrrrr000	P[9:5] ggggg000	P[4:0] bbbbb000	HICOLOR2
6	110	16-bit bypass	2	No	4	P[15:11] rrrrr000	P[10:5] gggggg00	P[4:0] bbbbb000	*XGA2*
7	111	24-bit bypass (18-bit bypass)	3	No	4	P[23:18] rrrrrrrr	P[15:0] gggggggg	P[7:0] bbbbbbbb	16M color

* This mode valid up to 66 MHz.

Functional Description (continued)

Color Modes

The ATT20C490/493 provides five different color modes that are selectable by programming the MPU control register bits CR[7:5]. True-color modes do not use the color look-up tables or pixel read mask register. Overlays take precedence in pseudocolor mode (mode 0). In true-color modes, a pixel modulo 2 or 3 counter will provide the internal load pulse that updates the DAC inputs. An active BLANK signal clears the modulo counter.

Mode 0: 8-bit pseudocolor (one clock per pixel). This mode is selected by setting control register bits CR[7:5] to 0XX. In this mode, 8 bits of pixel information are input to the device on every video clock cycle (see Figure 3). The P[7:0] inputs are latched on every rising edge of the pixel clock.

Mode 4: 15-bit true-color bypass (5-5-5 one clock per pixel). This mode corresponds to 15-bit HICOLOR1 mode. This mode is selected by setting the control register bits CR[7:5] to 100. The pixel information is collected over a single pixel clock cycle. The rising edge of PCLK latches the eight LSBs followed by the falling edge latching the eight MSBs. The latched 16-bit field is partioned as follows: bits 14:10 form the red pixel data; 9:5 form the green; 4:0 form the blue; and bit 15 is ignored. (See Figures 3 and 4.) The LSBs of the partitioned pixel information are set to logic 0. In this mode, the DAC outputs will be updated every video clock.

Mode 5: 15-bit true-color bypass (5-5-5 two clocks per pixel). This mode corresponds to 15-bit HICOLOR2 mode. This mode is selected by setting the control register bits CR[7:5] to 101. The pixel information is collected over two rising edges of the pixel clock. BLANK going high will signal that the first pixel information is available on P[7:0]. The rising edge of PCLK that captures BLANK going high also captures the LSBs of the pixel information. The LSBs are latched first, followed by the MSBs. The LSBs and MSBs follow in succession until BLANK goes low. The latched 16-bit field is partioned as follows: bits 14:10 form the red pixel data; 9:5 form the green; 4:0 form the blue; and bit 15 is ignored. (See Figures 3 and 4.) The LSBs of the pixel information are set to logic 0. In this mode, the DAC outputs will be updated on every second video clock.

Mode 6: 16-bit true-color bypass (5-6-5 two clocks per pixel). This mode corresponds to 16-bit *XGA2* mode. This mode is selected by setting the control register bits CR[7:5] to 110. The pixel information is collected over two rising edges of the pixel clock, and then is presented directly to the DACS. BLANK going high will signal that the first pixel information is available on P[7:0]. The rising edge of PCLK that captures BLANK going high also captures the LSBs of the pixel information. The LSBs are latched first, followed by the MSBs. The LSBs and MSBs follow in succession until BLANK goes low. The latched 16-bit field is partioned as follows: bits 15:11 form the red pixel data; 10:5, the green; and 4:0, the blue. (See Figures 3 and 4.) The LSBs of the pixel information are set to logic 0. In this mode, the DAC outputs will be updated on every second video clock.

Mode 7: 24-bit true-color bypass (8-8-8 three clocks per pixel). This mode is selected by setting the control register bits CR[7:5] to 111. The pixel information is collected over three rising edges of the pixel clock. BLANK going high will signal that the first pixel information is available on P[7:0]. The rising edge of PCLK that captures BLANK going high also captures the blue information of the first pixel. The blue pixel is latched first, followed by the green and red. Blue, green, and red follow in succession until BLANK goes low. (See Figure 3.) In this mode, the DAC outputs will be updated on every third video clock.

Table 6. Maximum Resolution by Speed Grade and Color Modes

Clock Per Pixel	Mode #	Mode	66 MHz	Clock Rate (MHz)	80 MHz	Clock Rate (MHz)	100 MHz	Clock Rate (MHz)	110 MHz	Clock Rate (MHz)
One	0	8-bit	1024 x 768 60 Hz	65	1024 x 768 75 Hz	80	1024 x 1024 60 Hz	95	1280 x 1024 60 Hz	107.5
	4	15-bit	1024 x 768 60 Hz	65	—	—	—	—	—	—
Two	5	15-bit	640 x 480 72 Hz	62.5	800 x 600 60 Hz	80	800 x 600 72 Hz	100	—	—
	6	16-bit								
Three	7	24-bit	—	—	640 x 480 60 Hz	75.5	640 x 480 72 Hz	93.6	800 x 600 56 Hz	108

Functional Description (continued)

Color Modes (continued)

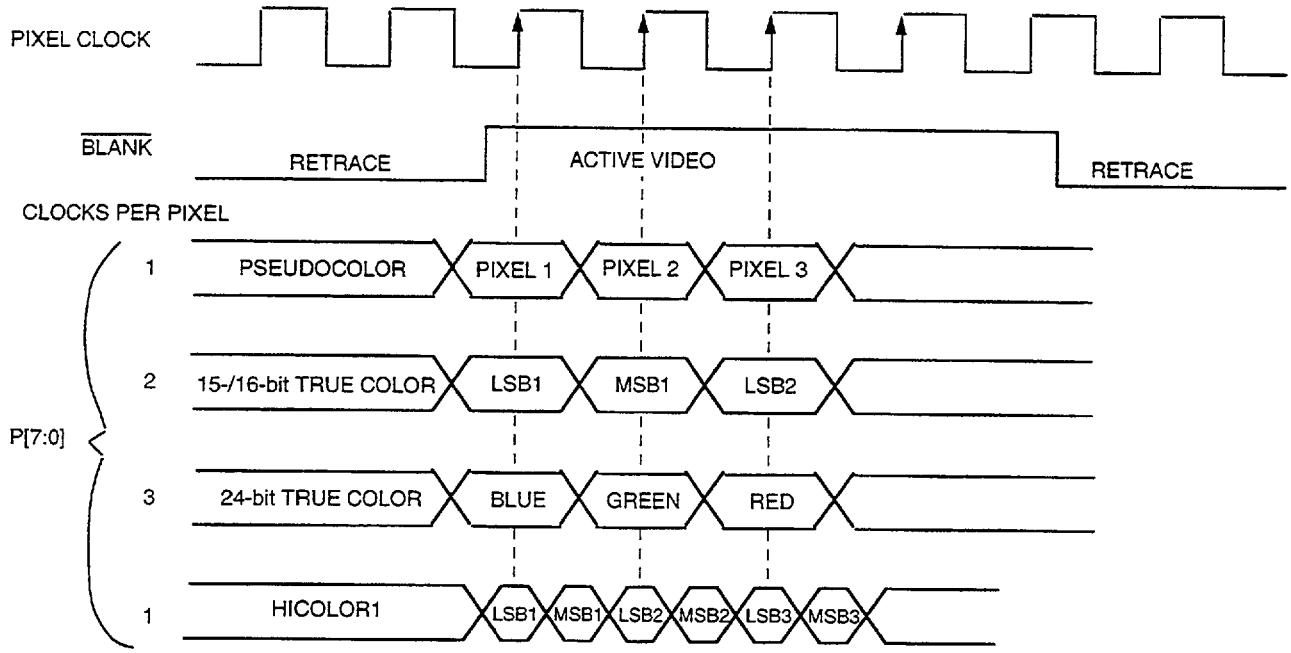
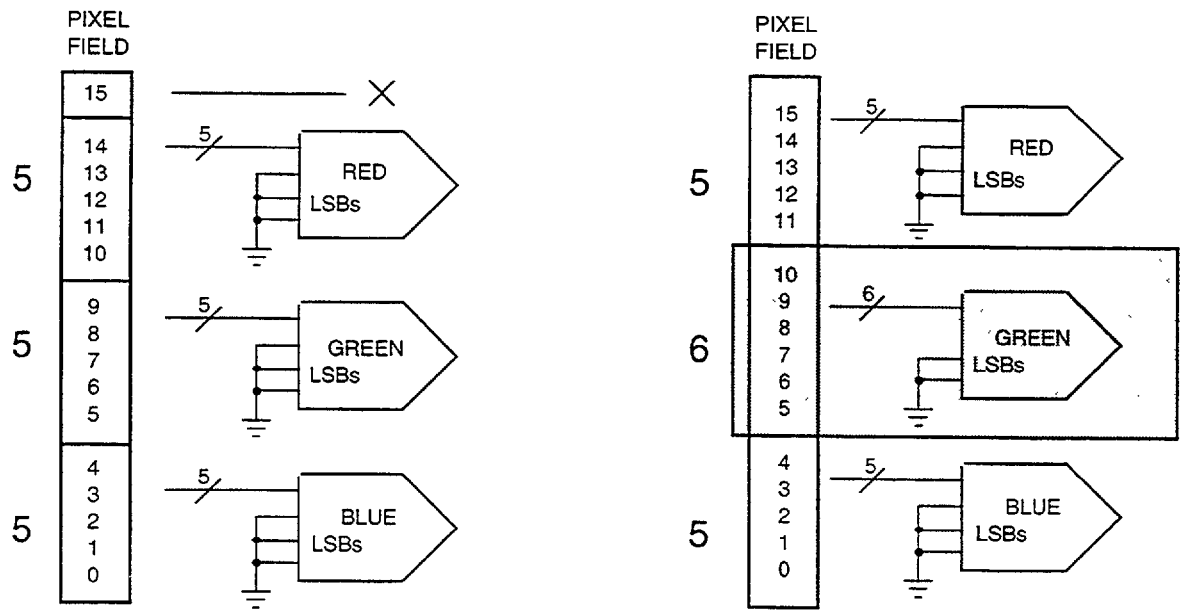


Figure 3. Pixel Data for Color Modes



A. 15-bit True Color (5-5-5) **B. 16-bit True Color (5-6-5)**

Figure 4. 15-/16-Bit Field Split for True-Color Modes

Functional Description (continued)

Pixel Read Mask Register (RMR)

The contents of the pixel read mask register (RMR) can be accessed by the MPU at any time and is not initialized. The RMR bits are logically ANDed with the 8-bit pixels in pseudocolor mode. In true-color modes, pixels are not modified by the RMR. A logic 1 stored in a data bit of the RMR leaves the corresponding bit in the pixel unchanged. A logic 0 in the RMR sets the pixel bit to zero. Bit D0 of the RMR corresponds to pixel bit P0. By reading the RMR four times, the control register will be accessed on the next read or write to the RMR.

Control Register

The control register can be written to or read by the MPU at any time and is not initialized. CR0 is the least significant bit in the control register and corresponds to D0 of the MPU port. Table 3 defines the bits of the control register. Bits CR[7:5] determine the color mode as shown in Table 4. These bits are also used for software identification (see software identification section).

Bits CR[4:2] indicate which analog channels will have composite sync information present when $\overline{\text{SYNC}}$ is asserted. CR1 controls whether 8 bits or 6 bits of color information are being passed over the D[7:0] port and whether the DACs are 8 bits or 6 bits (ATT20C490 only). This bit is logically ORed with the $\overline{8}/6$ pin (ATT20C490 only). A logic 1 in bit CR0 puts the RAMDAC to sleep. The RAMDAC wakes up to accept updates to the color RAM, and then goes back to sleep. Hence, the device tracks changes to the color look-up table while utilizing minimum power.

Control Register Access Using the RMR

For graphics systems controllers that do not have a control signal for RS2, the control register may be accessed by using the following sequence of events.

A flag will be set when the address register (ADDR) is read once, and then the RMR (RS = 1, RS = 0, also defined as VGA I/O port $3C6) is read four times consecutively. The next read or write to the RMR will be sent to the control register. Another read of the ADDR should be performed to reset the internal state machine. The count to four results in a single access and has to be repeated for each access to the control register via the RMR. Reading or writing any other register during the count will reset the flag.

Hence, any of the control register bits can be programmed by systems and graphics controllers not having an RS2 address pin.

Software Identification

The ATT20C490/493 can be differentiated from other 49X RAMDACs by programming control register bits CR[7:5] with 011 and reading the bits using the RMR. If zeros are returned, the device is an ATT20C490/493. The ATT20C490/493 can be differentiated from the ATT20C47XA family by trying to read the control register using the RMR. If this cannot be done, the device is from the ATT20C47X family. See Table 7 and Figure 5.

Table 7. Software Identification

Part Number	CR[7:5]	
	Write	Read*
ATT20C497	111	000
ATT20C491/492	111	111
ATT20C490/493	011	000
ATT20C47XA	†	†

* The read must be accomplished through the read mask register.
† The 47XA RAMDACs cannot be accessed in this manner and will identify themselves by this characteristic.

Figure 5 illustrates how programmers can identify the ATT20C47X family and ATT20C49X RAMDACs. The RMR is the pixel read mask register; write CR indicates that the programmer should write to the control register; and read CR indicates that the programmer should read the control register. Reading the address register resets the internal state machine.

Functional Description (continued)

Software Identification (continued)

- **Procedure to write CR**
  1. Read address register (VGA $3C8)
  2. Read RMR four times (VGA $3C6)
  3. Write RMR with value for CR
  4. Read address register

- **Procedure to read CR**
  1. Read address register (VGA $3C8)
  2. Read RMR five times (VGA $3C6)
  3. Results in CR contents
  4. Read address register

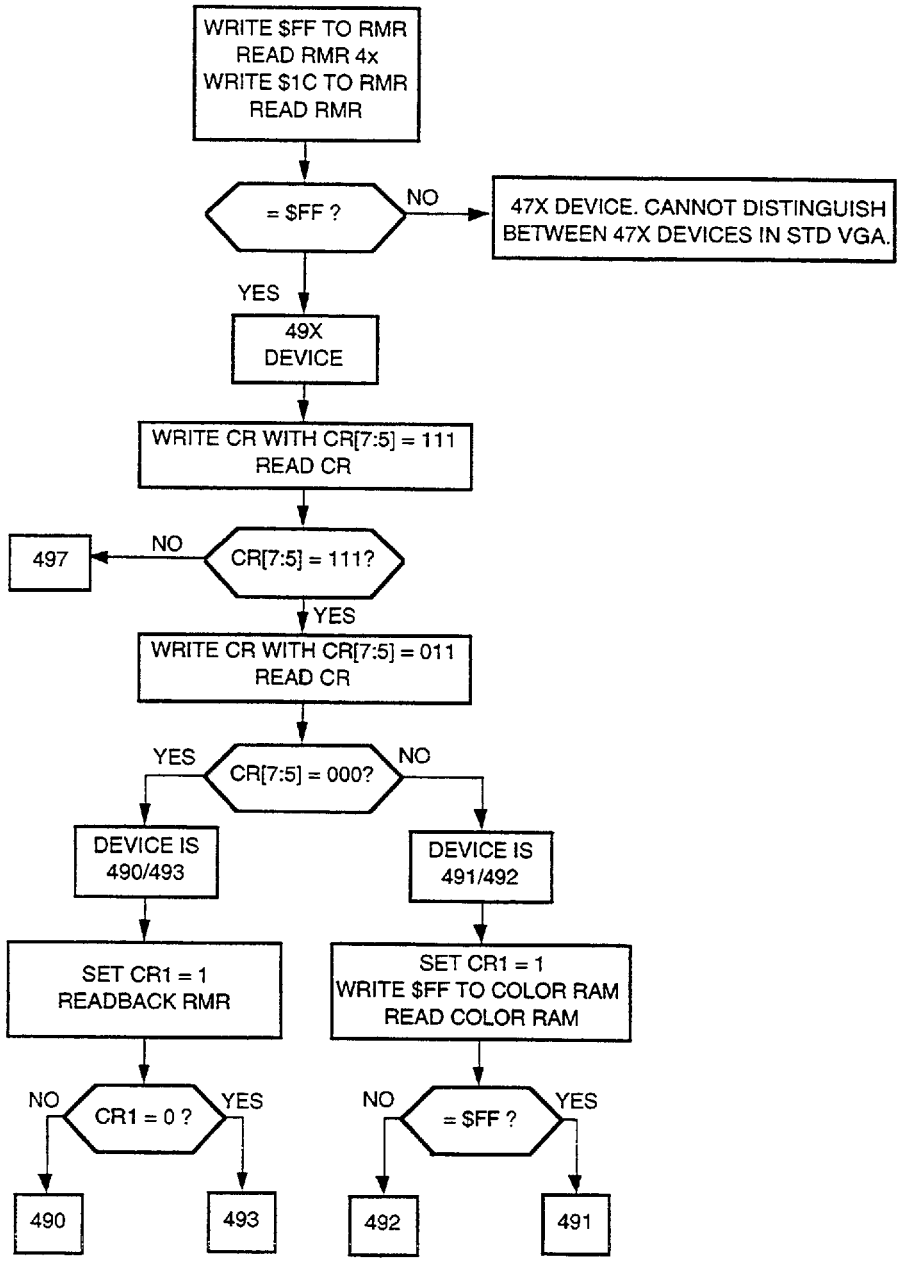


Figure 5. Software Indentification Flow Chart

Functional Description (continued)

MPU Interface

The ATT20C490/493 supports a standard MPU interface, allowing the MPU direct access to the RAMDAC color RAM, overlay RAM, or control register (see Figure 1). As outlined in Table 2, the RS[2:0] select inputs indicate whether the MPU is accessing the address register (ADDR), RAMDAC color RAM, overlay RAM, read mask register (RMR), or control register (CR). To eliminate the requirement for external address multiplexers, the 8-bit address register is used to address the RAMDAC color RAM and overlay registers. ADDR0 corresponds to D0 and is the least significant bit.

Writing the RAMDAC

The MPU writes the address register (RAM write mode) with the address of the RAMDAC color RAM location to be modified. Using RS[2:0] to select the RAMDAC color RAM, the MPU completes three continuous write cycles (6 bits or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the location specified by the address register. The address register advances to the next location, which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

Reading the RAMDAC

The MPU loads the address register (color RAM read mode) with the address of the RAMDAC color RAM location to be read. The contents of the RAMDAC color RAM at the specified address are copied into the RGB register, and the address register advances to the next RAM location. Using RS[2:0] to select the RAMDAC color RAM, the MPU completes three continuous read cycles (6 bits or 8 bits each of red, green, and blue). After the blue read cycle, the contents of the RAMDAC color RAM at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Writing the Overlay Registers

The MPU writes the address register (overlay RAM write mode) with the address of the overlay location to be modified. Using RS[2:0] to select the overlay registers, the MPU completes three continuous write cycles (6 bits or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the overlay location specified by the address register. The address register then advances to the next location, which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

Reading the Overlay Registers

The MPU loads the address register (overlay read RAM mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB register, and the address register advances to the next overlay RAM location. Using RS[2:0] to select the overlay registers, the MPU completes three continuous read cycles (6 bits or 8 bits each of red, green, and blue).

After the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Additional Information

Following a blue read or write cycle to RAM location $FF, the address register resets to $00. The four most significant bits of the address register ADDR[7:4] are ignored while accessing the overlay color RAM.

Functional Description (continued)

Additional Information (continued)

The MPU interface operates asynchronously to the pixel clock. Internal logic synchronizes data transfers between the RAMDAC color RAM, overlay color RAM, and the R, G, B color subregister. As a result, the WR and RD signals must maintain a logic high for several clock cycles. See Table 18 for RD and WR high time for further information. To eliminate sparkling on the CRT screen during MPU access to the RAMDAC RAMs, internal logic maintains the previous output color data on the analog outputs, while the transfer between look-up table RAMs and the RGB registers occurs.

To monitor the red, green, and blue read/write cycles, the address register has two additional bits (ADa, ADb) that count modulo three, as shown in Table 8. They are reset to 0 when the MPU writes to the address register and are not reset to 0 when the MPU reads the address register. The MPU does not have access to these bits.

The other 8 bits of the address register ADDR[7:0], incremented following a blue read or write cycle, are accessible to the MPU and are used to address RAMDAC color RAM locations and overlay color RAM, as outlined in Table 9.

The MPU can read the address register at any time without modifying its contents or the existing read/write mode. Note that the pixel clock must be active for MPU accesses to the RAMDAC RAM.

Table 8. Modulo 3 Counter Operation

AD[b:a]	Addressed by MPU
00	red color RAM byte
01	green color RAM byte
10	blue color RAM byte

Table 9. Address Register (ADDR) Operation

RS2	RS1	RS0	ADDR [7:0]	Addressed by MPU
0	0	1	$00—$FF	RAMDAC RAM
1	0	1	$X0	reserved
1	0	1	$X1	overlay color 1
:	:	:	:	:
1	0	1	$XF	overlay color 15

8-/$\overline{6}$-Bit Color Resolution

The 8/$\overline{6}$ pin and the 8/$\overline{6}$ bit (ATT20C490) in the control register (CR1) determine whether the MPU port reads and writes 8 bits or 6 bits of color data to the color look-up table RAM. The 8/$\overline{6}$ pin and the 8/$\overline{6}$ control register bit are logically ORed. In 6-bit mode, color data is on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logic 0. Note that in the 6-bit mode, the full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is a result of the two LSBs of each 8-bit DAC always being a logic 0 in the 6-bit mode. In the 8-bit color mode, bit D0 is the color data LSB and bit D7 is the MSB.

Pixel and Overlay Pins

Table 10 outlines how the P[7:0] and OL[3:0] inputs address the RAMDAC color RAM and overlay color RAM. The contents of the pixel read mask register can be accessed by the MPU at any time and are bitwise logically ANDed with the P[7:0] inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The address pointed to by the pixel data provides 18 bits of color information to the three DACs in the 6-bit mode and 24 bits in the 8-bit mode.

To maintain synchronization with color data, the rising edge of the clock latches the SYNC and BLANK inputs. SYNC and BLANK add appropriately weighted currents to the analog outputs to produce the SYNC and BLANK pedestal currents as shown in Figures 6, 7, and 8 and Tables 12, 13, and 14.

The analog outputs are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

Table 10. Pixel and Overlay Control Truth Table

OL[3:0]	P[7:0]	Addressed by Frame Buffer
$0	$00	color RAM location $00
$0	$01	color RAM location $01
:	:	:
$0	$FF	color RAM location $FF
$1	$XX	overlay RAM color 1
:	$XX	:
$F	$XX	overlay RAM color 15

Functional Description (continued)

Powerdown

The SLEEP control bit, CR0, controls the powerdown. The device operates normally while the SLEEP bit is a logic 0. A logic 1 in the control register SLEEP bit turns off power to the RAM and the DACs. The RAM still retains the data and can still be read or written to while sleeping, as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is completed.

The ATT20C490/493 disables all references both internal and external to the device, preventing current from flowing out of the device during powerdown. The internal reference disable circuitry eliminates the need for external disable logic and allows minimum power dissipation during sleep mode, regardless of the referencing scheme used.

$\overline{\text{SENSE}}$ Output

$\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level (340 mV). This output is used to determine the presence of a CRT monitor, and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned.

The range is 280 mV to 380 mV with a nominal value of 340 mV. Note that $\overline{\text{SYNC}}$ should be a logic 0 for $\overline{\text{SENSE}}$ to be stable. When using the ATT20C490/493 in a socket of an earlier, compatible device, make sure that the $\overline{\text{SENSE}}$ pin is not tied to power or ground.

DAC Gain

The device gain from the voltage reference to the DAC output current is shown below. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula below. V_{REF} is the voltage reference in volts, K is the gain constant from Table 9, and RSET is the resistor connected between the RSET pin and ground. Find the recommended RSET in Table 11.

I_{OUT} (mA) = [V_{REF} (V) * 1,000 * K] / RSET (Ω)

In this case, a voltage reference of 1.235 V with RSET = 147 Ω and a K factor of 3.17 results in I_{OUT} = 26.63 mA. A 6-bit DAC with no sync or blank results in a K factor of 2.1 and I_{OUT} = 17.64 mA.

As shown in Table 11, the recommended RSET for RS-343A compatibility applications (doubly terminated 75 Ω) is 147 Ω. The recommended RSET for *PS/2* applications (50 Ω) is 182 Ω.

Table 11. I_{OUT} Current

Output Waveform Level	RS-343A	*PS/2*	K Factor
Black to White (6 bit)	17.6 mA	14.25 mA	2.1
Black to White (8 bit)	17.6 mA	14.25 mA	2.125
Black to $\overline{\text{BLANK}}$	1.4 mA	—	0.1667
$\overline{\text{BLANK}}$ to $\overline{\text{SYNC}}$	7.6 mA	6.1 mA	0.9
Recommended RSET	147 Ω	182 Ω	—

Functional Description (continued)

DAC Gain (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

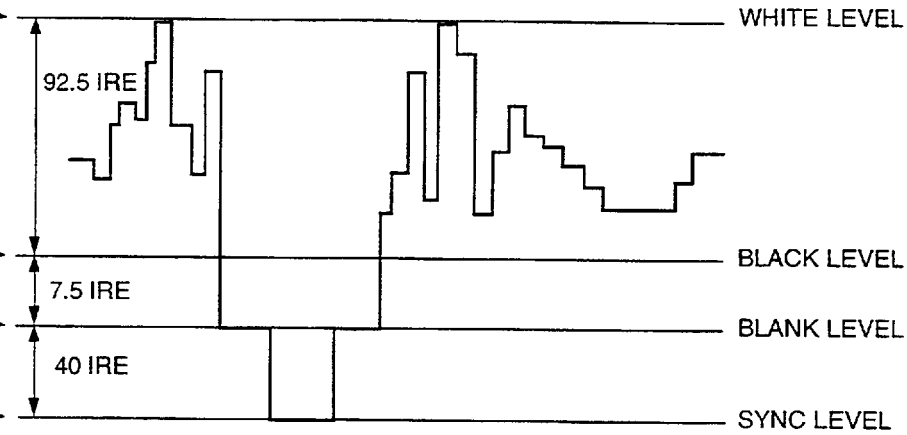


Figure 6. RS-343A Composite Video Output Waveforms

Table 12. RS-343A Video Output Truth Table (blank offset current to equal 7.5 IRE)

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA) $\overline{\text{SYNC}}$ Disabled	I_{OUT} (mA) $\overline{\text{SYNC}}$ Enabled
$FF	1	1	WHITE	19.05	26.67
data	1	1	DATA	data + 1.44	data + 9.05
data	0	1	DATA- $\overline{\text{SYNC}}$	data + 1.44	data + 1.44
$00	1	1	BLACK	1.44	9.05
$00	0	1	BLACK- $\overline{\text{SYNC}}$	1.44	1.44
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. V_{REF} = 1.235 V, RSET = 147 Ω.

Functional Description (continued)

DAC Gain (continued)

NO SYNC		SYNC	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000

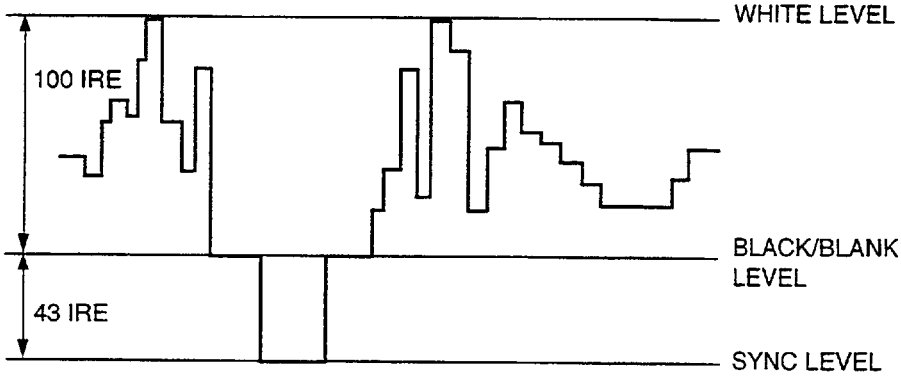


Figure 7. RS-343A Composite Video Output Waveforms

Table 13. RS-343A Video Output Truth Table (no blank offset current)

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA) $\overline{\text{SYNC}}$ Disabled	I_{OUT} (mA) $\overline{\text{SYNC}}$ Enabled
$FF	1	1	WHITE	17.62	25.24
data	1	1	DATA	data	data + 7.62
data	0	1	DATA- $\overline{\text{SYNC}}$	data	data
$00	1	1	BLACK	0	7.62
$00	0	1	BLACK- $\overline{\text{SYNC}}$	0	0
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. V_{REF} = 1.235 V, RSET = 147 Ω.

Functional Description (continued)

DAC Gain (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000

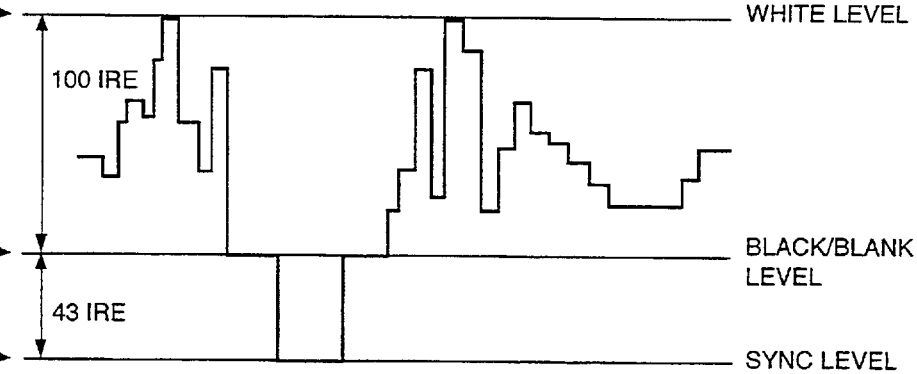


Figure 8. *PS/2* Composite Video Output Waveforms

Table 14. *PS/2* Video Output Truth Table

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	$\overline{\text{SYNC}}$ Disabled I_{OUT} (mA)	$\overline{\text{SYNC}}$ Enabled I_{OUT} (mA)
$FF	1	1	WHITE	14.25	20.36
data	1	1	DATA	data	data + 6.11
data	0	1	DATA- $\overline{\text{SYNC}}$	data	data
$00	1	1	BLACK	0	6.11
$00	0	1	BLACK- $\overline{\text{SYNC}}$	0	0
$XX	1	0	$\overline{\text{BLANK}}$	0	6.11
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 50 Ω load, SETUP = 0 IRE. V_{REF} = 1.235 V, RSET = 182 Ω.

Application Information

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This also helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

A four-layer PC board with separate power and ground planes will likely result in a board with quieter signals and supplies as well as less spectral content in emitted frequency bands. The board should have signal layers 1 and 4 (outside layers) and supply layers 2 and 3 (inside layers). Use a solid ground plane for frequencies up to 100 MHz.

The ATT20C490/493 should be placed close to the video output connector and between the video output connector and the edge card connector. This will keep the high-speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

Power Distribution

Separate the power plane into digital and analog areas. Place all digital components over the digital plane and all analog components over the analog plane. The analog components include the RAMDAC, reference circuitry, comparators, all mixed signal chips (such as a clock synthesizer), and any passive support components for analog circuits.

The analog and digital power plane should be connected with at least one ferrite bead across the separation, as illustrated in Figures 9 and 10. This bead provides resistance to high-frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The ferrite should have a resistance at a higher frequency than the maximum signal frequency on the board, but lower than the second harmonic (2x) of that frequency. The following beads provide resistances of approximately 75 Ω at 100 MHz: Ferroxcube VK20019-4B, Fair-Rite 2743001111, or Philips 431202036690.

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 in. of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads will work. Keep lead lengths as short as possible to reduce inductance and EMI. For leaded capacitors, use devices with a self-resonance above the pixel clock frequency.

For the ATT20C490/493, decouple Vcc pin 4 to ground with a 0.01 µF capacitor. Decouple Vcc pins 20—22 to ground with a 0.01 µF capacitor. For higher-frequency pixel clocks (>80 MHz), use a 0.01 µF capacitor in parallel with the 0.1 µF capacitor to shunt the higher-frequency noise to ground. Power supply noise should be less than 200 mV for a good design. About 10% of any noise below 1 MHz will be coupled onto the DAC outputs. As illustrated in Figures 9 and 10, the COMP pin should also be decoupled with a 0.1 µF capacitor. For designs showing ghosting or smearing, add a parallel COMP capacitance of 2.2 µF.

Digital Signals

The digital inputs should not travel over the analog power plane if possible. The RAMDAC should be located over the analog plane close to the digital/analog supply separation. The RAMDAC may also be placed over the supply separation so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the P[7:0] high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew rate edges since they can contribute to undershoot, overshoot, ringing, EMI, and noise feedthrough. Wherever possible, use slower edge rate (3 ns—5 ns) logic such as 74S or 74ALS devices. If this is not possible, edges can be slowed down by using series termination (75 Ω to 150 Ω). Edge noise will result if the digital signal propagates from an impedance mismatch while the signal rises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2 ns edge, the trace length must be less than 4 in.

Application Information (continued)

Digital Signals (continued)

The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high-frequency noise components, decouple the supply pins on the clock driver. If necessary, transmission line techniques should be used on the clock by providing controlled impedance striplines and parallel termination.

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination which is usually a 75 Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector.

Series ferrite beads can be added to the analog video signal to reduce high-frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace can be added to the ground plane or signal layer. This trace connects directly to the point where ground enters the card.

DAC Outputs

The ATT20C490/493 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac-coupled monitors.

The diode protection circuit shown in Figures 9 and 10 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes.

Application Information (continued)

DAC Outputs (continued)

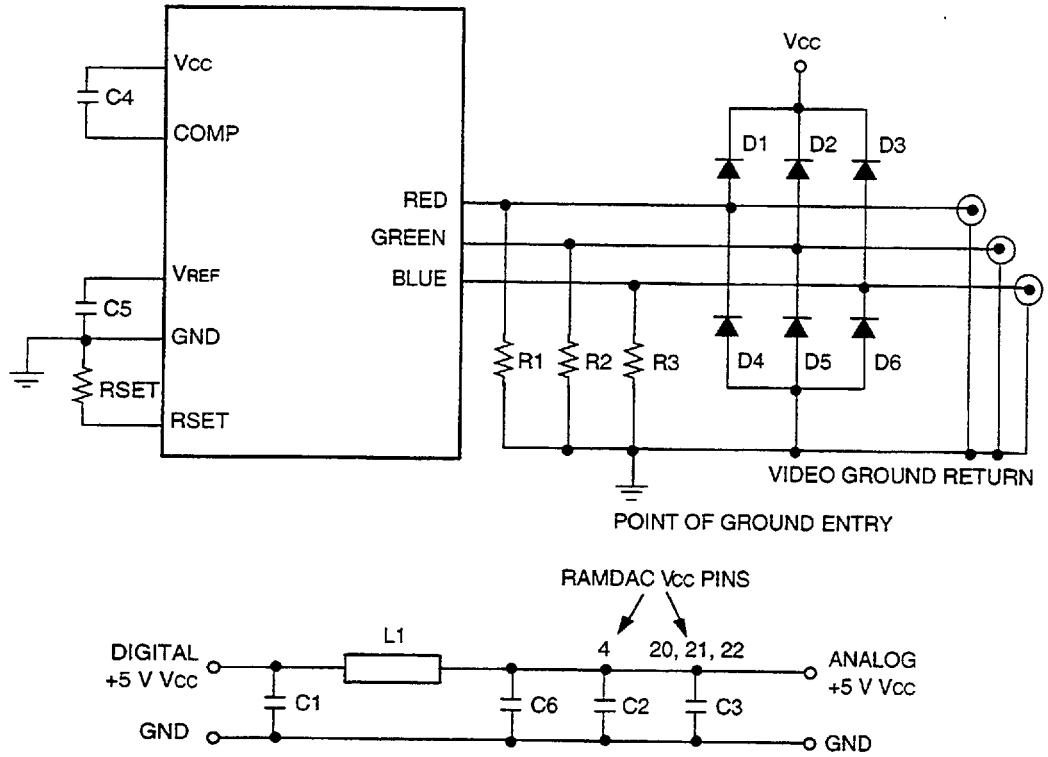


Figure 9. Typical Connection Diagram Using the Internal Voltage Reference

Table 15. Internal Voltage Reference Parts List

Location	Description	Vendor Part Number
C1—C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1—R3	75 Ω, 1% metal film resistor	Dale CMF-55C
RSET	147 Ω, 1% metal film resistor	Dale CMF-55C
D1—D6	Fast-switching diodes	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C490/493.

Application Information (continued)

DAC Outputs (continued)

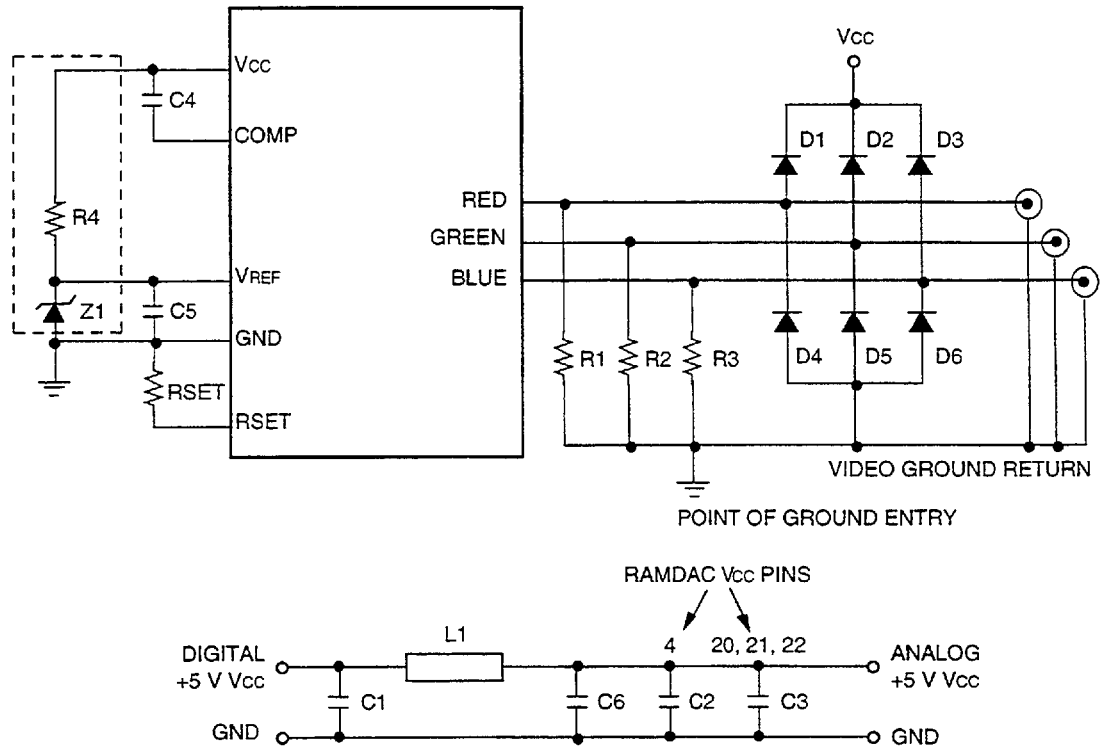


Figure 10. Typical Connection Diagram Using an External Voltage Reference

Table 16. External Voltage Reference Parts List

Location	Description	Vendor Part Number
C1—C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1—R3	75 Ω, 1% metal film resistor	Dale CMF-55C
R4	1 kΩ, 5% resistor	—
RSET	147 Ω, 1% metal film resistor	Dale CMF-55C
Z1	1.2 voltage reference	National Semiconductor LM385BZ-1.2
D1—D6	Fast-switching diodes	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C490/493.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
Vcc (measured to GND)	—	—	—	7.0	V
Voltage on Any Digital Pin	—	GND – 0.5	—	Vcc + 0.5	V
Analog Output Short Circuit: Duration to Any Power Supply or Common	ISC	—	Indefinite	—	—
Ambient Operating Temperature	T_A	–55	—	125	°C
Storage Temperature	T_{stg}	–65	—	150	°C
Junction Temperature	T_J	—	—	150	°C
Vapor Phase Soldering (60 s)	TV_{SOL}	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.75	5.00	5.25	V
Ambient Operating Temperature	T_A	0	—	70	°C
Output Load	R_L	—	37.5	—	Ω
Reference Voltage	V_{REF}	1.2	1.235	1.27	V

Electrical Characteristics

Table 17. dc Characteristics

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Digital Inputs:					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.8	V
High	V_{IH}	2.0	—	V_{CC} + 0.5	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{IL}	—	—	–1	µA
High (V_{IN} = 2.4 V)	I_{IH}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}	—	—	7	pF
Digital Outputs:					
Output Voltage:					
Low (I_{OL} = 3.2 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –400 µA)	V_{OH}	2.4	—	—	V
3-State Current	I_{OZ}	—	—	50	µA
Capacitance	C_{DOUT}	—	—	7	pF

Electrical Characteristics (continued)

Table 17. dc Characteristics (continued)

Test conditions generate RS-343A video signals unless otherwis- ⁻. The re- ₋ ended operating condi- tion for generating test signals is RSET = 147 Ω, VREF = 1.235 V. 7.5 IRE, .. 6 pin = logic 1. The parameters below are applicable over full voltage and temperatur shown ir the Recommended Operating Conditions table.

Parameter	Symbol	Min		Max	Unit
Resolution (each DAC):	—	6		8	bits
Accuracy (each DAC):					
Integral Linearity Error:	IL				
(each DAC, 6-bit mode)	—	—	—	±1/4	LSB
(each DAC, 8-bit mode)	—	—	—	±1	LSB
Differential Linearity Error:	DL				
(each DAC, 6-bit mode)	—	—	—	±1/4	LSB
(each DAC, 8-bit mode)	—	—	—	±1	LSB
Gain Error	—	—	—	±5	%
Monotonicity	—	—	Guaranteed	—	Scale
Coding	—	—	—	—	Binary
Analog Outputs:					
Gray Scale Current Range	Igray	—	—	20	mA
Output Current:					
White Level Relative to Black	Iwb	16.74	17.62	18.5	mA
Black Level Relative to Blank:	Ibb				
Setup = Logic High	—	0.95	1.44	1.90	mA
Setup = Logic Low	—	0	5	50	µA
Blank Level:	Iblank				
Sync Enabled	—	6.29	7.62	8.96	mA
Sync Disabled	—	0	5	50	µA
Sync Level	Isync	0	5	50	µA
LSB Size:	Ilsb				
6-bit DACs	—	—	69.1	—	µA
8-bit DACs	—	—	279.68	—	µA
DAC to DAC Matching	—	—	2	5	%
Output Compliance	VOC	–0.5	—	1.5	V
Output Impedance	RAOUT	—	10	—	kΩ
Output Capacitance	CAOUT	—	—	30	pF
(f = 1 MHz, IOUT = 0 mA)					
Internal Reference Output (±3%)	VREF	1.2		1.27	V
SENSE Trip Level	VSEN	—		—	mV
Power Supply Rejection Ratio:	PSRR	—			%/% ΔVcc
(COMP = 0.1 F, f = 1 kHz)	—	—			dB

Electrical Characteristics (continued)

Table 18. ac Characteristics

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, 8/6 = logic 1. Timing reference points are 50% for both inputs and outputs. The analog output load is ≤10 pF; SENSE and D[7:0] output loads are ≤50 pF. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

		110 MHz Devices			100 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	110	—	—	100	MHz
RS[2:0] Setup Time	1	10	—	—	10	—	—	ns
RS[2:0] Hold Time	2	10	—	—	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—	—	5	—	—	ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	40	—	—	40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	—	—	20	ns
Read Data Hold Time	6	5	—	—	5	—	—	ns
Write Data Setup Time	7	10	—	—	10	—	—	ns
Write Data Hold Time	8	10	—	—	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50	—	—	50	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	6	—	—	PCLK
Pixel and Control Setup Time	12	2	—	—	2	—	—	ns
Pixel and Control Hold Time	13	2	—	—	2	—	—	ns
Clock Cycle Time (PCLK)	14	9.1	—	—	10	—	—	ns
Clock Pulse Width High Time	15	3.6	—	—	4	—	—	ns
Clock Pulse Width Low Time	16	3.6	—	—	4	—	—	ns
Analog Output Delay	17	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	—	—	2	—	—	3	—	ns
Analog Output Settling Time*	—	—	20	—	—	20	—	ns
Clock and Data Feedthrough*	—	—	–30	—	—	–30	—	dB
Glitch Impulse*	—	—	75	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	–23	—	—	–23	—	dB
Analog Output Skew	—	—	—	2	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	—	1	—	µs
Pipeline Delay	—	4	4	4	4	4	4	Clocks
Vcc Supply Current† Normal Operation	Icc	—	140	200	—	130	190	mA
Sleep Mode‡	ISLP							
PCLK = 1 MHz	—	—	3	—	—	3	—	mA
PCLK = 35 MHz	—	—	5	—	—	5	—	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, Icc (typ) at Vcc = 5.0 V Icc (max) at Vcc (max).

‡ External current or voltage reference automatically disabled during sleep mode. Test conditions: 25 °C to 70 °C. Pixel and data ports at 0.4 V.

Electrical Characteristics (continued)

Table 18. ac Characteristics (continued)

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, 8/6 = logic 1. Timing reference points are 50% for both inputs and outputs. The analog output load is ≤10 pF; SENSE and D[7:0] output loads are ≤50 pF. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

		80 MHz Devices			66 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	80	—	—	66	MHz
RS[2:0] Setup Time	1	10	—	—	10	—	—	ns
RS[2:0] Hold Time	2	10	—	—	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—		5	—	—	ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	40	—	—	40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	—	—	20	ns
Read Data Hold Time	6	5	—	—	5	—	—	ns
Write Data Setup Time	7	10	—	—	10	—	—	ns
Write Data Hold Time	8	10	—	—	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50	—	—	50	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	6	—	—	PCLK
Pixel and Control Setup Time	12	3	—	—	3	—	—	ns
Pixel and Control Hold Time	13	3	—	—	3	—	—	ns
Clock Cycle Time (PCLK)	14	12.5	—	—	15.5	—	—	ns
Clock Pulse Width High Time	15	5	—	—	6	—	—	ns
Clock Pulse Width Low Time	16	5	—	—	6	—	—	ns
Analog Output Delay	17	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	—	—	3	—	—	3	—	ns
Analog Output Settling Time*	—	—	20	—	—	20	—	ns
Clock and Data Feedthrough*	—	—	–30	—	—	–30	—	dB
Glitch Impulse*	—	—	75	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	–23	—	—	–23	—	dB
Analog Output Skew	—	—	—	2	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	—	1	—	µs
Pipeline Delay	—	4	4	4	4	4	4	Clocks
Vcc Supply Current† Normal Operation	Icc	—	120	180	—	110	170	mA
Sleep Mode‡	ISLP							
PCLK = 1 MHz	—	—	3	—	—	3	—	mA
PCLK = 35 MHz	—	—	5	—	—	5	—	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, Icc (typ) at Vcc = 5.0 V Icc (max) at Vcc (max).

‡ External current or voltage reference automatically disabled during sleep mode. Test conditions: 25 °C to 70 °C. Pixel and data ports at 0.4 V.

Timing Characteristics

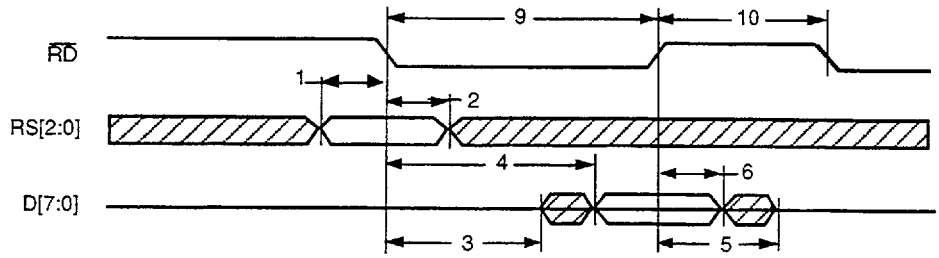


Figure 11. Basic Read-Cycle Timing Diagram

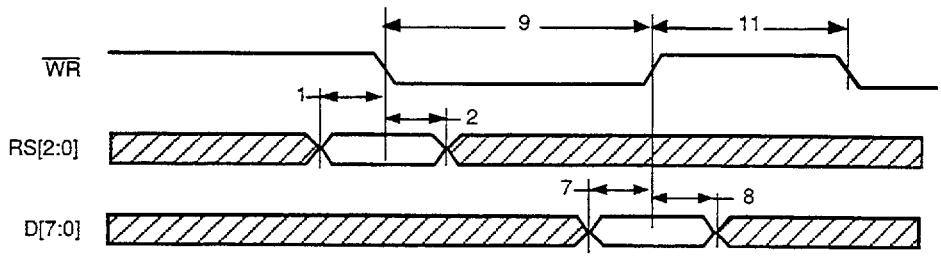


Figure 12. Basic Write-Cycle Timing Diagram

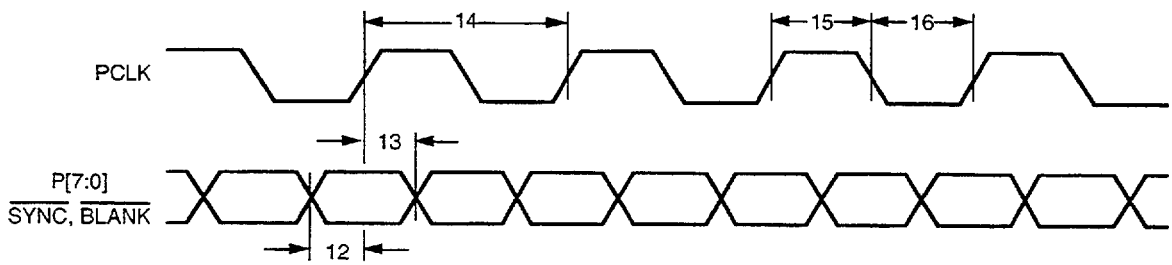


Figure 13. Pixel Timing

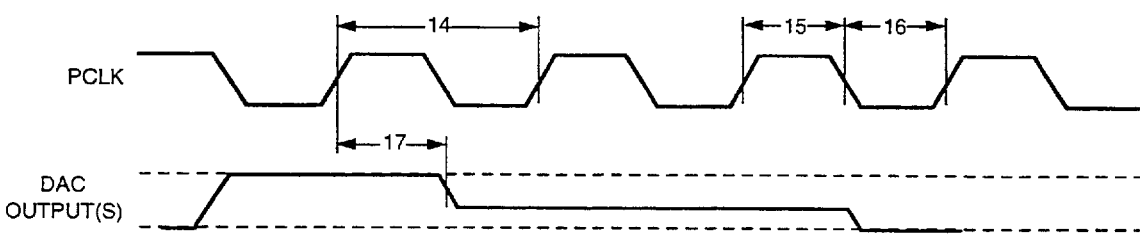
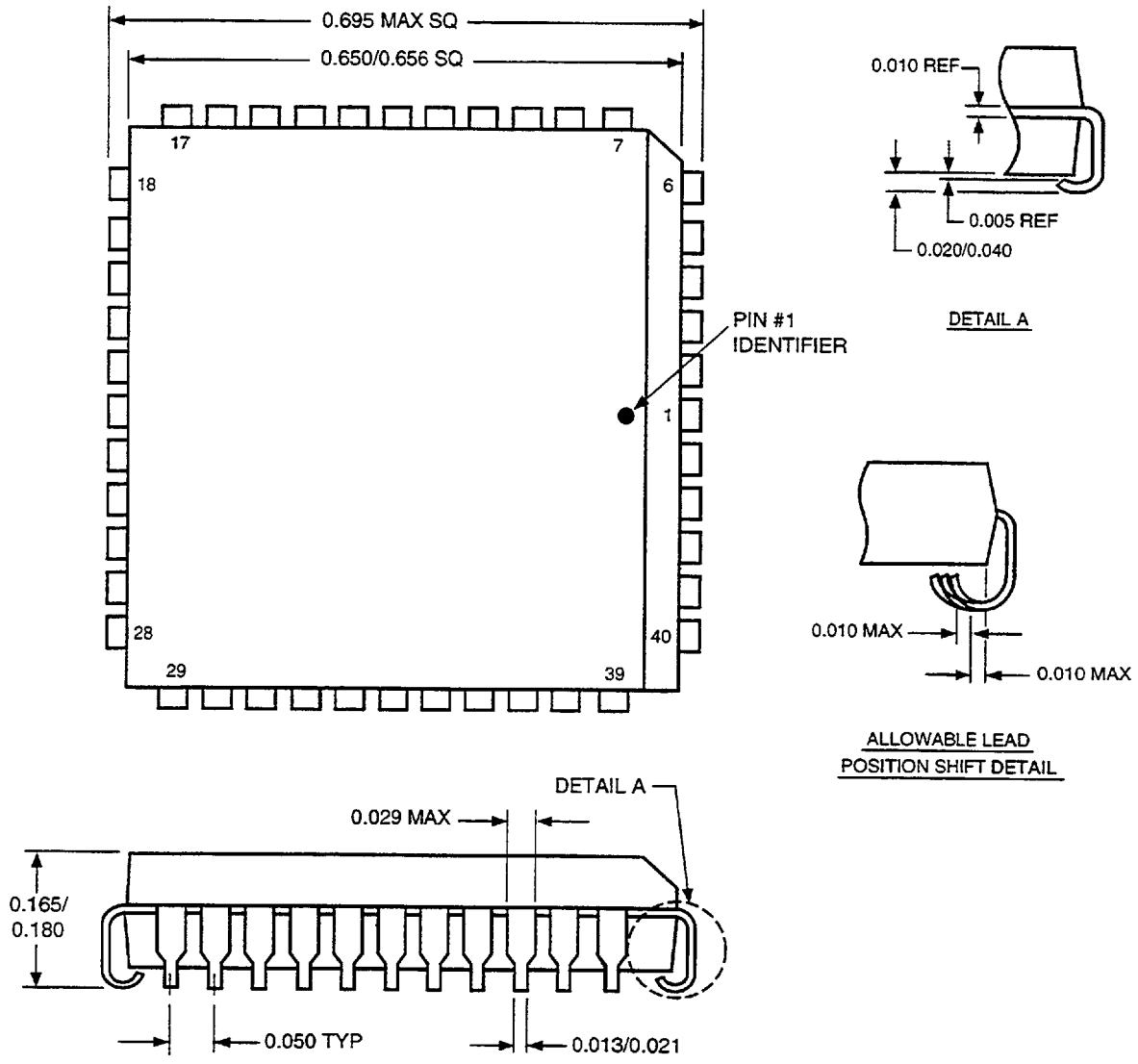


Figure 14. Video Timing

Outline Diagram

44-Pin PLCC Package

Dimensions are in inches.



Ordering Information

Device*	Speed	Package Type
ATT20C490-XXM44	110/100/80/66 MHz	44-Pin PLCC
ATT20C493-XXM44	110/100/80/66 MHz	44-Pin PLCC

* XX refers to speed grade:
11 = 110 MHz
10 = 100 MHz
80 = 80 MHz
66 = 66 MHz