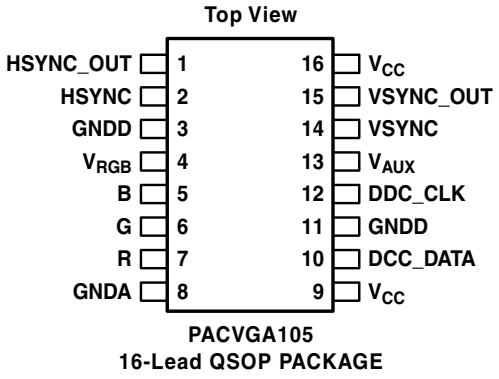
VGA Port Companion Circuit

Features

- 7 channels of ESD protection designed to meet IEC-1000-4-2 Level-4 ESD requirements (8KV contact discharge)
- Very low loading capacitance from ESD protection diodes, < 5pF typical
- TTL to CMOS level-translating buffers for the HSYNC and VSYNC lines
- Three independent supply pins (V_{CC}, V_{RGB} and V_{AUX}) to facilitate operation with sub-micron Graphics Controller ICs
- High impedance pull-ups (50KΩ nominal to V_{AUX}) for HSYNC & VSYNC inputs
- Pull-up resistors (1.8KΩ nominal to V_{CC}) for DDC_CLK and DDC_DATA lines
- Compact 16-pin QSOP package

Pin Diagram



PACVGA105
16-Lead QSOP PACKAGE

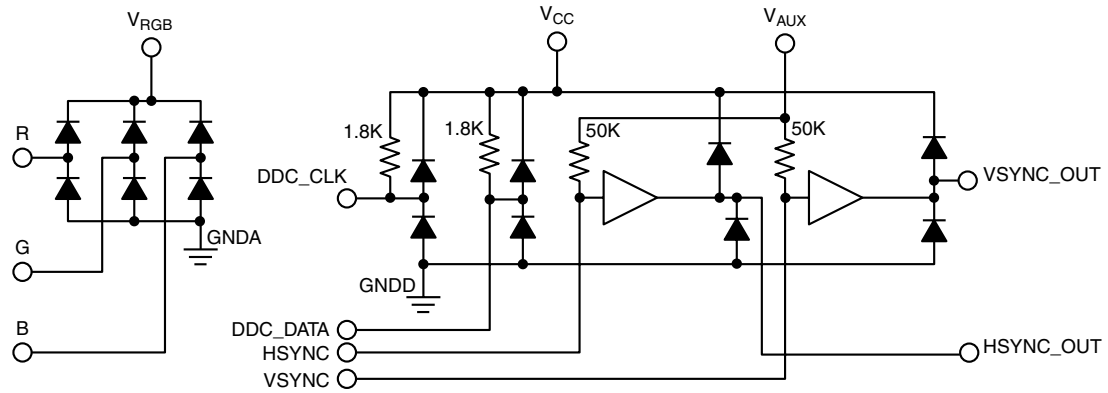
Product Description

The PACVGA105 incorporates 7 channels of ESD protection for signal lines commonly found in a VGA port for PCs. ESD protection is implemented with current steering diodes designed to safely handle the high peak surge currents associated with the IEC-1000-4-2 Level-4 ESD Protection Standard (8KV contact discharge). When the channels are subjected to an electrostatic discharge, the ESD current pulse is diverted via the protection diodes into the positive supply rails or ground where they may be safely dissipated.

The upper ESD diodes for the R, G & B channels are connected to a separate supply rail (V_{RGB}) to facilitate interfacing to graphics controller ICs with low voltage supplies. The remaining channels are connected to the main 5V rail (V_{CC}). The lower diodes for the R, G & B channels are also connected to a dedicated ground pin (GNDA) to minimize crosstalk due to common ground impedance.

Two non-inverting buffers are also included in this IC for buffering the HSYNC and VSYNC signals from the graphics controller IC. These buffers will accept TTL input levels and convert them to CMOS output levels that swing between GND and V_{CC}. These drivers have a nominal 60Ω output impedance to match the characteristic impedance of the HSYNC and VSYNC lines of the video cables typically used. The inputs of these drivers also have high impedance pull-ups (50KΩ nom.) pulling up to the V_{AUX} rail. In addition, the DDC_CLOCK and DDC_DATA channels have 1.8KΩ pull-up resistors pulling these inputs up to the main 5V (V_{CC}) rail.

Schematic Diagram



C1780401

Absolute Maximum Ratings			
Parameter		**Rating**	**Unit**
V_{CC} Supply Voltage		GND–0.5, 6.0	V
V_{RGB} Supply Voltage		GND–0.5, 6.0	V
V_{AUX} Supply Voltage		GND–0.5, 6.0	V
Diode Forward Current (only one diode conducting at a time)		20	mA
DC Voltage at Inputs	R, G, B	GND –0.5, V_{RGB} +0.5	V
	HSYNC, VSYNC	GND –0.5, V_{AUX} +0.5	V
	DDC_CLK, DDC_DATA	GND –0.5, V_{CC} +0.5	V
Storage Temperature		–40 to 150	°C
Operating Ambient Temperature		0 to 70	°C
Package Power Dissipation		0.75	W

Recommended Operating Conditions					
Symbol	**Parameter**		**MIN**	**MAX**	**UNIT**
V_{CC}	Main Supply Voltage		4.5	5.5	V
V_{RGB}	RGB Supply Voltage		1.7	3.7	V
V_{AUX}	Auxiliary Supply Voltage		2.9	3.7	V
V_{IH}	Logic High Input Voltage (Note 1)		2.0		V
V_{IL}	Logic Low Input Voltage (Note 1)			0.8	V
V_I	Input Voltage	RGB	0	V_{RGB}	V
		HSYNC, VSYNC	0	V_{AUX}	V
		DDC_CLK, DDC_DATA	0	V_{CC}	V
I_{OH}	High Level Output Current (Note 1)			–8	mA
I_{OL}	Low Level Output Current (Note 1)			8	mA
T_A	Operating Free-Air Temperature		0	70	°C

Note 1: These parameters apply only to the HSYNC and VSYNC signals.

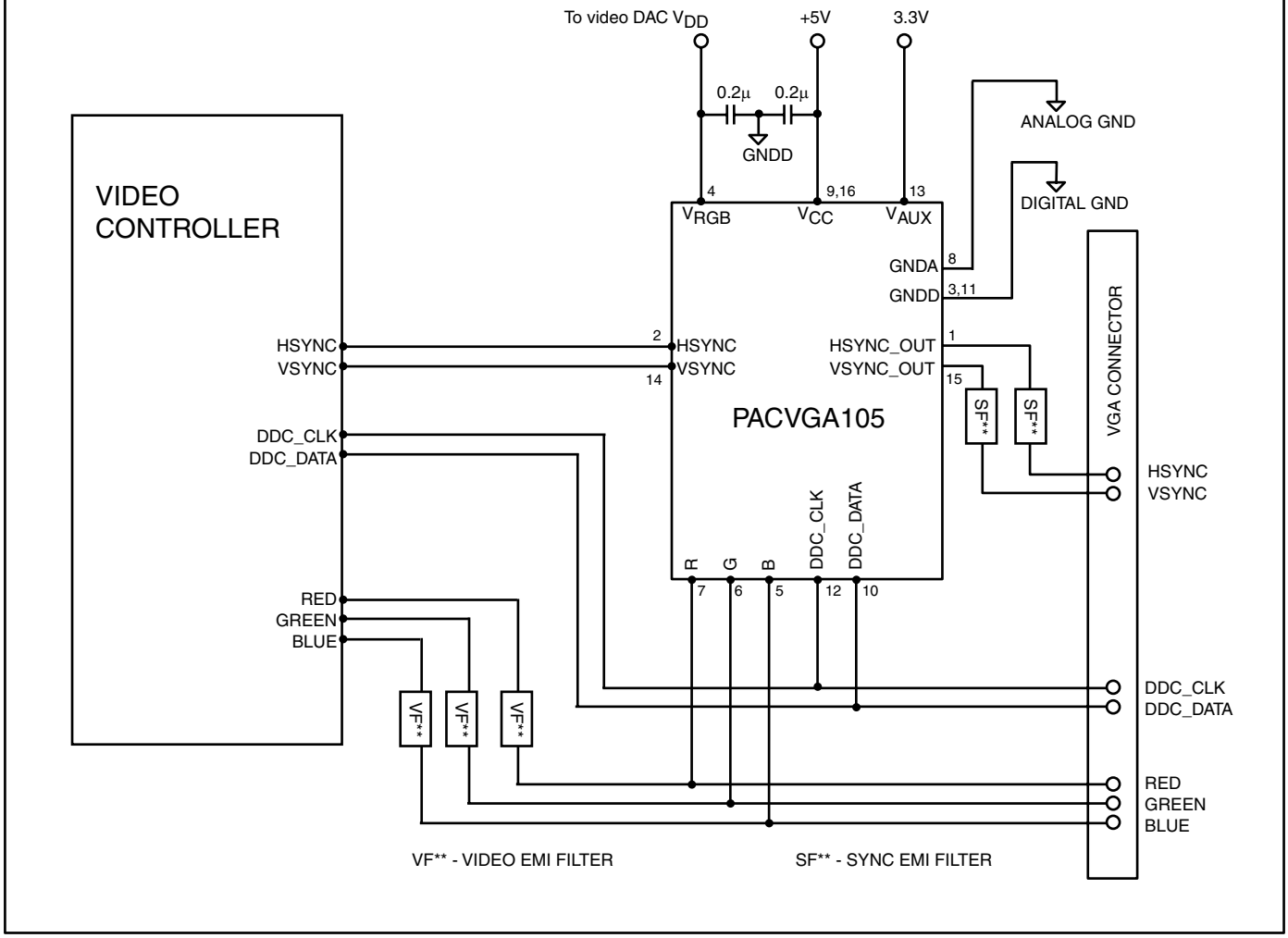
Electrical Characteristics at T_A = 25˚C						
Symbol	**Parameter**	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
V_F	Diode Forward Voltage	I_F = 10mA			1	V
V_{OH}	Logic High Output Voltage	I_{OH} = –4mA, V_{CC} = 4.5V	4.0			V
V_{OL}	Logic Low Output Voltage	I_{OL} = 4mA, V_{CC} = 4.5V			0.4	V
I_{IN}	Input Current	R, G, B pins; V_{RGB} = 3.63V; V_{IN} = V_{RGB} or GND			±1	µA
		HSYNC, VSYNC pins; V_{AUX} = 3.63V; V_{IN} = V_{AUX}			±1	µA
		HSYNC, VSYNC pins; V_{AUX} = 3.63V; V_{IN} = GND	–30	–72.5	–95	µA
I_{CC}	V_{CC} Supply Current	V_{CC} = 5.5V; V_{AUX} = V_{RGB} = 2.97V; All inputs and outputs floating		35	100	µA
I_{RGB}	V_{RGB} Supply Current	R, G, B pins at V_{CC} or GND; All other input and output floating			10	µA
C_{IN}	Input Capacitance	R,G, B (Note 1)		5		pF
		HSYNC, VSYNC (Note 1)		10		pF
		DDC_DATA, DDC_CLK (Note 1)		5		pF
R_{PU}	Pull-up Resistance	DDC_DATA, DDC_CLK	1.62	1.8	1.98	KΩ
V_{ESD}	ESD Withstand Voltage	V_{CC} = 5V; V_{RGB} = 3.3V; V_{AUX} = 3.3V; (Note 2)	±8			KV
t_{PLH}	L-H Propagation Delay	C_L = 50pF; V_{CC} = 5V; R_L = 500Ω; (Note 3)		7	15	ns
t_{PHL}	H-L Propagation Delay	C_L = 50pF; V_{CC} = 5V; R_L = 500Ω; (Note 3)		7	15	ns
t_R, t_F	Output Rise and Fall Time	C_L = 50pF; V_{CC} = 5V; R_L = 500Ω; (Note 3)		7		ns

Note 1: Measured at 1MHz. R/G/B inputs biased at 1.65V, with V_{RGB} = 3.3V. DDC_CLK and DDC_DATA biased at 2.5V, with V_{CC} = 5V. HSYNC and VSYNC inputs biased at V_{AUX} or GND, with V_{AUX} = 3.3V and V_{CC} = 5V. These parameters are guaranteed by design and characterization.

Note 2: Per the IEC-1000-4-2 ESD Standard, Level 4 contact discharge method. V_{RGB} and V_{CC} must each be bypassed to GND with a 0.2µF, low inductance, chip ceramic capacitor at the appropriate supply pin. This parameter is guaranteed by design and device characterization. ESD pulse is applied between the applicable pins and GND. ESD pulse can be positive or negative with respect to GND. Applicable pins are: R, G, B, HSYNC_OUT, VSYNC_OUT, DDC_CLK and DDC_DATA. The HSYNC and VSYNC inputs are ESD protected to the industry standard 2KV per the Human Body model (MIL-STD-883, Method 3015).

Note 3: Applicable to the SYNC buffers only. Input signals swing between 0V and 3.0V, with rise and fall times ≤ 5nS. Guaranteed by correlation to buffer output drive currents.

Typical Applications Diagram



GNDA, the negative voltage rail for the R,G,B diodes is not connected internally to GNDD. GNDA should ideally be connected to the ground of the video DAC IC. This will prevent any ground bounce caused by digital signals from injecting noise onto the R,G,B signals. Analog GND and digital GND will typically be connected on the pcb.

Standard Part Ordering Information

Package		Ordering Part Number
Pins	Style	Part Marking
16	QSOP	PACVGA105Q