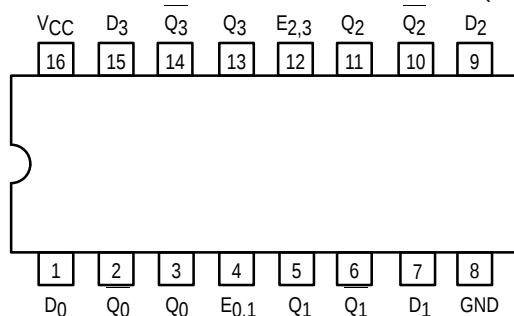




4-BIT D LATCH

The SN54/74LS375 is a 4-Bit D-Type Latch for use as temporary storage for binary information between processing limits and input/output or indicator units. When the Enable (E) is HIGH, information present at the D input will be transferred to the Q output and, if E is HIGH, the Q output will follow the input. When E goes LOW, the information present at the D input prior to its setup time will be retained at the Q outputs.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram) as
the Dual In-Line Package.

TRUTH TABLE
(Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

NOTES:
 t_n = bit time before enable
negative-going transition.
 t_{n+1} = bit time after enable
negative-going transition.

PIN NAMES

D ₁ –D ₄	Data Inputs
E ₀ –1	Enable Input Latches 0, 1
E ₂ –3	Enable Input Latches 2, 3
Q ₁ –Q ₄	Latch Outputs (Note b)
Q ₁ –Q ₄	Complimentary Latch Outputs (Note b)

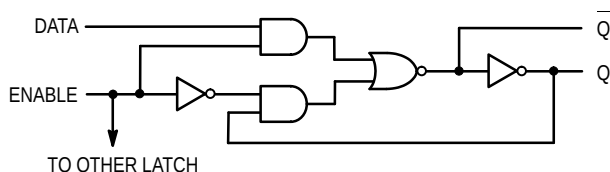
LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
2.0 U.L.	1.0 U.L.
2.0 U.L.	1.0 U.L.
10 U.L.	5 (2.5) U.L.
10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 25 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

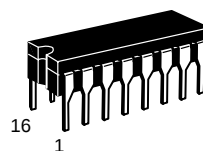
LOGIC DIAGRAM



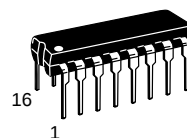
SN54/74LS375

4-BIT D LATCH

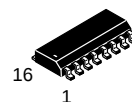
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

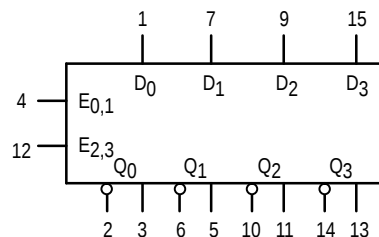


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS375

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V _{CC} = MIN, I _{IN} = −18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current	D Input E Input			20 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		D Input E Input			0.1 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current	D Input E Input			−0.4 −1.6	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				12	mA	V _{CC} = MAX	

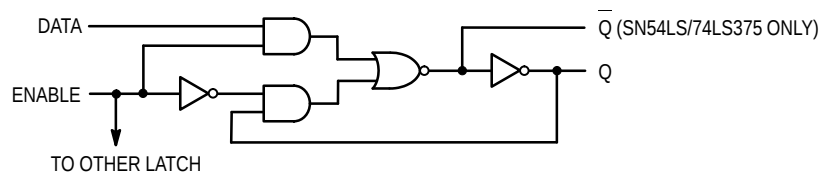
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t_{PLH} t_{PHL}	Propagation Delay, Data to Q			15 9.0	27 17	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$	
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Q}$			12 7.0	20 15	ns		
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q			15 14	27 25	ns		
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Q}$			16 7.0	30 15	ns		

SN54/74LS375

LOGIC DIAGRAM



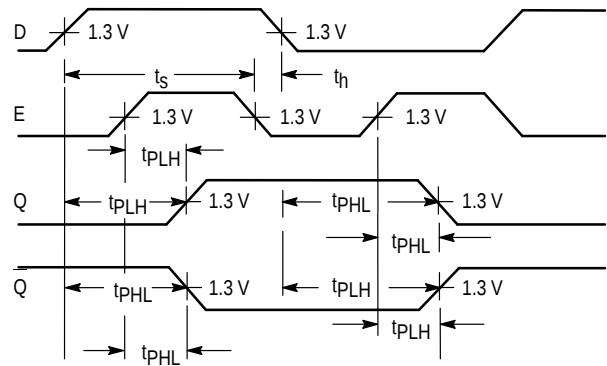
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Enable Pulse Width	20			ns	V _{CC} = 5.0 V
t _S	Setup Time	20			ns	
t _H	Hold Time	0			ns	

AC WAVEFORMS



DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following

the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.