

Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size
- Passivated Die for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Available in Two Package Styles
 - Surface Mount Lead Form — Case 369A
 - Miniature Plastic Package — Straight Leads — Case 369

ORDERING INFORMATION

- To Obtain "DPAK" in Surface Mount Leadform (Case 369A)
Shipped in 16 mm Tape and Reel — Add "T4" Suffix to Device Number, i.e. MCR8DCNT4
- To Obtain "DPAK" in Straight Lead Version (Case 369) Shipped in Sleeves —
Add "–1" Suffix to Device Number, i.e. MCR8DCN–1

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage ⁽¹⁾ Peak Repetitive Reverse Voltage ($T_J = -40$ to 125°C)	V_{DRM} V_{RRM}	600 800	Volts
On-State RMS Current (All Conduction Angles; $T_C = 105^\circ\text{C}$)	$I_{\text{T(RMS)}}$	8.0	Amps
Average On-State Current (All Conduction Angles; $T_C = 105^\circ\text{C}$)	$I_{\text{T(AV)}}$	5.1	
Peak Non-Repetitive Surge Current (One Half Cycle, 60 Hz, $T_J = 125^\circ\text{C}$)	I_{TSM}	80	
Circuit Fusing Consideration ($t = 8.3$ msec)	i^2t	26	A ² sec
Peak Gate Power (Pulse Width ≤ 10 μsec , $T_C = 105^\circ\text{C}$)	P_{GM}	5.0	Watts
Average Gate Power ($t = 8.3$ msec, $T_C = 105^\circ\text{C}$)	$P_{\text{G(AV)}}$	0.5	
Peak Gate Current (Pulse Width ≤ 10 μsec , $T_C = 105^\circ\text{C}$)	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	–40 to 125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	–40 to 150	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient ⁽²⁾	$R_{\theta\text{JC}}$ $R_{\theta\text{JA}}$ $R_{\theta\text{JA}}$	2.2 88 80	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes ⁽³⁾	T_L	260	$^\circ\text{C}$

(1) V_{DRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.

(2) Surface mounted on minimum recommended pad size.

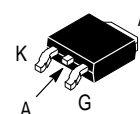
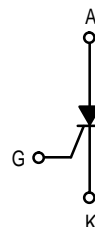
(3) 1/8" from case for 10 seconds.

Preferred devices are Motorola recommended choices for future use and best overall value.

MCR8DCM
MCR8DCN

Motorola Preferred Devices

SCRs
8.0 AMPERES RMS
600 thru 800 VOLTS



CASE 369A–13
STYLE 4



MCR8DCM MCR8DCN

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current Peak Reverse Blocking Current (V _{AK} = Rated V _{DRM} or V _{RRM} , Gate Open) T _J = 25°C T _J = 125°C	I _{DRM} I _{RRM}	— —	— —	0.01 5.0	mA
Peak On-State Voltage (1) (I _{TM} = 16 A)	V _{TM}	—	1.4	1.8	Volts
Gate Trigger Current (Continuous dc) (V _D = 12 V, R _L = 100 Ω, T _J = 25°C) (V _D = 12 V, R _L = 100 Ω, T _J = -40°C)	I _{GT}	2.0 —	7.0 —	15 30	mA
Gate Trigger Voltage (Continuous dc) (V _D = 12 V, R _L = 100 Ω, T _J = 25°C) (V _D = 12 V, R _L = 100 Ω, T _J = -40°C) (V _D = 12 V, R _L = 100 Ω, T _J = 125°C)	V _{GT}	0.5 — 0.2	0.65 — —	1.0 2.0 —	Volts
Holding Current (V _D = 12 V, I _T = 200 mA, T _J = 25°C) (V _D = 12 V, I _T = 200 mA, T _J = -40°C)	I _H	4.0 —	22 —	30 60	mA
Latching Current (V _D = 12 V, I _G = 15 mA, T _J = 25°C) (V _D = 12 V, I _G = 30 mA, T _J = -40°C)	I _L	4.0 —	22 —	30 60	mA

DYNAMIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Critical Rate of Rise of Off-State Voltage (V _D = Rated V _{DRM} , Exponential Waveform, Gate Open, T _J = 125°C)	dv/dt	50	200	—	V/μs

(1) Pulse Test; Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.

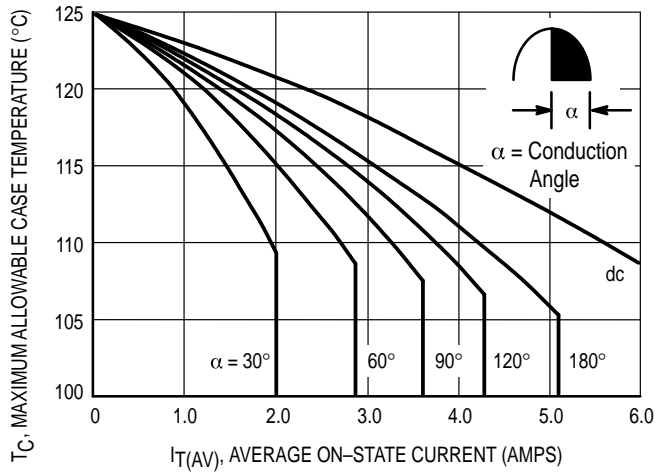


Figure 1. Average Current Derating

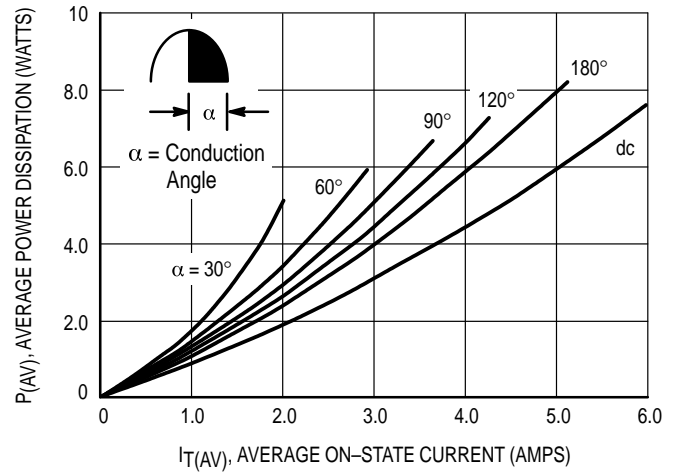


Figure 2. On-State Power Dissipation

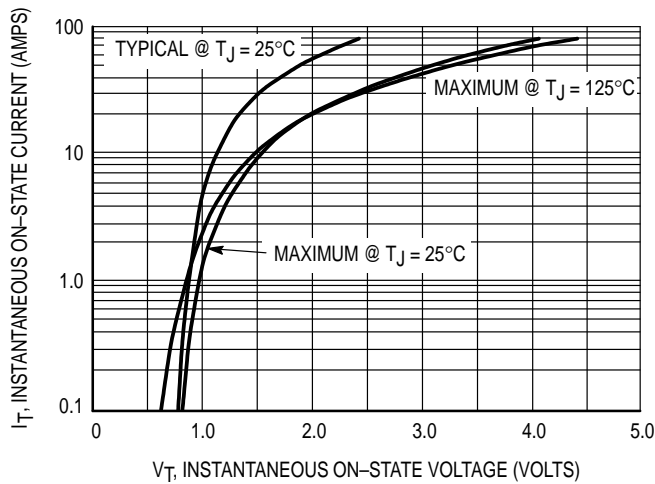


Figure 3. On-State Characteristics

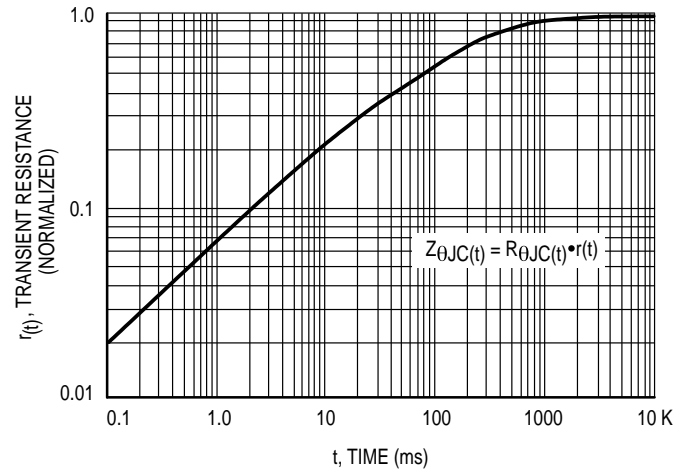


Figure 4. Transient Thermal Response

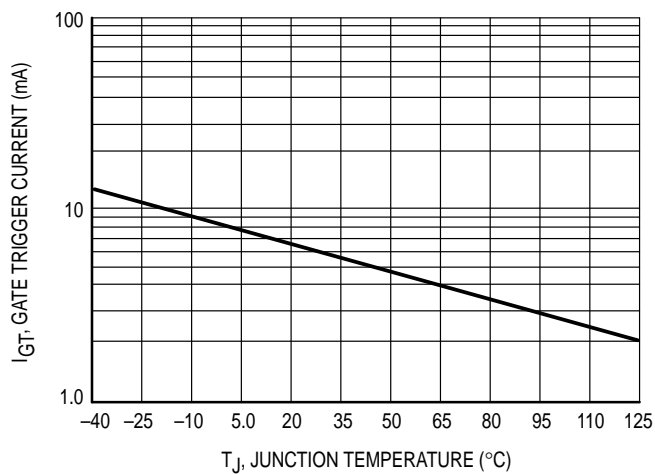


Figure 5. Typical Gate Trigger Current versus Junction Temperature

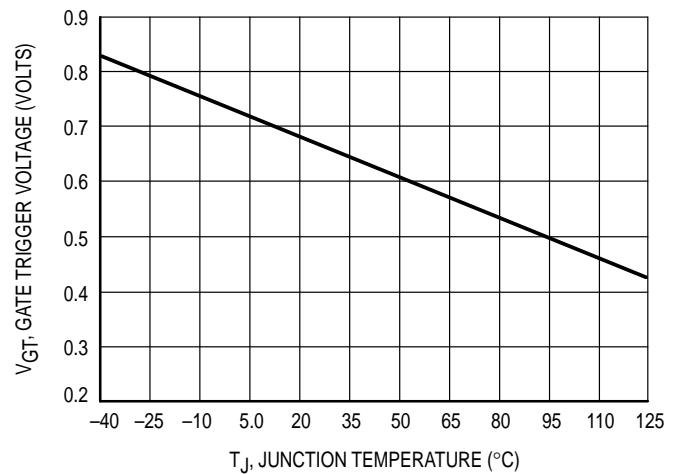


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

MCR8DCM MCR8DCN

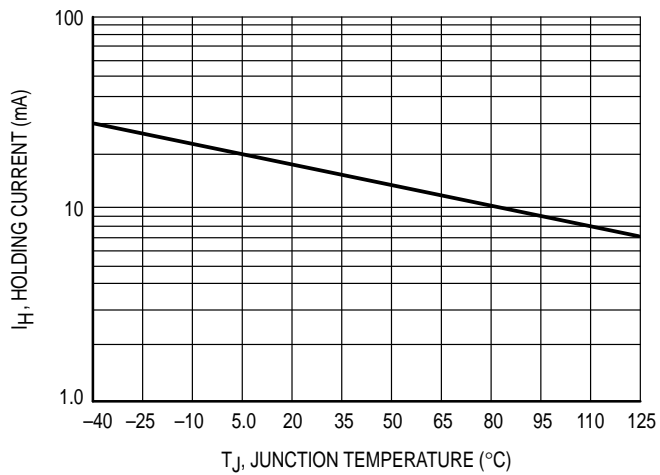


Figure 7. Typical Holding Current versus Junction Temperature

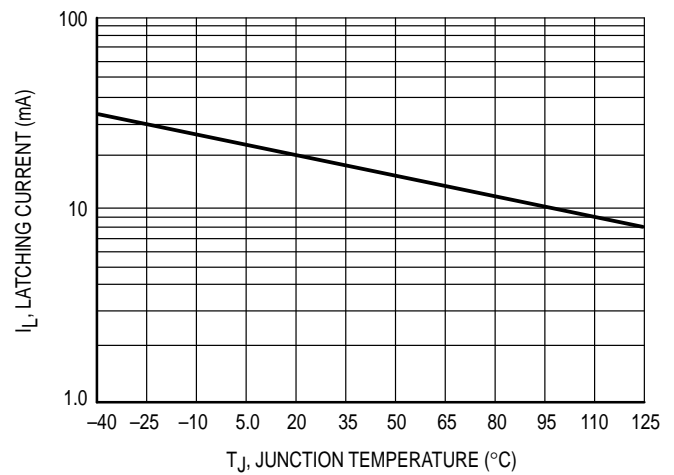


Figure 8. Typical Latching Current versus Junction Temperature

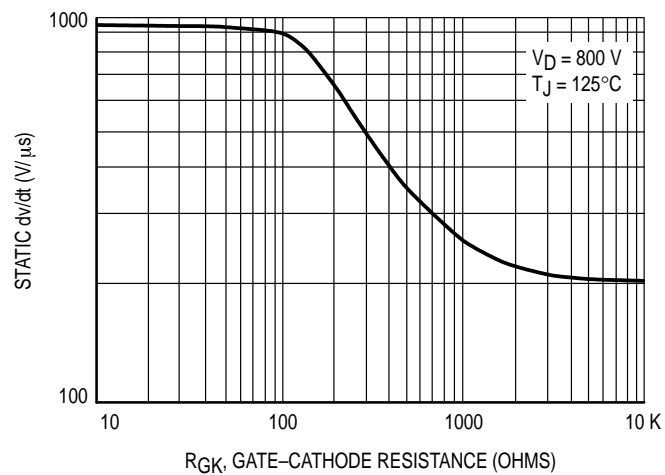
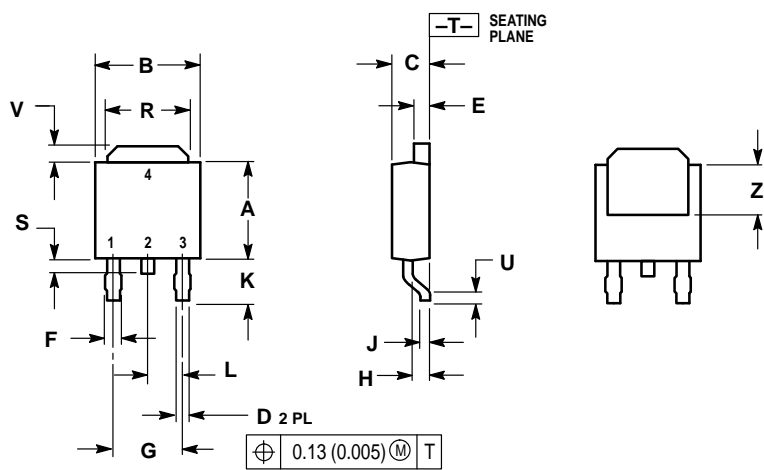


Figure 9. Exponential Static dv/dt versus Gate-Cathode Resistance

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

CASE 369A-13
ISSUE Y

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