

# MCR12DCM, MCR12DCN

Preferred Device

## Silicon Controlled Rectifiers

### Reverse Blocking Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size
- Passivated Die for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Device Marking: Logo, Device Type, e.g., R12DCN, Date Code

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage <sup>(1)</sup> ( $T_J = -40$ to $125^\circ\text{C}$ , Sine Wave, 50 to 60 Hz, Gate Open) MCR12DCM MCR12DCN	$V_{DRM}$ , $V_{RRM}$	600 800	Volts
On-State RMS Current ( $180^\circ$ Conduction Angles; $T_C = 90^\circ\text{C}$ )	$I_T(\text{RMS})$	12	Amps
Average On-State Current ( $180^\circ$ Conduction Angles; $T_C = 90^\circ\text{C}$ )	$I_T(\text{AV})$	7.6	Amps
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, $T_J = 125^\circ\text{C}$ )	$I_{TSM}$	100	Amps
Circuit Fusing Consideration ( $t = 8.3$ msec)	$I^2t$	41	$\text{A}^2\text{sec}$
Forward Peak Gate Power (Pulse Width $\leq 1.0$ $\mu\text{sec}$ , $T_C = 90^\circ\text{C}$ )	$P_{GM}$	5.0	Watts
Forward Average Gate Power ( $t = 8.3$ msec, $T_C = 90^\circ\text{C}$ )	$P_{G(\text{AV})}$	0.5	Watts
Forward Peak Gate Current (Pulse Width $\leq 1.0$ $\mu\text{sec}$ , $T_C = 90^\circ\text{C}$ )	$I_{GM}$	2.0	Amps
Operating Junction Temperature Range	$T_J$	$-40$ to $125$	$^\circ\text{C}$
Storage Temperature Range	$T_{\text{stg}}$	$-40$ to $150$	$^\circ\text{C}$

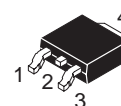
(1)  $V_{DRM}$  for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.



ON Semiconductor

<http://onsemi.com>

SCRs  
12 AMPERES RMS  
600 thru 800 VOLTS



D-PAK  
CASE 369A  
STYLE 4

#### PIN ASSIGNMENT

PIN ASSIGNMENT	
1	Cathode
2	Anode
3	Gate
4	Anode

#### ORDERING INFORMATION

Device	Package	Shipping
MCR12DCMT4	DPAK 369A	16mm Tape and Reel (2.5K/Reel)
MCR12DCNT4	DPAK 369A	16mm Tape and Reel (2.5K/Reel)

Preferred devices are recommended choices for future use and best overall value.

# MCR12DCM, MCR12DCN

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	2.2	$^{\circ}\text{C}/\text{W}$
— Junction to Ambient	$R_{\theta JA}$	88	
— Junction to Ambient <sup>(1)</sup>	$R_{\theta JA}$	80	
Maximum Lead Temperature for Soldering Purposes <sup>(2)</sup>	$T_L$	260	$^{\circ}\text{C}$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

## OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current ( $V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}$ , Gate Open)	$I_{DRM}, I_{RRM}$	—	—	0.01	mA
$T_J = 25^{\circ}\text{C}$		—	—	5.0	
$T_J = 125^{\circ}\text{C}$		—	—		

## ON CHARACTERISTICS

Peak Forward On-State Voltage <sup>(3)</sup> ( $I_{TM} = 20 \text{ A}$ )	$V_{TM}$	—	1.3	1.9	Volts
Gate Trigger Current (Continuous dc) ( $V_D = 12 \text{ V}$ , $R_L = 100 \Omega$ )	$I_{GT}$	2.0	7.0	20	mA
$T_J = 25^{\circ}\text{C}$		—	—	40	
$T_J = -40^{\circ}\text{C}$					
Gate Trigger Voltage (Continuous dc) ( $V_D = 12 \text{ V}$ , $R_L = 100 \Omega$ )	$V_{GT}$	0.5	0.65	1.0	Volts
$T_J = 25^{\circ}\text{C}$		—	—	2.0	
$T_J = -40^{\circ}\text{C}$					
Gate Non-Trigger Voltage ( $V_D = 12 \text{ V}$ , $R_L = 100 \Omega$ )	$V_{GD}$	0.2	—	—	Volts
$T_J = 125^{\circ}\text{C}$					
Holding Current ( $V_D = 12 \text{ V}$ , Initiating Current = 200 mA, Gate Open)	$I_H$	4.0	22	40	mA
$T_J = 25^{\circ}\text{C}$		—	—	80	
$T_J = -40^{\circ}\text{C}$					
Latching Current ( $V_D = 12 \text{ V}$ , $I_G = 20 \text{ mA}$ , $T_J = 25^{\circ}\text{C}$ ) ( $V_D = 12 \text{ V}$ , $I_G = 40 \text{ mA}$ , $T_J = -40^{\circ}\text{C}$ )	$I_L$	4.0	22	40	mA
		—	—	80	

## DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Critical Rate of Rise of Off-State Voltage ( $V_D = \text{Rated } V_{DRM}$ , Exponential Waveform, Gate Open, $T_J = 125^{\circ}\text{C}$ )	$dv/dt$	50	200	—	$\text{V}/\mu\text{s}$

(1) Surface mounted on minimum recommended pad size.

(2) 1/8" from case for 10 seconds.

(3) Pulse Test: Pulse Width  $\leq 2.0 \text{ msec}$ , Duty Cycle  $\leq 2\%$ .

# MCR12DCM, MCR12DCN

## Voltage Current Characteristic of SCR

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Off State Forward Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Off State Reverse Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Peak On State Voltage
$I_H$	Holding Current

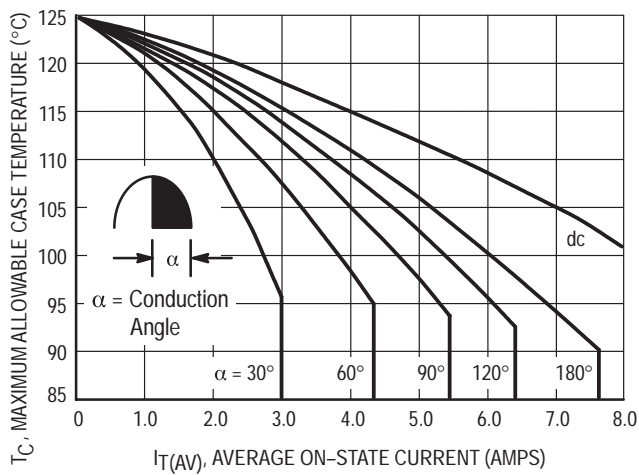
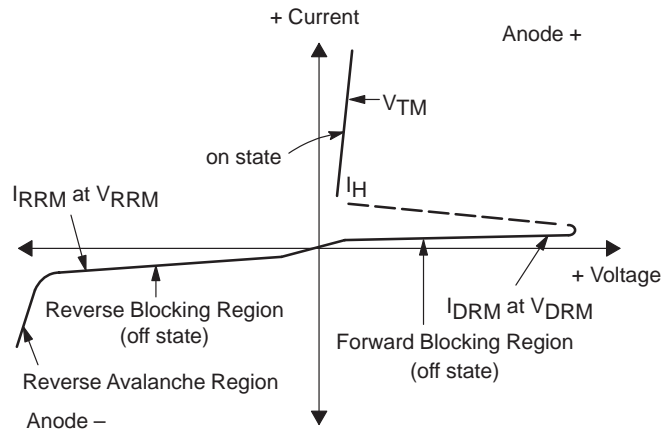


Figure 1. Average Current Derating

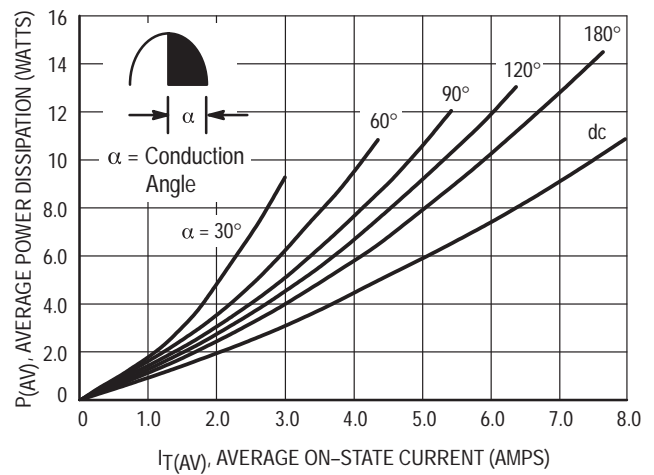


Figure 2. On-State Power Dissipation

# MCR12DCM, MCR12DCN

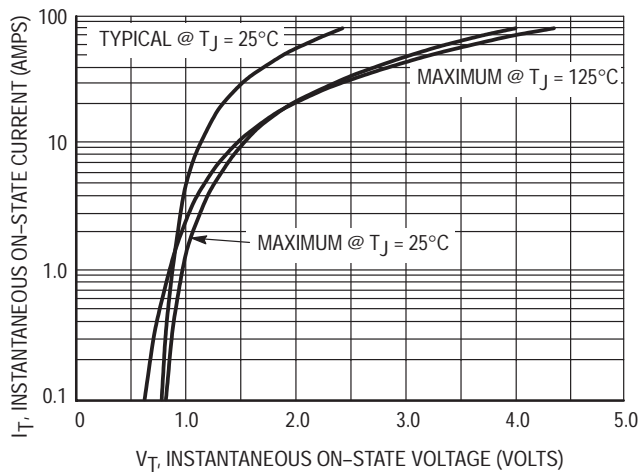


Figure 3. On-State Characteristics

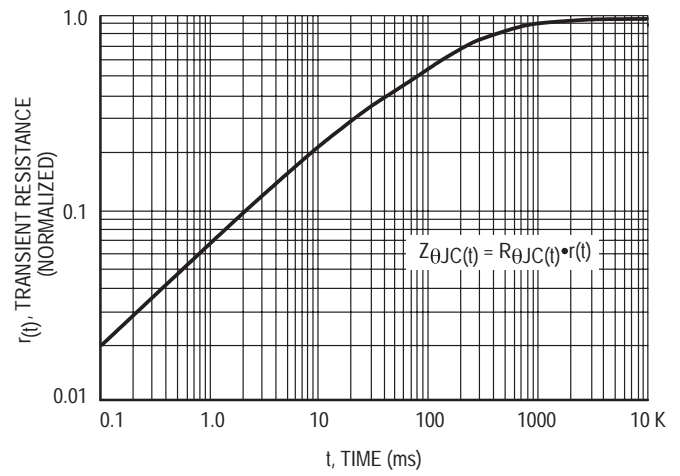


Figure 4. Transient Thermal Response

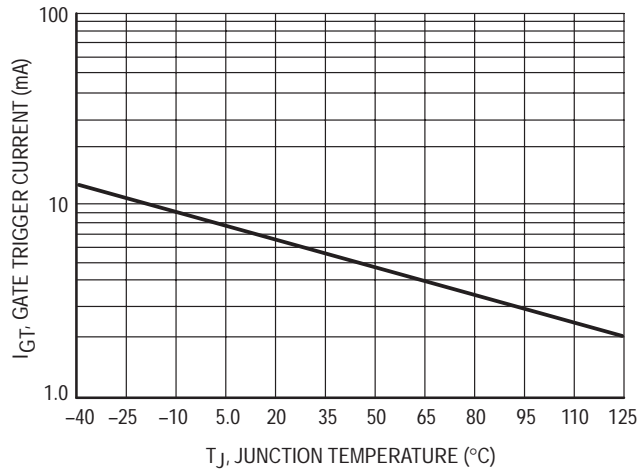


Figure 5. Typical Gate Trigger Current versus Junction Temperature

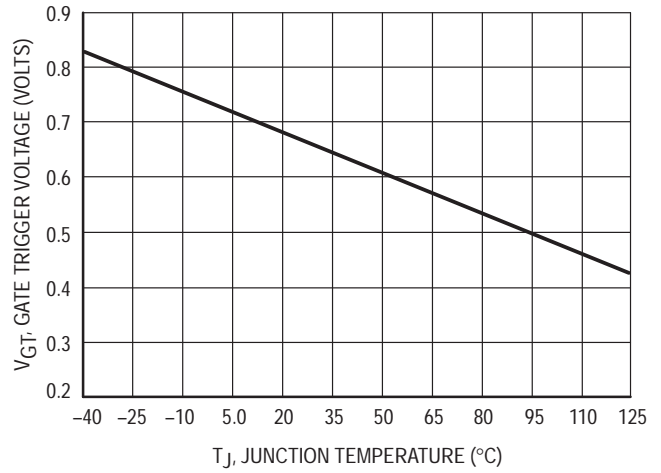
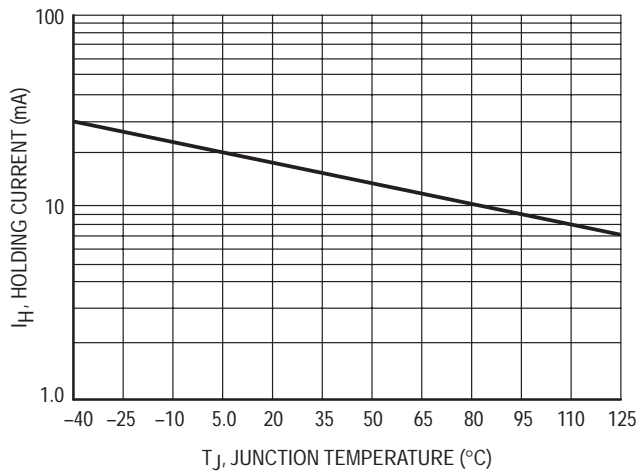
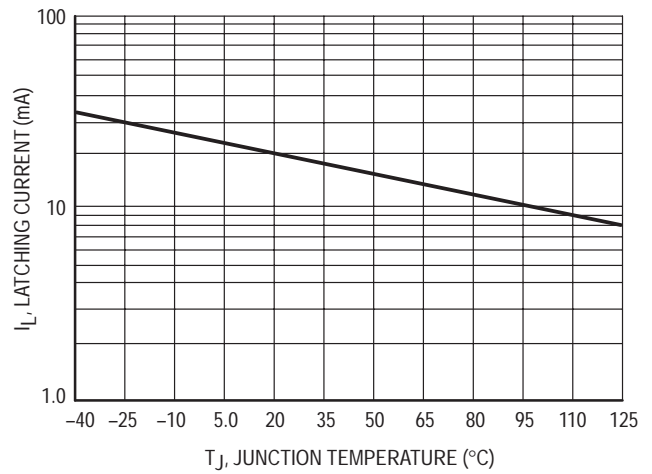


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

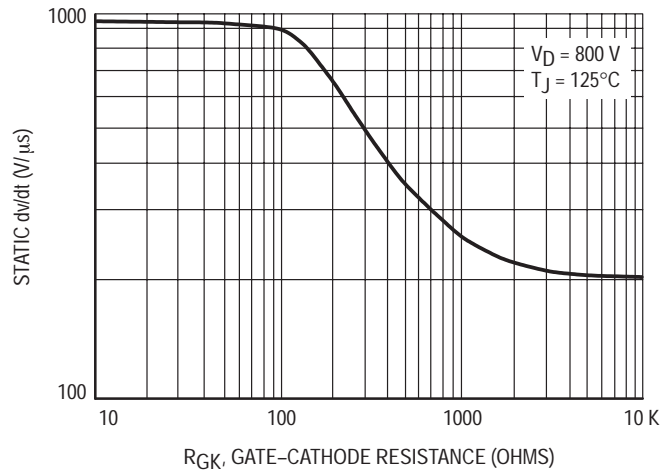
# MCR12DCM, MCR12DCN



**Figure 7. Typical Holding Current versus Junction Temperature**



**Figure 8. Typical Latching Current versus Junction Temperature**



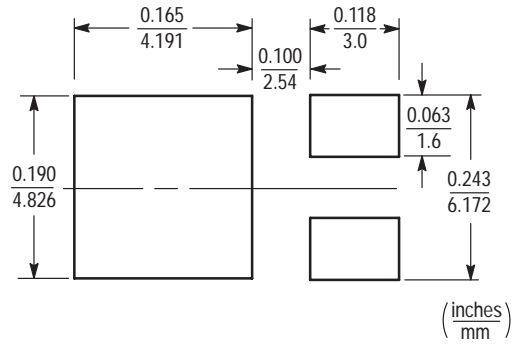
**Figure 9. Exponential Static dv/dt versus Gate-Cathode Resistance**

## MCR12DCM, MCR12DCN

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

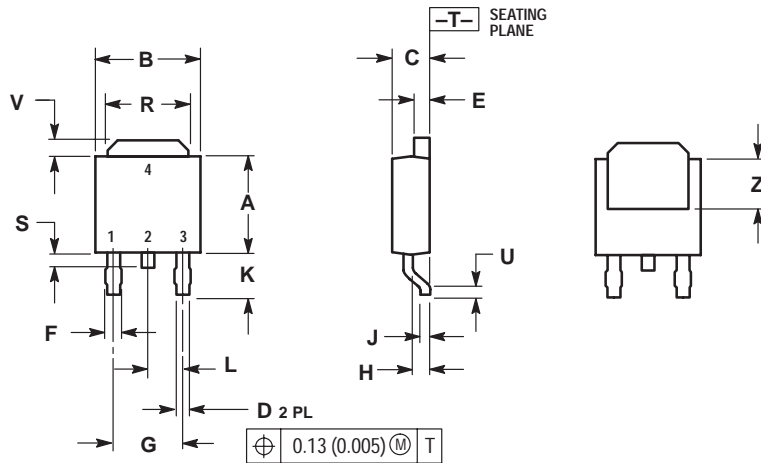


**DPAK**

# MCR12DCM, MCR12DCN

## PACKAGE DIMENSIONS


### D-PAK CASE 369A-13 ISSUE Z



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

STYLE 4:  
PIN 1: CATHODE  
PIN 2: ANODE  
PIN 3: GATE  
PIN 4: ANODE

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### **NORTH AMERICA Literature Fulfillment:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**EUROPE:** LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (M–F 1:00pm to 5:00pm Munich Time)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (M–F 1:00pm to 5:00pm Toulouse Time)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (M–F 12:00pm to 5:00pm UK Time)  
**Email:** ONlit@hibbertco.com

**EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781**

\*Available from Germany, France, Italy, England, Ireland

### **CENTRAL/SOUTH AMERICA:**

**Spanish Phone:** 303-308-7143 (Mon–Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com

**ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)  
Toll Free from Hong Kong & Singapore:  
**001-800-4422-3781**  
**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549  
**Phone:** 81-3-5740-2745  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.