MOTOROLA
Semiconductor Components

Order Number: MC10EP31/D
Rev. 1.1, 05/1999

MC10EP31

SO–8, D SUFFIX
8–LEAD PLASTIC SOIC PACKAGE
CASE 751

ORDERING INFORMATION

MC10EP31D SOIC

ECLinPS Plus™

Product Preview

D Flip Flop with Set and Reset

- 380ps Typical Propagation Delay
- High Bandwidth to 3 Ghz Typical
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- 75kΩ Internal Input Pulldown Resistors
- Q Output will default LOW with inputs open or at V_{EE}
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 75 devices

PIN DESCRIPTION

PIN	FUNCTION
CLK	ECL Clock Inputs
Reset	ECL Asynchronous Reset
Set	ECL Asynchronous Set
D	ECL Data Input
Q, $\overline{Q}$	ECL Data Outputs

TRUTH TABLE

D	SET	RESET	CLK	Q
L	L	L	Z	L
H	L	L	Z	H
X	H	L	X	H
X	L	H	X	L
X	H	H	X	UNDEF

Z = LOW to HIGH Transition

The MC10EP31 is a D flip flop with set and reset. The device is pin and functionally equivalent to the EL31 and LVEL31 devices. With AC performance much faster than the EL31 and LVEL31 devices, the EP31 is ideal for applications requiring the fastest AC performance available. Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip–flop when CLK is low and is transferred to the slave, and thus the outputs, upon a positive transition of the CLK.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

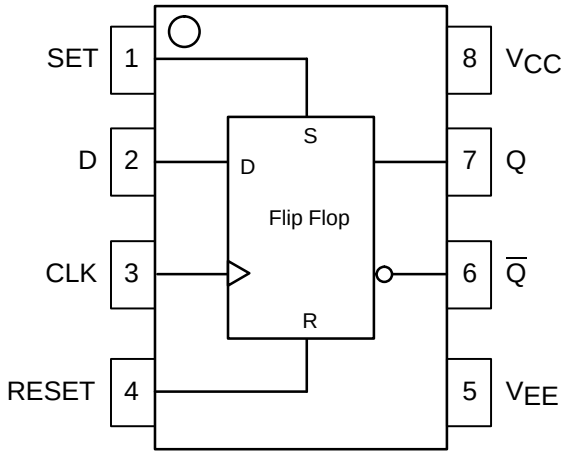


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 3.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current (Note 1.)	26	34	44	26	35	44	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 6.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current (Note 4.)	26	34	44	26	35	44	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 5.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 5.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
5. All loading with 50 ohms to V_{CC}–2.0 volts.
6. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 9.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
IEE	Power Supply Current (Note 7.)	26	34	44	26	35	44	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 8.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 8.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

7. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Input and output parameters vary 1:1 with V_{CC}.

AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –3.0V to –5.5V) or (V_{CC} = 3.0V to 5.5V; V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (Note 10.)	2.7	3.0		2.7	3.0		2.7	3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	CLK–>Q, $\overline{Q}$	175	250	325	200	275	350	250	320	400	
	S, R–>Q, $\overline{Q}$	200	280	360	250	330	420	325	400	475	
t_{RR}	Set/Reset Recovery		TBD			TBD			TBD		ps
t_S	Setup Time		TBD			TBD			TBD		ps
t_H	Hold Time		TBD			TBD			TBD		
t_{SKEW}	Duty Cycle Skew (Note 11.)		TBD			TBD			TBD		ps
	Skew Part–to–Part		TBD			TBD			TBD		
t_{PW}	Minimum Pulse Width										ps
	CLK, SET, RESET		TBD			TBD			TBD		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Output Rise/Fall Times										ps
t_f	(20% – 80%) Q, $\overline{Q}$	50	120	180	60	130	200	70	150	220	

10. F_{max} guaranteed for functionality only. See Figure 2 for typical output swing. V_{OL} and V_{OH} levels are guaranteed at DC only.
11. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

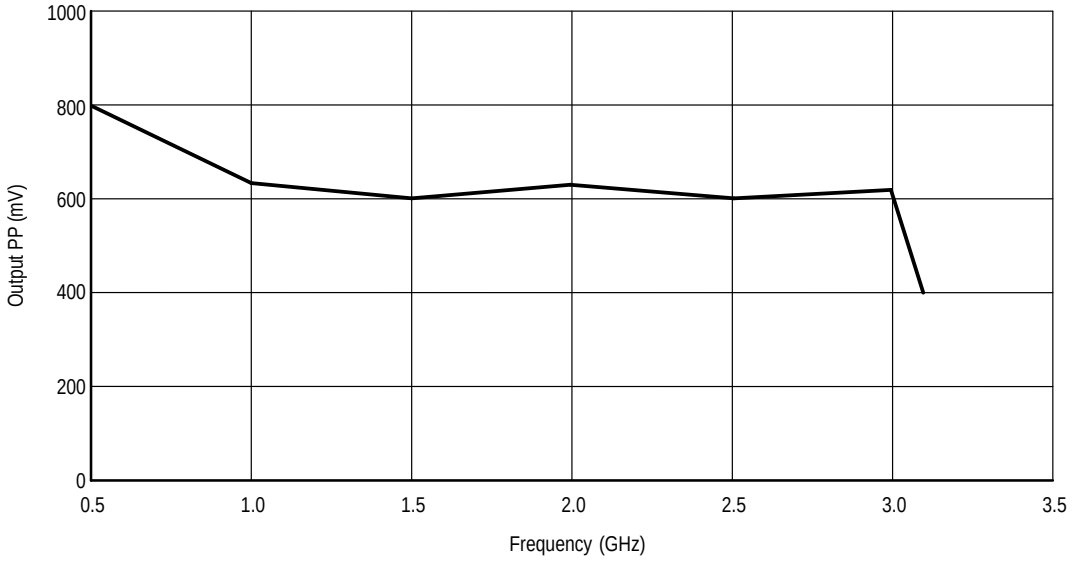
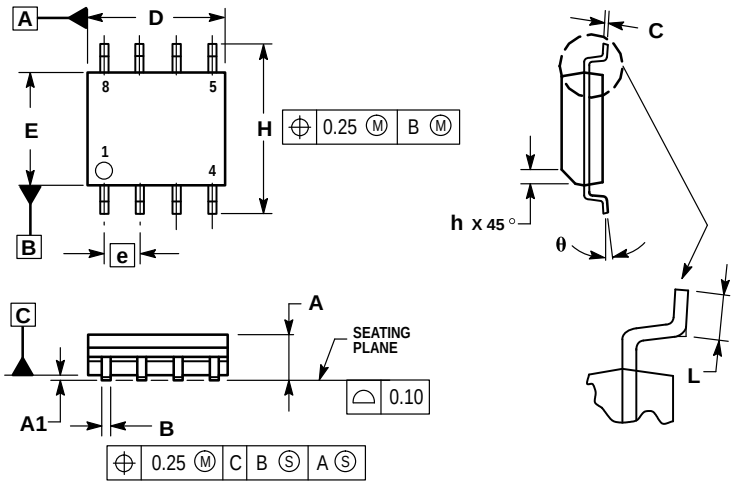


Figure 2. Typical Output V_{PP} vs. Frequency

OUTLINE DIMENSIONS

SO–8, D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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