MOTOROLA
Semiconductor Components

Order Number: MC100EPT24/D
Rev. 0.1, 05/1999

MC100EPT24

SO–8, D SUFFIX
8–LEAD PLASTIC SOIC PACKAGE
CASE 751

ORDERING INFORMATION

MC100EPT24D SOIC

ECLinPS Plus™

Product Preview

LVTTL/LVCMOS to Differential LVECL Translator

PIN DESCRIPTION

PIN	FUNCTION
Q, $\overline{Q}$	Diff LVECL Outputs
D	LVTTL Input
V_{CC}	Positive Supply
GND	Ground
V_{EE}	Negative Supply

- 350ps Typical Propagation Delay
- Maximum Frequency > 1.0GHz
- Differential ECL Outputs
- Small Outline SOIC Package
- PNP LVTTL Inputs for Minimal Loading
- Flow Through Pinouts
- Q Output will default HIGH with inputs open
- ESD Protection:TBD KV HBM, TBD V MM
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 181 devices

The MC100EPT24 is a LVTTL/LVCMOS to differential LVECL translator. Because LVECL levels and LVTTL/LVCMOS levels are used, a –3.3V, +3.3V and ground are required. The small outline 8–lead SOIC package and the single gate of the EPT24 makes it ideal for those applications where space, performance, and low power are at a premium.

The EPT24 is available in the 100E standard and is compatible with ECL 100K logic levels.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

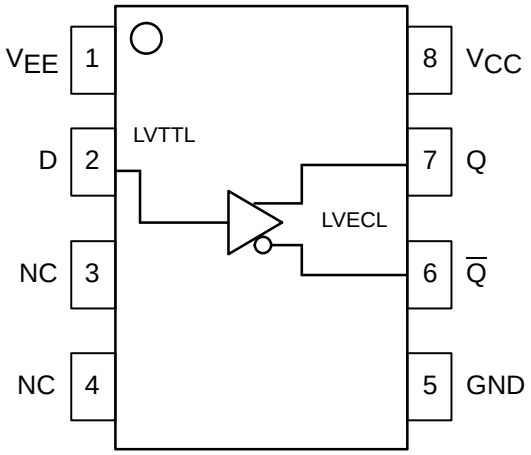


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

LVTTL INPUT DC CHARACTERISTICS (V_{CC} = 3.3V ±0.3V; GND = 0V; T_A = –40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current (V_{in} = 2.7V)			20	μA
I_{IHH}	Input HIGH Current MAX (V_{in} = 6.0V)			100	μA
I_{IL}	Input LOW Current (V_{in} = 0.5V)			–0.6	mA
V_{IK}	Input Clamp Voltage (I_{in} = –18mA)			–1.2	V
V_{IH}	Input HIGH Voltage	2.0			V
V_{IL}	Input LOW Voltage			0.8	V

LVECL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; V_{EE} = –3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 1.)	-1135		-885	-1070		-820	-1010		-760	mV
V_{OL}	Output LOW Voltage (Note 1.)	-1935		-1685	-1870		-1620	-1810		-1560	mV
I_{CCH}	Power Supply Current HIGH (Note 2.)	TBD		TBD	TBD		TBD	TBD		TBD	mA
I_{CCL}	Power Supply Current LOW (Note 3.)	TBD		TBD	TBD		TBD	TBD		TBD	mA

1. Output levels will vary 1:1 with GND; Outputs loaded through 50Ω to GND – 2.0V.
2. Outputs in HIGH state.
3. Outputs in LOW state.

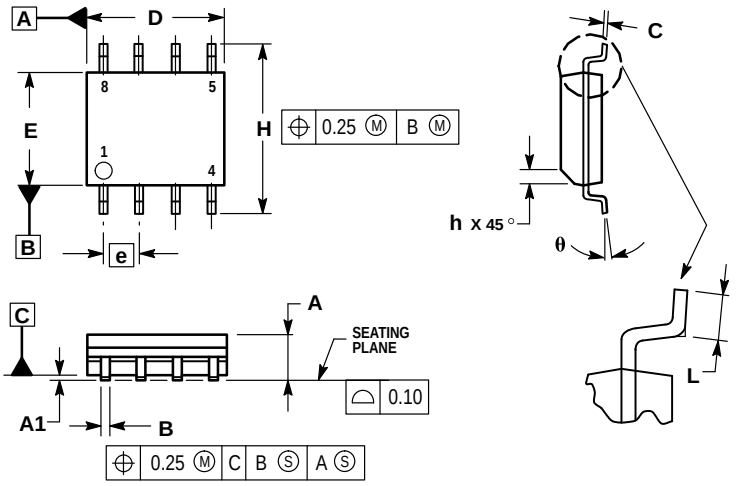
AC CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V; V_{EE} = –3.3V ± 0.3V; GND = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency (Note 4.)		TBD			>1.0			TBD		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential		TBD TBD			350 380			TBD TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, $\overline{Q}$		TBD TBD			TBD 120			TBD TBD		ps

4. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

OUTLINE DIMENSIONS

SO–8, D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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