

## MC100EP139



**SO-20, DT SUFFIX**  
20 PIN PLASTIC TSSOP PACKAGE  
CASE 948E

**ORDERING INFORMATION**  
MC100EP139DT TSSOP

# ECLPS Plus™

Product Preview

## ÷2/4, ÷4/5/6 Clock Generation Chip

- Maximum Frequency > 2.7GHz
- 50ps Output-to-Output Skew
- PECL mode: 3.0V to 5.5V  $V_{CC}$  with  $V_{EE} = 0V$
- ECL mode: 0V  $V_{CC}$  with  $V_{EE} = -3.0V$  to  $-5.5V$
- Synchronous Enable/Disable
- Master Reset for Synchronization
- Q Output will default LOW with inputs open or at  $V_{EE}$
- ESD Protection: >4KV HBM, >200V MM
- $V_{BB}$  Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 758 devices

### PIN NAMES

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
$\overline{EN}$	ECL Sync Enable
MR	ECL Master Reset
$V_{BB}$	ECL Reference Output
Q0, Q1, $\overline{Q0}$ , $\overline{Q1}$	ECL Diff ÷2/4 Outputs
Q2, Q3, $\overline{Q2}$ , $\overline{Q3}$	ECL Diff ÷4/5/6 Outputs
DIVSEL <sub>a</sub>	ECL Freq. Select Input ÷ 2/4
DIVSEL <sub>b0</sub>	ECL Freq. Select Input ÷ 4/5/6
DIVSEL <sub>b1</sub>	ECL Freq. Select Input ÷ 4/5/6
$V_{CC}$ , $V_{CC0}$	ECL Positive Supply
$V_{EE}$	ECL Negative, 0 Supply

### FUNCTION TABLES

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

Z = Low-to-High Transition  
ZZ = High-to-Low Transition

DIVSEL <sub>a</sub>	Q0:1 OUTPUTS	
0	Divide by 2	
1	Divide by 4	
DIVSEL <sub>b0</sub>	DIVSEL <sub>b1</sub>	Q2:3 OUTPUTS
0	0	Divide by 4
1	0	Divide by 6
0	1	Divide by 5
1	1	Divide by 5

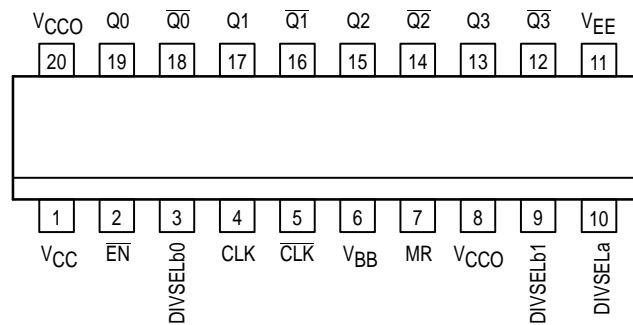
The MC100EP139 is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the  $V_{BB}$  output, a sinusoidal source can be AC coupled into the device. If a single-ended input is to be used, the  $V_{BB}$  output should be connected to the  $\overline{CLK}$  input and bypassed to ground via a 0.01μF capacitor.

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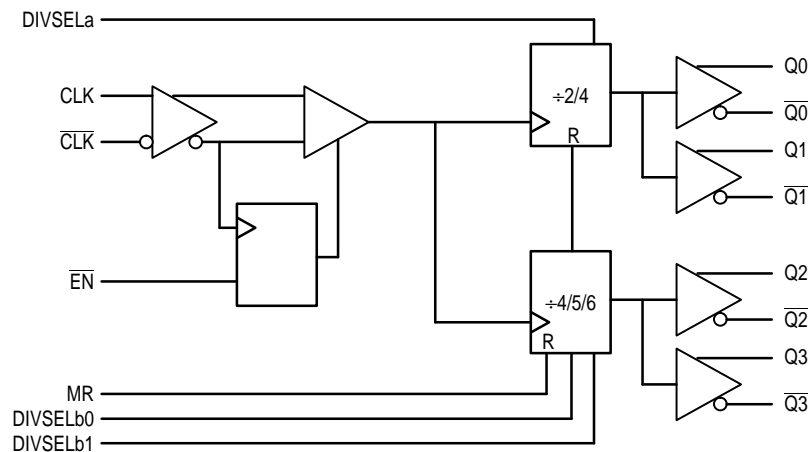
**ECLinPS Plus™ MC100EP139**

The common enable ( $\overline{\text{EN}}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

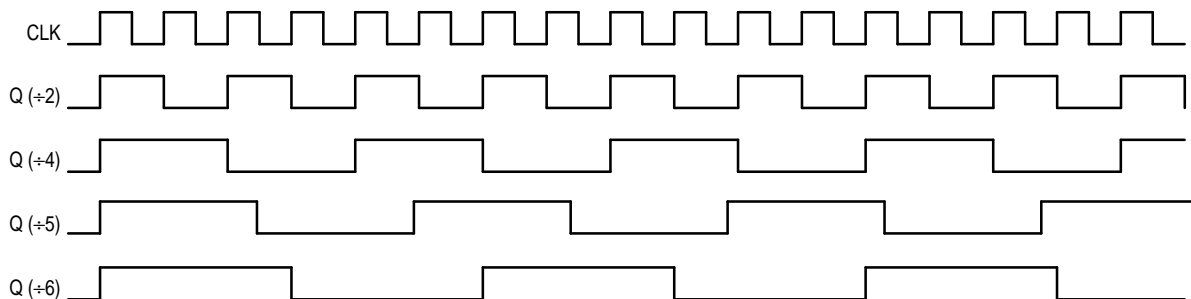
Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EP139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EP139, the MR pin need not be exercised as the internal divider design ensures synchronization between the +2/4 and the +4/5/6 outputs of a single device.



### Figure 1. 20—Lead SOIC (Top View)



### Figure 2. Logic Diagram



### Figure 3. Timing Diagrams

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
$V_{EE}$	Power Supply ( $V_{CC} = 0V$ )	-6.0 to 0	VDC
$V_{CC}$	Power Supply ( $V_{EE} = 0V$ )	6.0 to 0	VDC
$V_I$	Input Voltage ( $V_{CC} = 0V$ , $V_I$ not more negative than $V_{EE}$ )	-6.0 to 0	VDC
$V_I$	Input Voltage ( $V_{EE} = 0V$ , $V_I$ not more positive than $V_{CC}$ )	6.0 to 0	VDC
$I_{out}$	Output Current Continuous Surge	50 100	mA
$I_{BB}$	$V_{BB}$ Sink/Source Current†	$\pm 0.5$	mA
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) Still Air 500lfpm	90 60	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	33 to 35 $\pm 5\%$	°C/W
$T_{sol}$	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

**DC CHARACTERISTICS** ( $V_{EE} = -5V$ ;  $V_{CC} = V_{CCO} = GND$ ;  $T_A = 0^\circ C$  to  $+85^\circ C$ )

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions	
V <sub>OH</sub>	Output HIGH Voltage			−895	mV	V <sub>IN</sub> = V <sub>IH</sub> (max) or V <sub>IL</sub> (min)	Loading with 50Ω to −2.0V
V <sub>OL</sub>	Output LOW Voltage	−1945			mV		
V <sub>OHA</sub>	Output HIGH Voltage	−1145			mV		
V <sub>OLA</sub>	Output LOW Voltage			−1695	mV		
V <sub>IH</sub>	Input HIGH Voltage		−1022.5		mV	Guaranteed HIGH Signal for All Inputs	
V <sub>IL</sub>	Input LOW Voltage		−1642.5		mV	Guaranteed LOW Signal for All Inputs	
I <sub>IL</sub>	Input LOW Current	0.5			μA	V <sub>IN</sub> = V <sub>IL</sub> (min)	

1.  $V_{BB} = V_{CC} - 1.425 \pm 100mV$

**AC CHARACTERISTICS** ( $V_{EE} = -3.8V$  to  $-3.0V$ ;  $V_{CC} = GND$ )

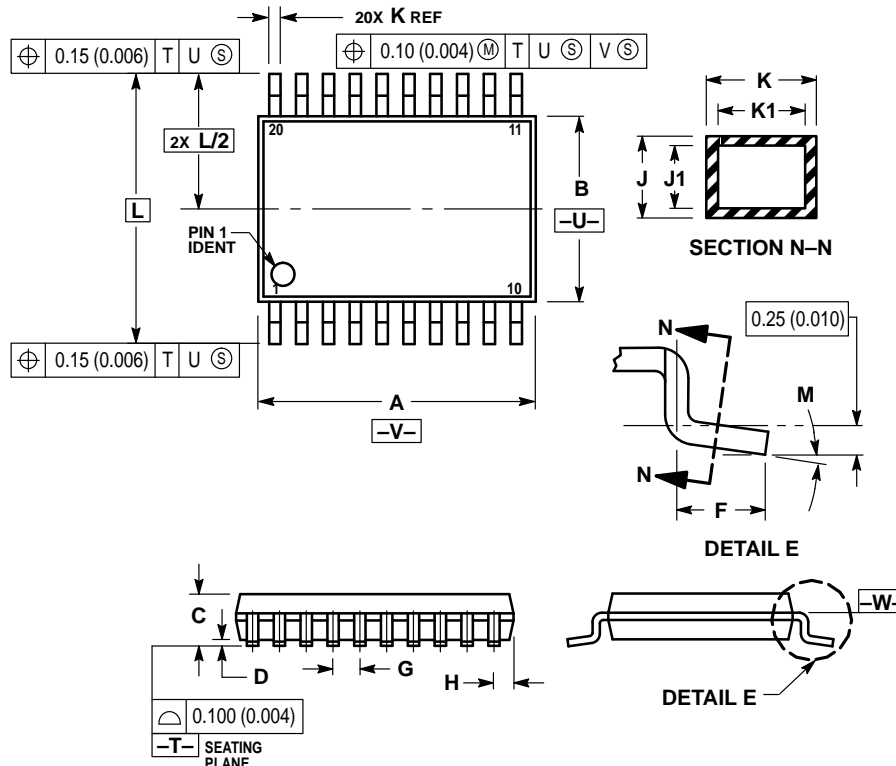
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency		TBD			TBD			1500			TBD		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CLK Q (Diff) to Output CLK Q (S.E.) MR Q		TBD TBD TBD			TBD TBD TBD			550 570 620			TBD TBD TBD		ps
$t_{SKEW}$	Within-Device Skew $Q_0 - Q_3$ (Note 2.)		TBD TBD			TBD TBD			50			TBD TBD		ps
	Part-to-Part $Q_0 - Q_3$ (Diff)		TBD			TBD			200			TBD		
$t_S$	Setup Time $\overline{EN}$ CLK DIVSEL CLK		TBD TBD			TBD TBD			300 450			TBD TBD		ps
	Hold Time $\overline{CLK}$ $\overline{EN}$ CLK Div_Sel		TBD TBD			TBD TBD			150 200			TBD TBD		
$V_{PP}$	Minimum Input Swing (Note 3.) CLK		TBD			TBD			300			TBD		mV
$V_{CMR}$	Common Mode Range (Note 4.) $V_{PP} < 500mV$ $V_{PP} \geq 500mV$		TBD TBD			TBD TBD		-2.1 -1.9		-0.4 -0.4		TBD TBD		V
$t_{RR}$	Reset Recovery Time		TBD			TBD			100			TBD		ps
$t_{PW}$	Minimum Pulse Width CLK MR		TBD TBD			TBD TBD			400 500			TBD TBD		ps
$t_r, t_f$	Output Rise/Fall Times (20% – 80%) Q		TBD			TBD			165			TBD		ps

2. Skew is measured between outputs under identical transitions.

3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.

4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1V. The lower end of the CMR range varies 1:1 with  $V_{EE}$ . The numbers in the spec table assume a nominal  $V_{EE} = -3.3V$ . Note for PECL operation, the  $V_{CMR(min)}$  will be fixed at  $3.3V - |V_{CMR(min)}|$ .


**OUTLINE DIMENSIONS**  
**SO-20, DT SUFFIX**  
 20 PIN PLASTIC TSSOP PACKAGE  
 CASE 948E-02  
 ISSUE A



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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