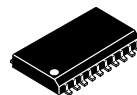


## MC100EP139



**SO-20, DW SUFFIX**  
20-LEAD PLASTIC WIDE SOIC PACKAGE  
CASE 751D

**ORDERING INFORMATION**  
MC100EP139DW SOIC

# ECLPS Plus™

## Product Preview ÷2/4, ÷4/5/6 Clock Generation Chip

- Maximum Frequency > 2.7GHz
- 50ps Output-to-Output Skew
- PECL mode: 3.0V to 5.5V V<sub>CC</sub> with V<sub>EE</sub> = 0V
- ECL mode: 0V V<sub>CC</sub> with V<sub>EE</sub> = -3.0V to -5.5V
- Synchronous Enable/Disable
- Master Reset for Synchronization
- Q Output will default LOW with inputs open or at V<sub>EE</sub>
- ESD Protection: >4KV HBM, >200V MM
- V<sub>BB</sub> Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 758 devices

### PIN NAMES

| PIN   | FUNCTION                       |
|---|--------------------------------|
| CLK, $\overline{\text{CLK}}$                            | ECL Diff Clock Inputs          |
| $\overline{\text{EN}}$                                  | ECL Sync Enable                |
| MR  | ECL Master Reset               |
| V <sub>BB</sub>   | ECL Reference Output           |
| Q0, Q1, $\overline{\text{Q0}}$ , $\overline{\text{Q1}}$ | ECL Diff ÷2/4 Outputs          |
| Q2, Q3, $\overline{\text{Q2}}$ , $\overline{\text{Q3}}$ | ECL Diff ÷4/5/6 Outputs        |
| DIVSEL <sub>a</sub>                                     | ECL Freq. Select Input ÷ 2/4   |
| DIVSEL <sub>b0</sub>                                    | ECL Freq. Select Input ÷ 4/5/6 |
| DIVSEL <sub>b1</sub>                                    | ECL Freq. Select Input ÷ 4/5/6 |
| V <sub>CC</sub> , V <sub>CC0</sub>                      | ECL Positive Supply            |
| V <sub>EE</sub>   | ECL Negative, 0 Supply         |

### FUNCTION TABLES

| CLK | $\overline{\text{EN}}$ | MR | FUNCTION   |
|-----|------------------------|----|------------|
| Z   | L                      | L  | Divide     |
| ZZ  | H                      | L  | Hold Q0:3  |
| X   | X                      | H  | Reset Q0:3 |

Z = Low-to-High Transition  
ZZ = High-to-Low Transition

| DIVSEL <sub>a</sub>  | Q0:1 OUTPUTS         |              |
|----------------------|----------------------|--------------|
| 0                    | Divide by 2          |              |
| 1                    | Divide by 4          |              |
| DIVSEL <sub>b0</sub> | DIVSEL <sub>b1</sub> | Q2:3 OUTPUTS |
| 0                    | 0                    | Divide by 4  |
| 1                    | 0                    | Divide by 6  |
| 0                    | 1                    | Divide by 5  |
| 1                    | 1                    | Divide by 5  |

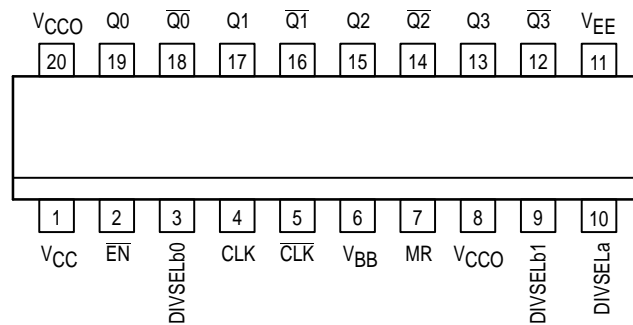
The MC100EP139 is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the V<sub>BB</sub> output, a sinusoidal source can be AC coupled into the device. If a single-ended input is to be used, the V<sub>BB</sub> output should be connected to the  $\overline{\text{CLK}}$  input and bypassed to ground via a 0.01μF capacitor.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

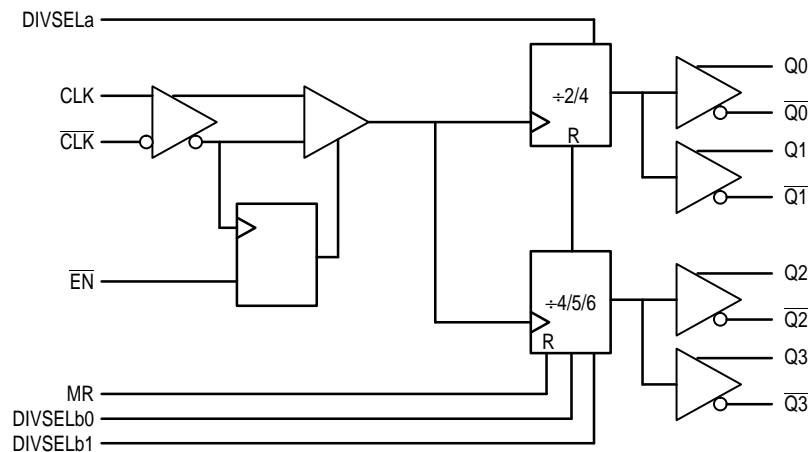
**ECLinPS Plus™ MC100EP139**

The common enable ( $\overline{\text{EN}}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

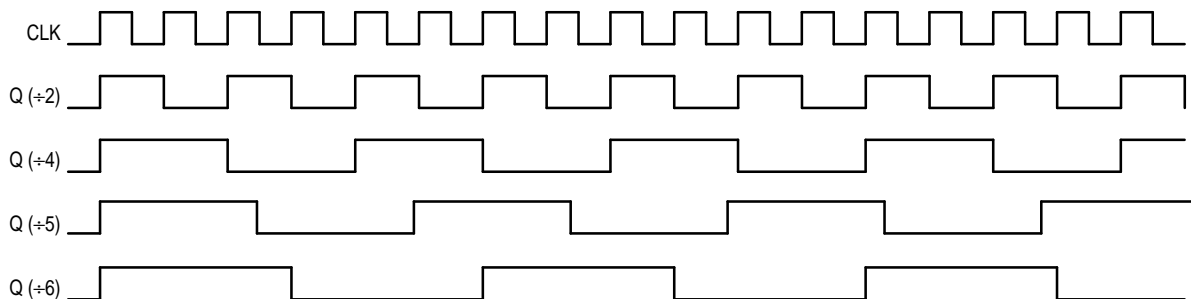
Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EP139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EP139, the MR pin need not be exercised as the internal divider design ensures synchronization between the  $\div 2/4$  and the  $\div 4/5/6$  outputs of a single device.



### Figure 1. 20—Lead SOIC (Top View)



### Figure 2. Logic Diagram



### Figure 3. Timing Diagrams

**MAXIMUM RATINGS\***

| Symbol        | Parameter   | Value              | Unit |
|---------------|---|--------------------|------|
| $V_{EE}$      | Power Supply ( $V_{CC} = 0V$ )  | -6.0 to 0          | VDC  |
| $V_{CC}$      | Power Supply ( $V_{EE} = 0V$ )  | 6.0 to 0           | VDC  |
| $V_I$         | Input Voltage ( $V_{CC} = 0V$ , $V_I$ not more negative than $V_{EE}$ ) | -6.0 to 0          | VDC  |
| $V_I$         | Input Voltage ( $V_{EE} = 0V$ , $V_I$ not more positive than $V_{CC}$ ) | 6.0 to 0           | VDC  |
| $I_{out}$     | Output Current<br>Continuous<br>Surge                                   | 50<br>100          | mA   |
| $I_{BB}$      | $V_{BB}$ Sink/Source Current†   | $\pm 0.5$          | mA   |
| $T_A$         | Operating Temperature Range   | -40 to +85         | °C   |
| $T_{stg}$     | Storage Temperature   | -65 to +150        | °C   |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient)<br>Still Air<br>500lfpm        | 90<br>60           | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)                                   | 33 to 35 $\pm 5\%$ | °C/W |
| $T_{sol}$     | Solder Temperature (<2 to 3 Seconds: 245°C desired)                     | 265                | °C   |

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

**DC CHARACTERISTICS** ( $V_{EE} = -5V$ ;  $V_{CC} = V_{CCO} = GND$ ;  $T_A = 0^\circ C$  to  $+85^\circ C$ )

| Symbol           | Characteristic      | Min   | Typ     | Max   | Unit | Conditions  |                              |
|------------------|---------------------|-------|---------|-------|------|---|------------------------------|
| V <sub>OH</sub>  | Output HIGH Voltage |       |         | −895  | mV   | V <sub>IN</sub> = V <sub>IH</sub> (max)<br>or V <sub>IL</sub> (min) | Loading with<br>50Ω to −2.0V |
| V <sub>OL</sub>  | Output LOW Voltage  | −1945 |         |       | mV   |   |                              |
| V <sub>OHA</sub> | Output HIGH Voltage | −1145 |         |       | mV   |   |                              |
| V <sub>OLA</sub> | Output LOW Voltage  |       |         | −1695 | mV   |   |                              |
| V <sub>IH</sub>  | Input HIGH Voltage  |       | −1022.5 |       | mV   | Guaranteed HIGH Signal for All Inputs                               |                              |
| V <sub>IL</sub>  | Input LOW Voltage   |       | −1642.5 |       | mV   | Guaranteed LOW Signal for All Inputs                                |                              |
| I <sub>IL</sub>  | Input LOW Current   | 0.5   |         |       | μA   | V <sub>IN</sub> = V <sub>IL</sub> (min)                             |                              |

1.  $V_{BB} = V_{CC} - 1.425 \pm 100mV$ **AC CHARACTERISTICS** ( $V_{EE} = -3.8V$  to  $-3.0V$ ;  $V_{CC} = GND$ )

| Symbol                 | Characteristic  | -40°C |                   |     | 0°C |                   |     | 25°C         |                   |              | 85°C |                   |     | Unit |
|------------------------|---|-------|-------------------|-----|-----|-------------------|-----|--------------|-------------------|--------------|------|-------------------|-----|------|
|                        |   | Min   | Typ               | Max | Min | Typ               | Max | Min          | Typ               | Max          | Min  | Typ               | Max |      |
| $f_{MAX}$              | Maximum Toggle Frequency  |       | TBD               |     |     | TBD               |     |              | 1500              |              |      | TBD               |     | MHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLK<br>Q (Diff)<br>to Output CLK Q (S.E.)<br>MR Q    |       | TBD<br>TBD<br>TBD |     |     | TBD<br>TBD<br>TBD |     |              | 550<br>570<br>620 |              |      | TBD<br>TBD<br>TBD |     | ps   |
| $t_{SKEW}$             | Within-Device Skew<br>$Q_0 - Q_3$ (Note 2.)                               |       | TBD<br>TBD        |     |     | TBD<br>TBD        |     |              | 50                |              |      | TBD<br>TBD        |     | ps   |
|                        | Part-to-Part<br>$Q_0 - Q_3$ (Diff)  |       | TBD               |     |     | TBD               |     |              | 200               |              |      | TBD               |     |      |
| $t_S$                  | Setup Time $\overline{EN}$ CLK<br>DIVSEL CLK                              |       | TBD<br>TBD        |     |     | TBD<br>TBD        |     |              | 300<br>450        |              |      | TBD<br>TBD        |     | ps   |
|                        | Hold Time $\overline{CLK}$ $\overline{EN}$<br>CLK Div_Sel                 |       | TBD<br>TBD        |     |     | TBD<br>TBD        |     |              | 150<br>200        |              |      | TBD<br>TBD        |     |      |
| $V_{PP}$               | Minimum Input Swing<br>(Note 3.) CLK                                      |       | TBD               |     |     | TBD               |     |              | 300               |              |      | TBD               |     | mV   |
| $V_{CMR}$              | Common Mode Range<br>(Note 4.)<br>$V_{PP} < 500mV$<br>$V_{PP} \geq 500mV$ |       | TBD<br>TBD        |     |     | TBD<br>TBD        |     | -2.1<br>-1.9 |                   | -0.4<br>-0.4 |      | TBD<br>TBD        |     | V    |
|                        |   |       |                   |     |     |                   |     |              |                   |              |      |                   |     |      |
| $t_{RR}$               | Reset Recovery Time   |       | TBD               |     |     | TBD               |     |              | 100               |              |      | TBD               |     | ps   |
| $t_{PW}$               | Minimum Pulse Width<br>CLK<br>MR  |       | TBD<br>TBD        |     |     | TBD<br>TBD        |     |              | 400<br>500        |              |      | TBD<br>TBD        |     | ps   |
|                        |   |       |                   |     |     |                   |     |              |                   |              |      |                   |     |      |
| $t_r, t_f$             | Output Rise/Fall Times<br>(20% – 80%) Q                                   |       | TBD               |     |     | TBD               |     |              | 165               |              |      | TBD               |     | ps   |

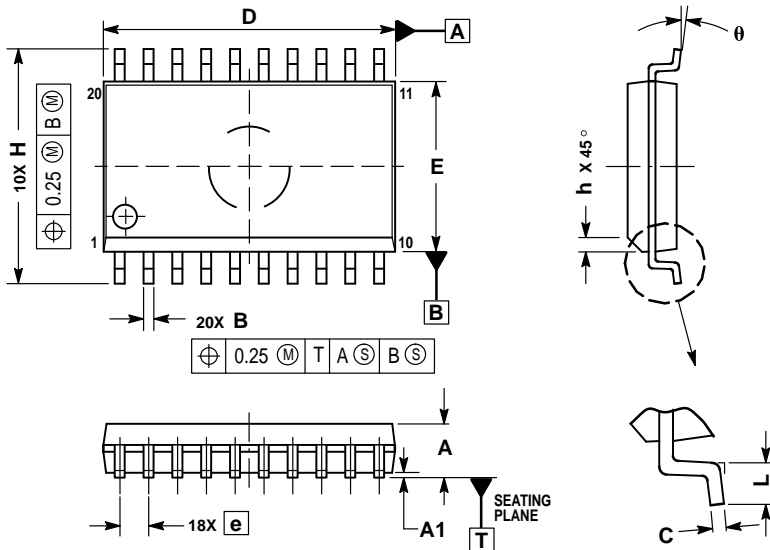
2. Skew is measured between outputs under identical transitions.

3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.

4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1V. The lower end of the CMR range varies 1:1 with  $V_{EE}$ . The numbers in the spec table assume a nominal  $V_{EE} = -3.3V$ . Note for PECL operation, the  $V_{CMR(min)}$  will be fixed at  $3.3V - |V_{CMR(min)}|$ .


OUTLINE DIMENSIONS

SO-20, DW SUFFIX  
PLASTIC WIDE SOIC PACKAGE  
CASE 751D-05  
ISSUE F



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM   | MILLIMETERS |       |
|-------|-------------|-------|
|       | MIN         | MAX   |
| A     | 2.35        | 2.65  |
| A1    | 0.10        | 0.25  |
| B     | 0.35        | 0.49  |
| C     | 0.23        | 0.32  |
| D     | 12.65       | 12.95 |
| E     | 7.40        | 7.60  |
| e     | 1.27 BSC    |       |
| H     | 10.05       | 10.55 |
| h     | 0.25        | 0.75  |
| L     | 0.50        | 0.90  |
| theta | 0°          | 7°    |

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