# **Sensitive Gate TRIACS**

# **Silicon Bidirectional Thyristors**

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

- Small Size Surface Mount DPAK Package
- Passivated Die for Reliability and Uniformity
- Four–Quadrant Triggering
- · Blocking Voltage to 600 V
- On-State Current Rating of 4.0 Amperes RMS at 93°C
- · Low Level Triggering and Holding Characteristics

#### **ORDERING INFORMATION**

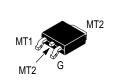
- To Obtain "DPAK" in Surface Mount Leadform (Case 369A)
   Shipped in 16 mm Tape and Reel Add "T4" Suffix to Device Number,
   i.e. MAC4DHMT4
- To Obtain "DPAK" in Straight Lead Version (Case 369) Shipped in Sleeves Add "-1" Suffix to Device Number, i.e. MAC4DHM-1

# MAC4DHM MAC4DLM

Motorola Preferred Devices

TRIACS 4.0 AMPERES RMS 600 VOLTS

MT2



CASE 369A-13 STYLE 6

### **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Peak Repetitive Off–State Voltage (1) (T <sub>J</sub> = -40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open)	MAC4DHM MAC4DLM	VDRM	600 600	Volts
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, T <sub>C</sub> = 93°C)		<sup>I</sup> T(RMS)	4.0	Amps
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T <sub>J</sub> = 110°C)		ITSM	40	
Circuit Fusing Consideration (t = 8.3 msec)		l <sup>2</sup> t	6.6	A <sup>2</sup> sec
Peak Gate Power (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 93°C)		$P_{GM}$	0.5	Watts
Average Gate Power (t = 8.3 msec, T <sub>C</sub> = 93°C)		P <sub>G(AV)</sub>	0.1	
Peak Gate Current (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 93°C)		I <sub>GM</sub>	0.2	Amps
Peak Gate Voltage (Pulse Width ≤ 10 μsec, T <sub>C</sub> = 93°C)		V <sub>GM</sub>	5.0	Volts
Operating Junction Temperature Range		TJ	-40 to 110	°C
Storage Temperature Range		T <sub>stg</sub>	-40 to 150	

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (2)	$R_{ heta$ JC $R_{ heta}$ JA	3.5 88 80	°C/W
Maximum Lead Temperature for Soldering Purposes (3)	TL	260	°C

- (1) V<sub>DRM</sub> for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.
- (2) Surface mounted on minimum recommended pad size.
- (3) 1/8" from case for 10 seconds.

**Preferred** devices are Motorola recommended choices for future use and best overall value.

REV 1



## **MAC4DHM MAC4DLM**

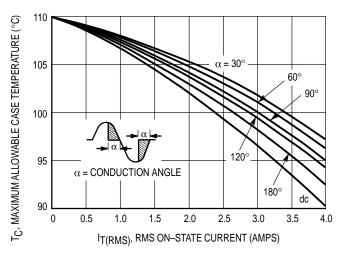
# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Characteristics	Symbol	Min	Тур	Max	Unit
Peak Repetitive Blocking Current ( $V_D$ = Rated $V_{DRM}$ , Gate Open) $T_J$ = 25°C $T_J$ = 110°C	IDRM		_	0.01 2.0	mA
Peak On–State Voltage (1) (I <sub>TM</sub> = ±6.0 A)	V <sub>TM</sub>	_	1.3	1.6	Volts
Gate Trigger Current (Continuous dc) ( $V_D$ = 12 V, $R_L$ = 100 $\Omega$ )  MT2(+), G(+) MAC4DLM  MT2(+), G(-)  MT2(-), G(-)  MT2(-), G(+)  MT2(+), G(+) MAC4DHM  MT2(+), G(-)  MT2(-), G(-)  MT2(-), G(-)	<sup>I</sup> GT	-	1.8 2.1 2.4 4.2 1.8 2.1 2.4 4.2	3.0 3.0 3.0 5.0 5.0 5.0 5.0	mA
Gate Trigger Voltage (Continuous dc) ( $V_D$ = 12 V, $R_L$ = 100 $\Omega$ ) MT2(+), G(+) MT2(+), G(-) MT2(-), G(-) MT2(-), G(+) ( $V_D$ = 12 V, $R_L$ = 10 K $\Omega$ , $T_J$ = 110°C) MT2(+), G(+); MT2(+), G(-); MT2(-), G(-); MT2(-), G(+)	VGT	0.5 0.5 0.5 0.5	0.62 0.57 0.65 0.74	1.3 1.3 1.3 1.3	Volts
Holding Current ( $V_D = 12 \text{ V}$ , Gate Open, $I_T = \pm 200 \text{ mA}$ )	lн	_	1.5	15	mA
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	ΙL	_ _ _ _	1.75 5.2 2.1 2.2	10 10 10 10	mA

## **DYNAMIC CHARACTERISTICS**

Characteristics	Symbol	Min	Тур	Max	Unit
Rate of Change of Commutating Current (1) (V <sub>D</sub> = 200 V, I <sub>TM</sub> = 1.8 A, Commutating dv/dt = 1.0 V/ $\mu$ sec, T <sub>J</sub> = 110°C, f = 250 Hz, CL = 5.0 $\mu$ fd, LL = 80 mH, RS = 56 $\Omega$ , CS = 0.03 $\mu$ fd) See Figure 10	di/dt(c)	_	3.0	_	A/ms
Critical Rate of Rise of Off–State Voltage $(V_D = 0.67 \text{ X Rated V}_{DRM}, \text{Exponential Waveform}, \\ \text{Gate Open, T}_J = 110^{\circ}\text{C})$	dv/dt	_	10	_	V/μs

<sup>(1)</sup> Pulse test: Pulse Width ≤ 2.0 msec, Duty Cycle ≤ 2%.





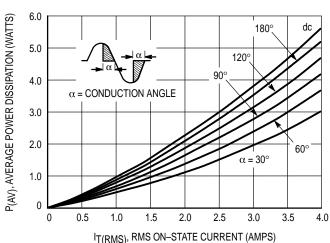


Figure 2. On-State Power Dissipation

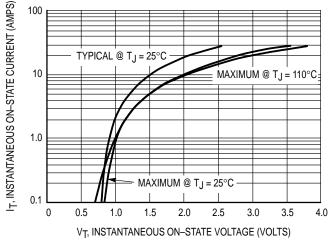
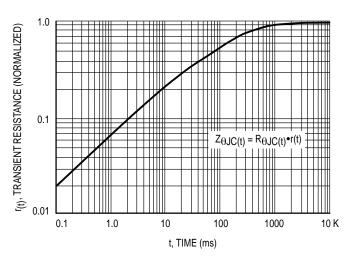


Figure 3. On-State Characteristics



**Figure 4. Transient Thermal Response** 

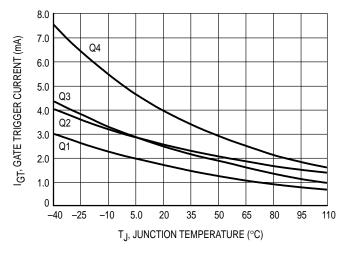


Figure 5. Typical Gate Trigger Current versus
Junction Temperature

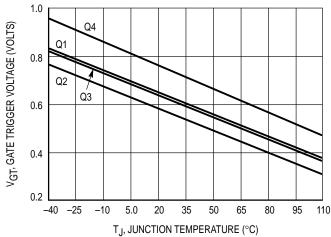


Figure 6. Typical Gate Trigger Voltage versus
Junction Temperature

#### **MAC4DHM MAC4DLM**

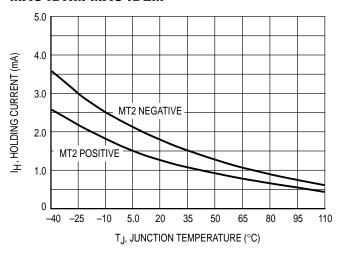


Figure 7. Typical Holding Current versus Junction Temperature

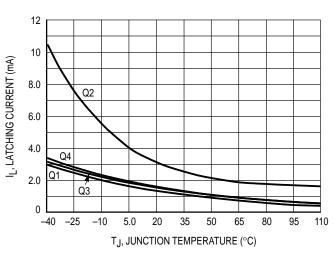


Figure 8. Typical Latching Current versus Junction Temperature

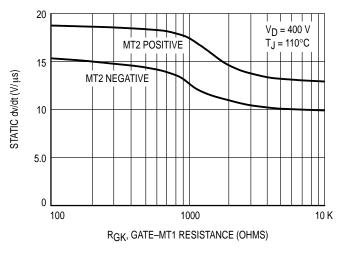


Figure 9. Exponential Static dv/dt versus Gate-MT1 Resistance, MT2(+)

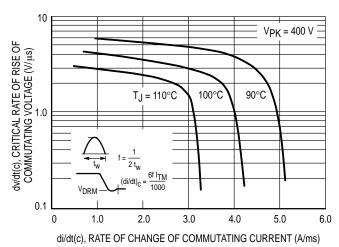
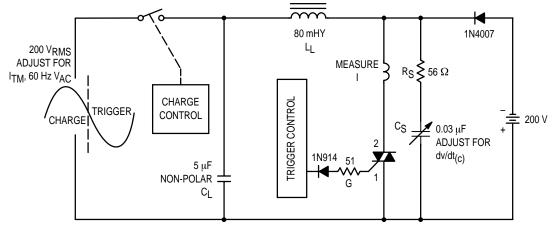


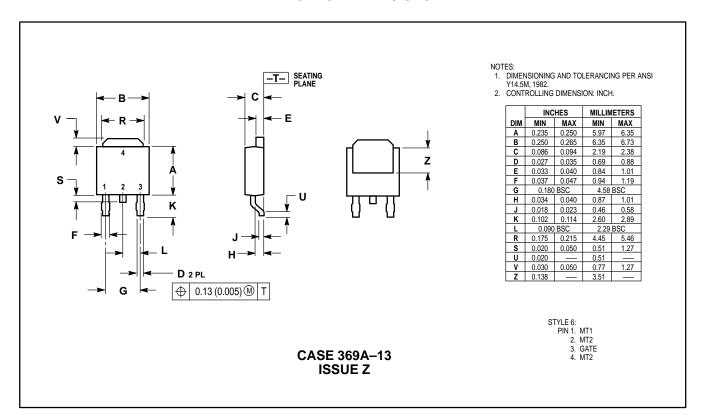
Figure 10. Critical Rate of Rise of Commutating Voltage



Note: Component values are for verification of rated (dv/dt)<sub>C</sub>. See AN1048 for additional information.

Figure 11. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage

## **PACKAGE DIMENSIONS**



# **NOTES**

#### **MAC4DHM MAC4DLM**

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