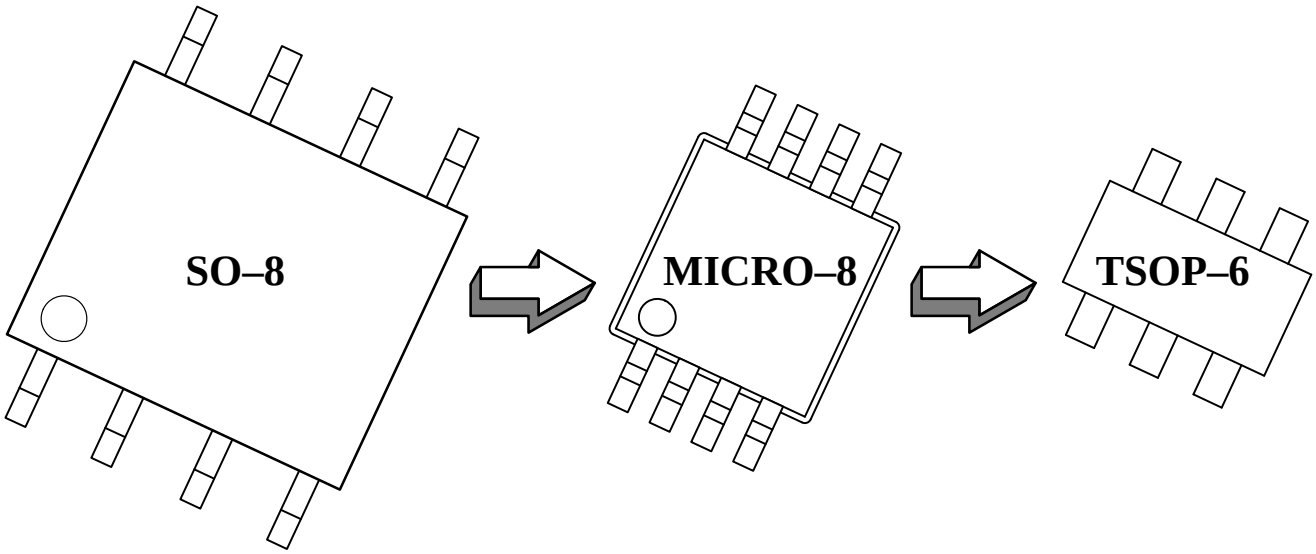
APRIL 1997 BR1491/D

MOTOROLA

TSOP–6



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Selector Guide

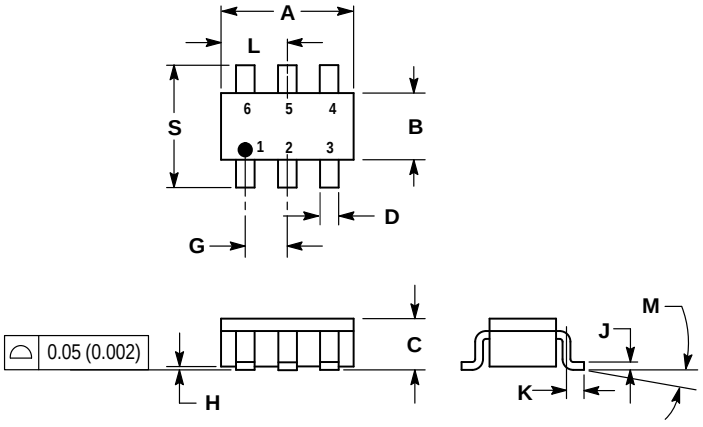
Part Number	Maximum Ratings					Configuration	Available
	V_{DS} (V)	$R_{DS(on)}$ (Ω)			I_{DS} (A)		
		V_{GS} = 10 V	V_{GS} = 4.5 V	V_{GS} = 2.5 V			
MGSF3454VT1	30	0.065	0.095		±4.2	N–Channel	July 97
MGSF3454XT1	30	0.065	0.095		±1.75	N–Channel	Now
MGSF3455VT1	30	0.10	0.19		±3.5	P–Channel	July 97
MGSF3455XT1	30	0.10	0.19		±1.45	P–Channel	July 97
MGSF3442VT1	20		0.07	0.095	±4.0	N–Channel	July 97
MGSF3442XT1	20		0.07	0.095	±1.7	N–Channel	July 97
MGSF3441VT1	20		0.10	0.135	±3.3	P–Channel	July 97
MGSF3441XT1	20		0.10	0.135	±1.5	P–Channel	July 97

Table of Contents

TSOP–6

Cellular telephones, notebook computers, and other portable electronic systems are becoming smaller with each new generation of products. The new TSOP–6 family anticipates this evolution. Its small size allows the placement of a MOSFET in spaces that have become too small for any other surface–mount power MOSFET package.

With a power rating of 2.0 W, on–resistance as low as 0.065 Ω, and current ratings of up to 4.2 A, the new TSOP–6 (Figure 1) is a true power package, providing the kind of performance, on an even smaller scale, that designers have come to expect from TSOP–6.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

Figure 1. TSOP–6 Outline Drawing

Not only is the TSOP–6 small, it's also a JEDEC registered package. It has the same footprint as the SC–59, but with a lower profile and higher power rating (up to 2.0 W). As further assurance that the TSOP–6 will be established as the industry standard for low–voltage applications with limited circuit board space, these devices are being second–sourced by TEMIC Semiconductor. For these TSOP–6 devices, TEMIC Semiconductor and Motorola have agreed on compatible pin–outs, power ratings, and package outlines and dimensions.

New Branch of a Great Family

When the first true surface–mount power MOSFETs were created in the SO–8 family, two innovations were involved, 1) a lower on–resistance power MOSFET technology, 2) modified standard surface–mount SOIC package. The lower on–resistance MOSFET reduced the power dissipation per unit of current, while the innovative packaging provided a path for heat to escape, allowing high currents to be switched in a package that is much smaller and easier to assemble.

The introduction of smaller MOSFETs in the SO–8 inevitably raised the expectations of the market as regards surface–mounted power MOSFETs, resulting in a demand for devices with greater capabilities in even smaller packages. In 1994, the size of the smallest available power MOSFET was halved with the introduction of the MICRO–8.

This introduction answered the demand of the market for smaller size and greater capabilities with even smaller devices that provide the current handling available until now only in the MICRO–8, SO–8 and other larger packages.

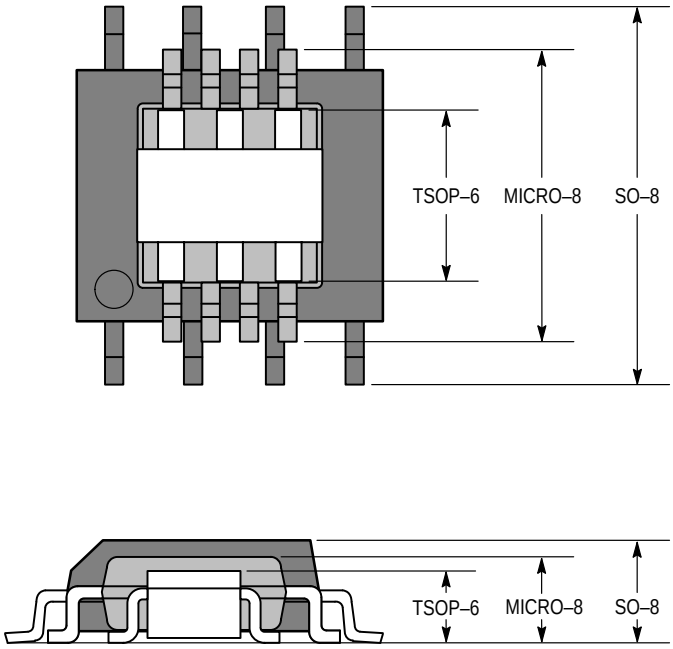


Figure 2. Family Package Evolution

The TSOP–6 is a 6–leaded, 1 mm thick package with a total height of 1.1 mm. The package and leads occupy an area of 2.75 X 3.10 mm. To put this in perspective, Figure 2 gives a visual comparison by overlaying the package outlines of the TSOP–6, the MICRO–8 and the SO–8 packages. The TSOP–6 measures 2.75 mm in width, including the leads, less than half as wide as the SO–8. Table 1 gives a comparison of the dimensions of these packages.

Table 1. Comparison of Dimensions

Dim	TSOP–6				MICRO–8				SOIC–8			
	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Height	—	1.10	—	0.043	1.05	1.20	0.041	0.047	1.35	1.75	0.053	0.069
Lead Width	0.25	0.50	0.010	0.020	0.25	0.30	0.010	0.012	0.35	0.45	0.014	0.018
Package Length	2.90	3.10	0.114	0.122	2.90	3.10	0.114	0.122	4.69	5.00	0.185	0.196
Package Width	1.30	1.70	0.051	0.067	4.30	4.50	0.170	0.177	3.50	4.05	0.140	0.160
Width of Foot Print	2.75BSC		0.0108BSC		6.20	6.60	0.244	0.260	5.70	6.30	0.224	0.248
Lead Pitch	1.00BSC		0.039BSC		0.065BSC		0.025BSC		1.27BSC		0.050BSC	

Thermal Capabilities

The same copper lead frame innovations introduced in the SO–8 have been used in the TSOP–6 to dissipate heat. The TSOP–6 lead frame is shown in Figure 3. As in the SO–8 and MICRO–8 packages, the thermal path runs from the die, through the die attach, into the copper lead frame, and out the drain leads (Figure 4). The drain lead accounts for the largest portion of the thermal impedance due to the small cross sectional area of the leads. The small size of the package helps to keep the length of the drain leads short. The short lead length, in combination with the use of four drain leads, keeps the thermal impedance low for this size package.

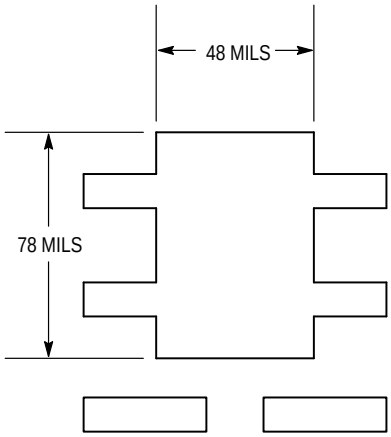


Figure 3. TSOP–6 Lead Frame

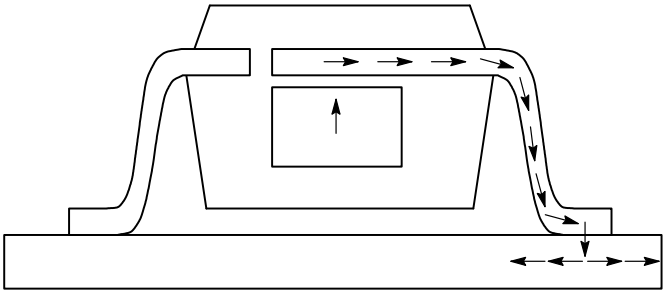


Figure 4. Thermal Path

The thermal rating (as provided on data sheets for surface–mount MOSFETs) is measured with the part mounted on a one–inch square piece of 0.062 inch thick FR4 PC board. This choice of test board is neither a “worst–case” or “best–case” layout. It represents a compromise between single–layer and multilayer boards, with more copper on its single side than the average single–layer construction. Thus, it can serve as an approximation of multilayer boards with center power planes and far less surface copper.

The junction is heated by a known amount of power for a known amount of time. The junction temperature is measured immediately after heating using the temperature coefficient of the forward voltage of the internal diode. This procedure is repeated from a time of 5 ms out to several hundred seconds. This series of measurements and measurement of the ambient temperature provides $R_{\theta JA}$, the single pulse power curve, and provides the data required to generate the transient thermal impedance curves from junction to ambient.

Two Versions: 0.95 W and 2.0 W

Each TSOP–6 device is available in two versions with different thermal ratings. The rating is dependent on the lead frame material used. The parts with the “V” suffix are built with a copper leadframe which gives the best thermal performance. The parts with the “X” suffix have a copper plated Alloy 42 leadframe. Although the “X” series devices are rated with the same electrical resistance as the “V” series devices, they are specified at a reduced current level to compensate for their increased thermal impedance.

The first thermal performance parameter that is normally seen is $R_{\theta JA}$. This parameter gives a means of comparing the package capability before the PC board starts to have a significant effect. For the TSOP–6, the board is considered to dominate after 5 seconds. $R_{\theta JA}$ for the TSOP–6 is 62.5°C/W for the “V” parts and 132°C/W for the “X” parts. The “V” parts, which have the copper lead frame compare very favorably with 50°C/W for the single–die SO–8, 62.5°C/W for the dual–die SO–8.

A comparison of the single–pulse power curves (Figure 5) reveals the difference in the thermal mass of the TSOP–6 and the SO–8 die and lead frames, and therefore, in ability of these two packages to handle surge currents. The single–pulse power curve shows the amount of power it takes for a single pulse of fixed duration to raise the junction temperature from room temperature to 150°C. If extended below 10 ms, the curves would become asymptotic and converge, reflecting the limitations of the die alone. The opposite end of the curve reflects the limitations of the PC mass of the TSOP–6 results in a significant but reduced capability in pulse duration, amounting to less than 5 seconds. It should be noted that the TSOP–6 can dissipate a 20–W pulse of 10–ms duration.

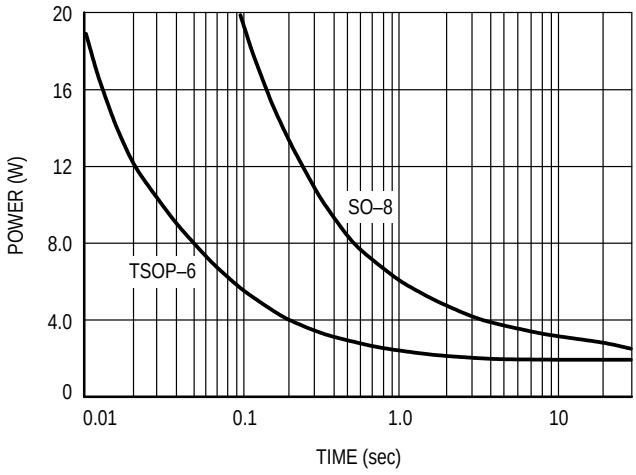


Figure 5. Single Pulse Power

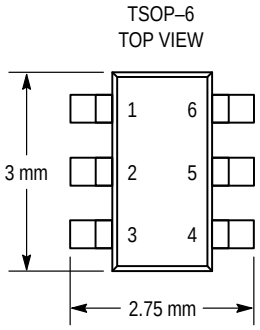
The combination of very low on–resistance power MOSFET technology, and a thermally efficient copper leadframe in the new TSOP–6 package creates a new standard for performance per footprint. For applications requiring very low on–resistance, at less current, the Alloy 42–leadframes offer manufacturing advantages that make them even more economical.

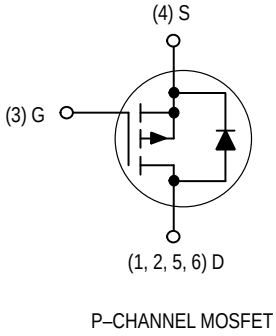
P–Channel Enhancement–Mode MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
– 20	0.10 @ V_{GS} = – 4.5 V	± 3.3
	0.135 @ V_{GS} = – 2.5 V	± 2.9

2.5–V Rated





Power Dissipation
MGSF3441VT1 – 2.0 W

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain–Source Voltage		V_{DS}	–20	V
Gate–Source Voltage		V_{GS}	± 8.0	
Continuous Drain Current (T_J = 150°C) (1)	T_A = 25°C	I_D	± 3.3	A
	T_A = 70°C		± 2.6	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction) (1)		I_S	– 1.6	
Maximum Power Dissipation (1)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.28	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	– 55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction–to–Ambient (1)	$R_{\theta JA}$	62.5	°C/W

1. Surface Mounted on FR4 Board, t ≤ 5 sec.

Specifications (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	– 0.45			V
Gate–Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8.0 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –20 V, V_{GS} = 0 V			–1.0	μA
		V_{DS} = –20 V, V_{GS} = 0 V, T_J = 70°C			– 5.0	
On–State Drain Current (1)	$I_{D(on)}$	V_{DS} = – 5.0 V, V_{GS} = – 4.5 V	–10			A
		V_{DS} = – 5.0 V, V_{GS} = –2.5 V	– 4.0			
Drain Source On–State Resistance (1)	$R_{DS(on)}$	V_{GS} = – 4.5 V, I_D = 3.3 A		0.078	0.10	Ω
		V_{GS} = –2.5 V, I_D = 2.9 A		0.110	0.135	
Forward Transconductance (1)	g_{FS}	V_{DS} = –10 V, I_D = – 3.3 A		8.8		S
Diode Forward Voltage (1)	V_{SD}	I_S = –1.6 A, V_{GS} = 0 V		0.8	–1.2	V
Dynamic (2)						
Total Gate Charge	Q_g	V_{DS} = –10 V, V_{GS} = – 4.5 V, I_D = – 3.3 A		8.6	14	nC
Gate–Source Charge	Q_{gs}			1.5		
Gate–Drain Charge	Q_{gd}			3.1		
Turn–On Delay Time	$t_{d(on)}$	V_{DD} = –10 V, R_L = 10 Ω $I_D \cong$ –1.6 A, V_{GEN} = – 4.5 V, R_G = 6.0 Ω		27	50	ns
Rise Time	t_r			17	30	
Turn–Off Delay Time	$t_{d(off)}$			52	80	
Fall Time	t_f			45	70	
Source–Drain Reverse Recovery Time	t_{rr}	I_F = –1.6 A, di/dt = 100 A/μs		50	80	

1. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
2. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C unless otherwise noted)

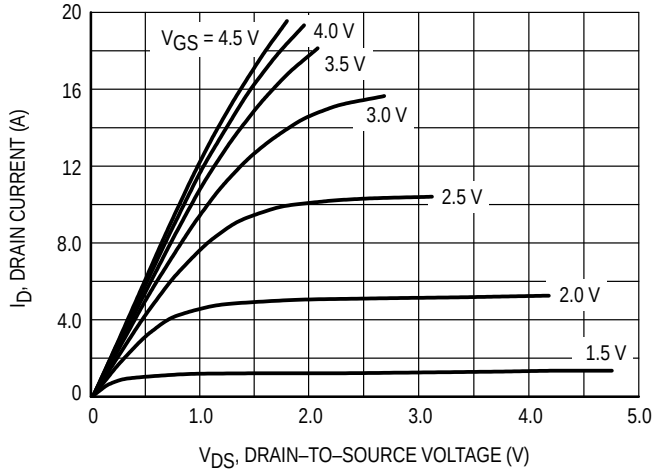


Figure 1. Output Characteristics

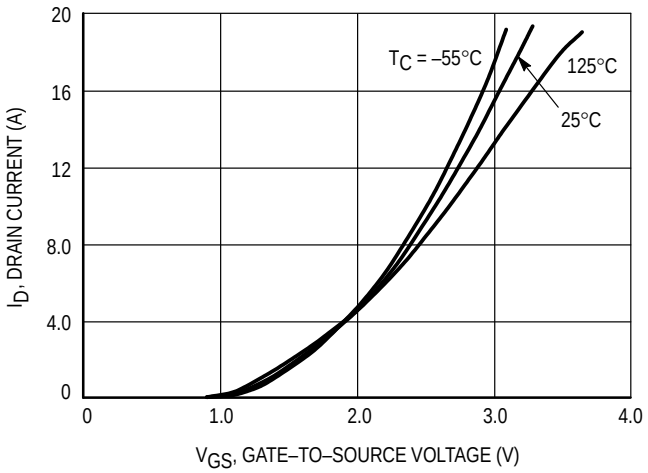


Figure 2. Transfer Characteristics

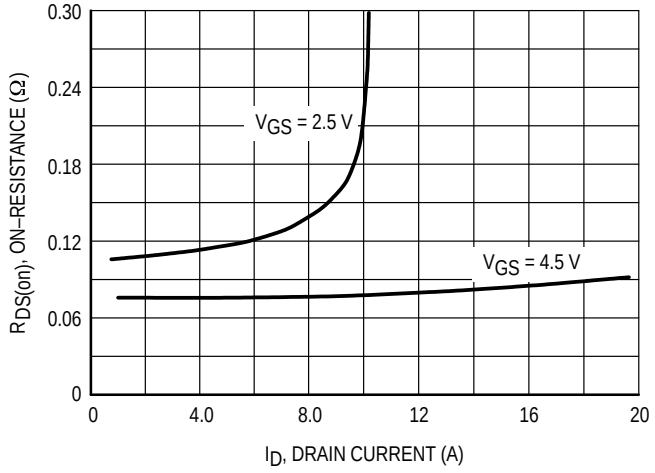


Figure 3. On–Resistance versus Drain Current

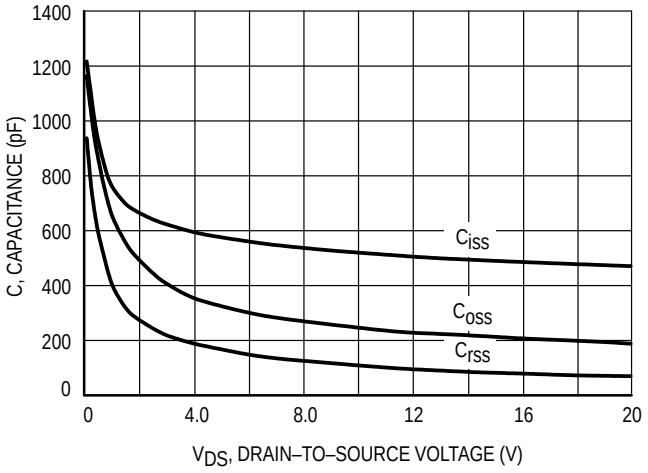


Figure 4. Capacitance

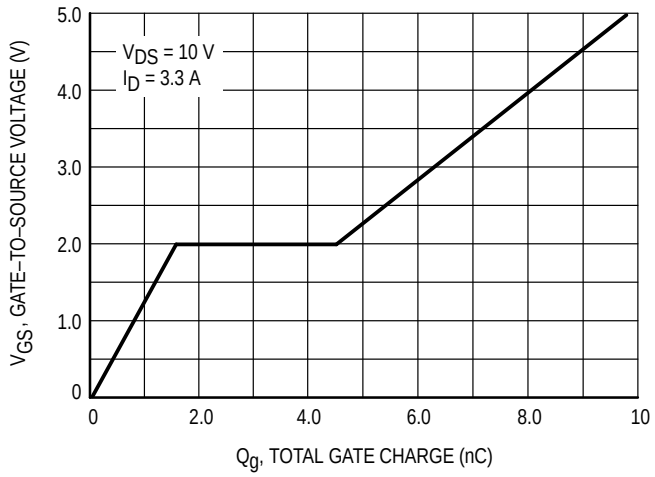


Figure 5. Gate Charge

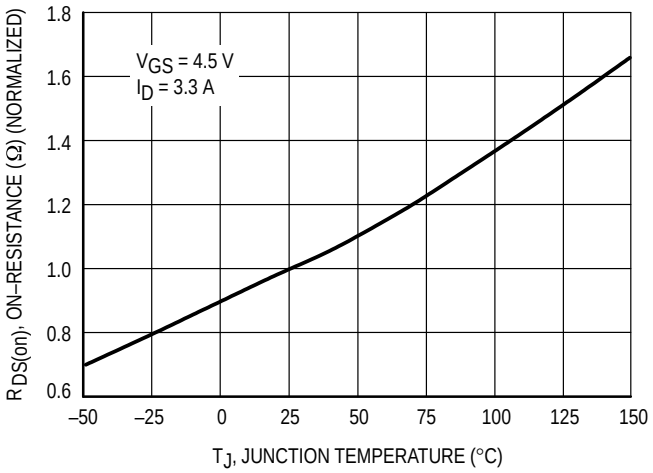


Figure 6. On–Resistance versus Junction Temperature

TYPICAL CHARACTERISTICS (25°C unless otherwise noted)

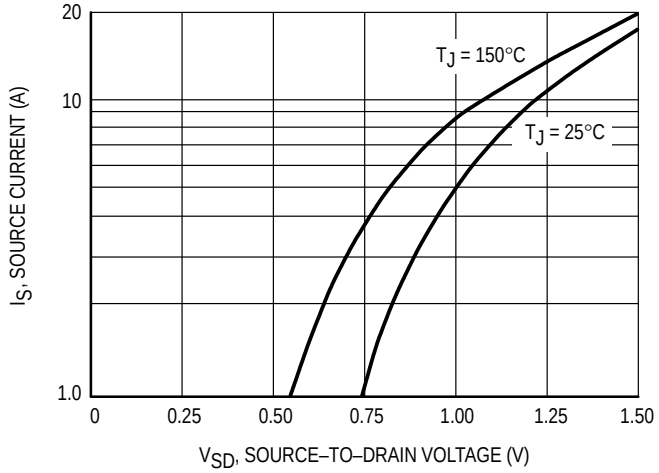


Figure 7. Source–Drain Diode Forward Voltage

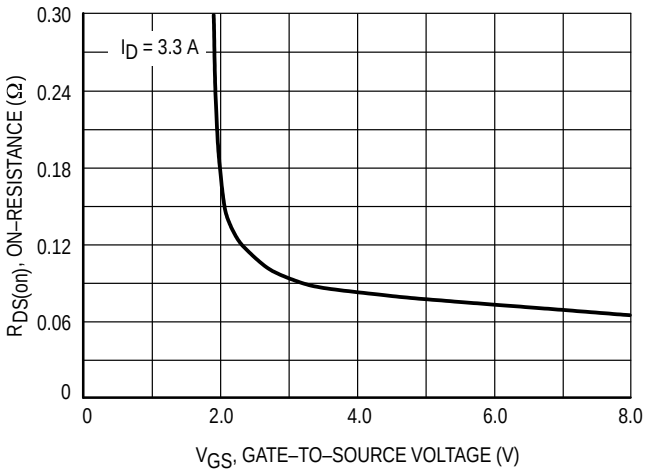


Figure 8. On–Resistance versus Gate–to–Source Voltage

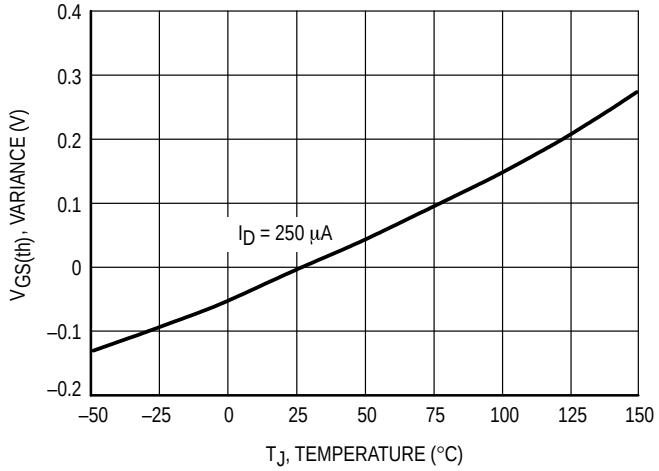


Figure 9. Threshold Voltage

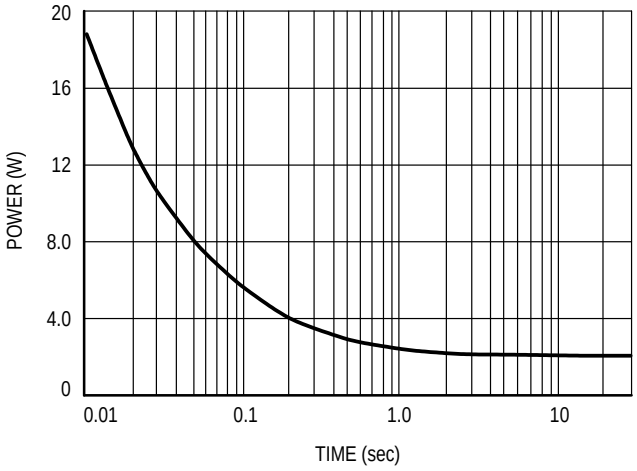


Figure 10. Single Pulse Power

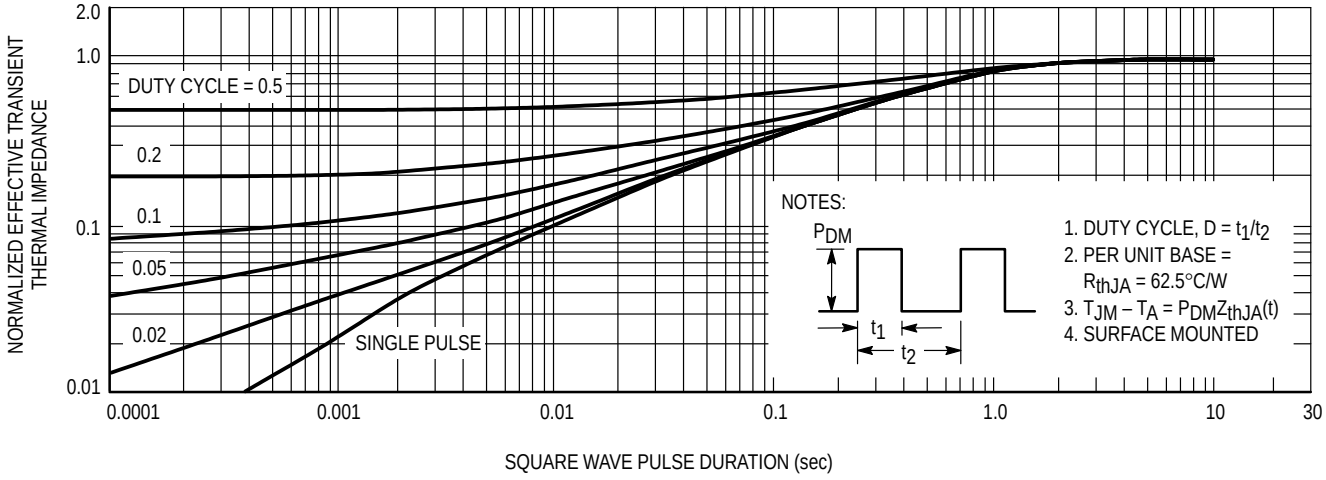


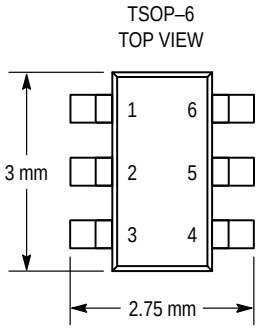
Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient

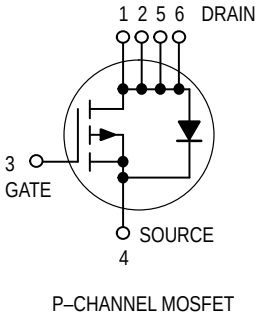
P–Channel Enhancement–Mode MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.100 @ V_{GS} = 4.5 V	± 1.5
	0.135 @ V_{GS} = 2.5 V	± 1.2

2.5–V Rated





P–CHANNEL MOSFET

Power Dissipation
MGSF3441XT1 – 0.95 W

Absolute Maximum Ratings (T$_J$ = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain–Source Voltage	V_{DSS}	20	Vdc
Gate–Source Voltage — Continuous	V_{GS}	± 8.0	
Drain Current — Continuous @ T_A = 25°C — Pulsed Drain Current ($t_p \leq 10$ μs)	I_D I_{DM}	1.5 20	A
Total Power Dissipation @ T_A = 25°C	P_D	950	mW
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Maximum Lead Temperature for Soldering Purposes, for 10 seconds	T_L	260	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction–to–Ambient (1)	$R_{\theta JA}$	132	°C/W

1. Surface Mounted on FR4 Board, t ≤ 5 sec.

Specifications (T_J = 25°C unless otherwise noted)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μA)		$V_{(BR)DSS}$	20	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 70°C)		I_{DSS}	— —	— —	1.0 4.0	μAdc
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0)		I_{GSS}	—	—	±100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	0.45	—	—	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 4.5 Vdc, I_D = 1.5 A) (V_{GS} = 2.5 Vdc, I_D = 1.2 A)		$R_{DS(on)}$	— —	0.078 0.110	0.100 0.135	Ohms
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 5.0 V)	C_{iss}	—	90	—	pF
Output Capacitance	(V_{DS} = 5.0 V)	C_{oss}	—	50	—	
Transfer Capacitance	(V_{DG} = 5.0 V)	C_{rss}	—	10	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 1.0 A, V_{GEN} = 10 V, R_L = 10 Ω)	$t_{d(on)}$	—	27	50	ns
Rise Time		t_r	—	17	30	
Turn–Off Delay Time		$t_{d(off)}$	—	52	80	
Fall Time		t_f	—	45	70	
Gate Charge		Q_T	—	3000	—	pC
SOURCE–DRAIN DIODE CHARACTERISTICS						
Continuous Current		I_S	—	—	1.0	A
Pulsed Current		I_{SM}	—	—	20	A
Forward Voltage(2)		V_{SD}	—	0.80	1.2	V

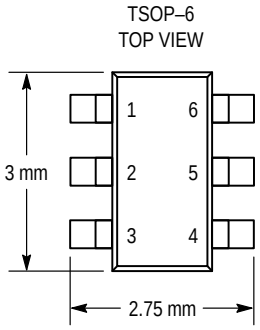
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

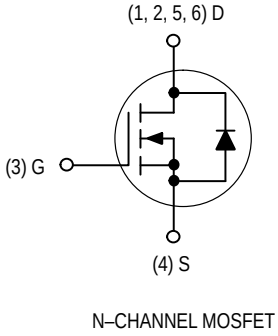
N–Channel Enhancement–Mode MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.07 @ V_{GS} = 4.5 V	± 4.0
	0.095 @ V_{GS} = 2.5 V	± 3.4

2.5–V Rated





Power Dissipation
MGSF3442VT1 – 2.0 W

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain–Source Voltage		V_{DS}	± 20	V
Gate–Source Voltage		V_{GS}	± 8.0	
Continuous Drain Current (T_J = 150°C) (1)	T_A = 25°C	I_D	± 4.0	A
	T_A = 70°C		± 3.1	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction) (1)		I_S	± 1.6	
Maximum Power Dissipation (1)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.28	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	– 55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction–to–Ambient (1)	$R_{\theta JA}$	62.5	°C/W

1. Surface Mounted on FR4 Board, t ≤ 5 sec.

Specifications (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	0.6			V
Gate–Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8.0 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1.0	μA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 70°C			5.0	
On–State Drain Current (1)	$I_{D(on)}$	V_{DS} = 5.0 V, V_{GS} = 4.5 V	10			A
		V_{DS} = 5.0 V, V_{GS} = 2.5 V	4.0			
Drain–Source On–State Resistance (1)	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.0 A		0.058	0.07	Ω
		V_{GS} = 2.5 V, I_D = 3.4 A		0.072	0.095	
Forward Transconductance (1)	g_{FS}	V_{DS} = 10 V, I_D = 4.0 A		11.3		S
Diode Forward Voltage (1)	V_{SD}	I_S = 1.6 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic (2)						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 4.0 A		7.0	10	nC
Gate–Source Charge	Q_{gs}			1.1		
Gate–Drain Charge	Q_{gd}			2.0		
Turn–On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1.0 A, V_{GEN} = 4.5 V, R_G = 6.0 Ω		8.0	20	ns
Rise Time	t_r			24	40	
Turn–Off Delay Time	$t_{d(off)}$			35	60	
Fall Time	t_f			10	20	
Source–Drain Reverse Recovery Time	t_{rr}	I_F = 1.6 A, di/dt = 100 A/μs		40	70	

1. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
2. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C unless otherwise noted)

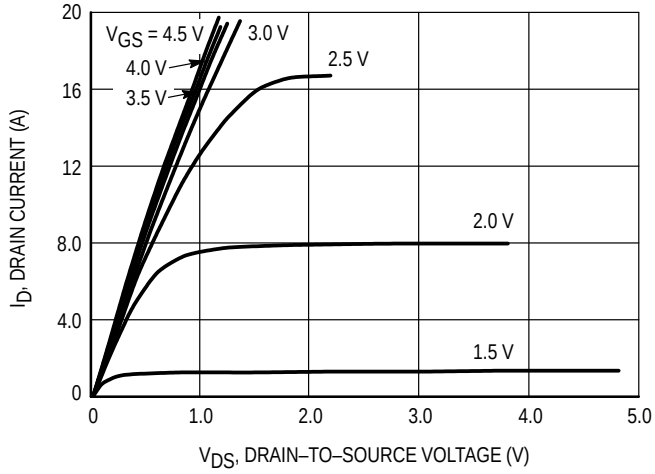


Figure 1. Output Characteristics

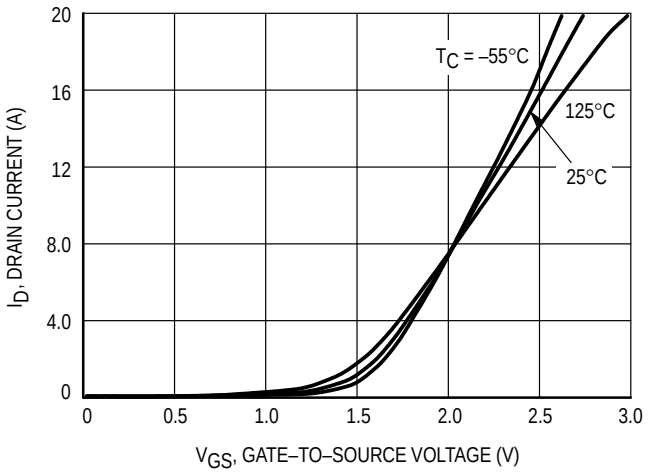


Figure 2. Transfer Characteristics

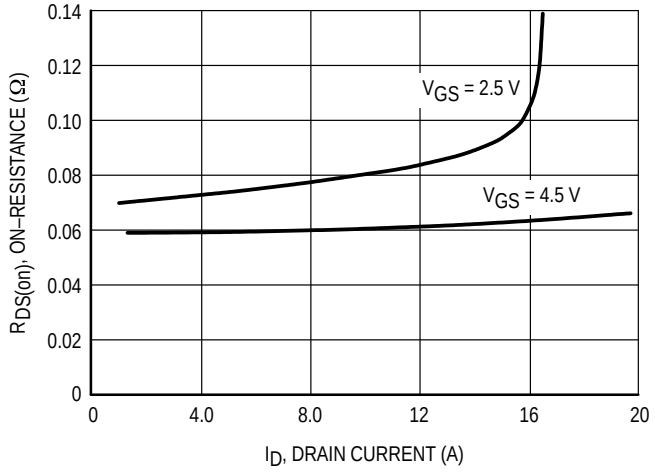


Figure 3. On–Resistance versus Drain Current

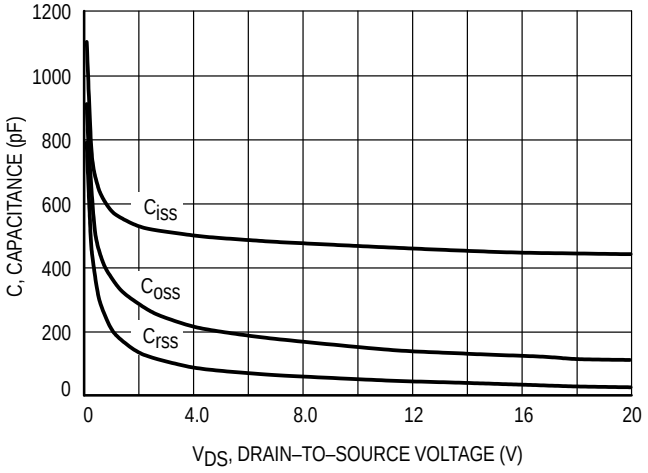


Figure 4. Capacitance

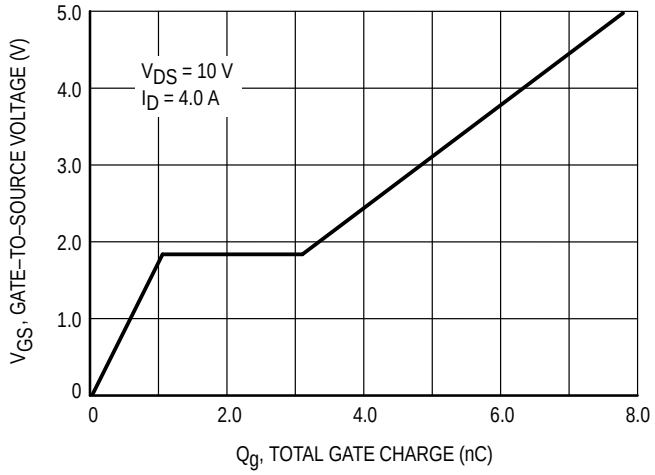


Figure 5. Gate Charge

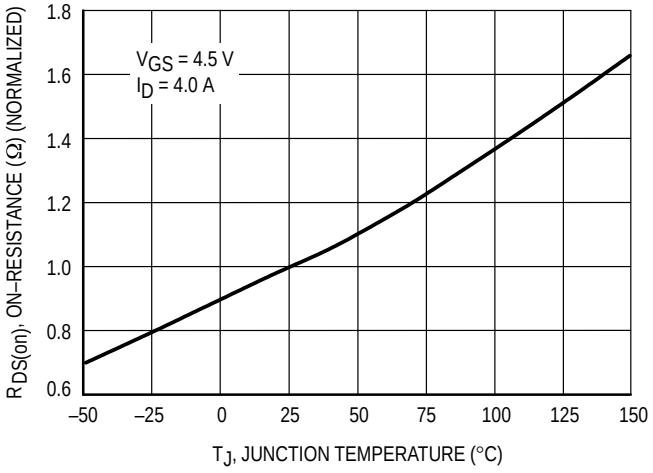


Figure 6. On–Resistance versus Junction Temperature

TYPICAL CHARACTERISTICS (25°C unless otherwise noted)

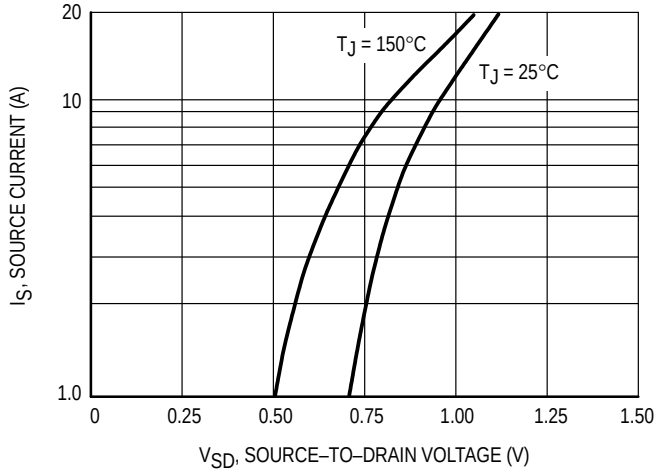


Figure 7. Source–Drain Diode Forward Voltage

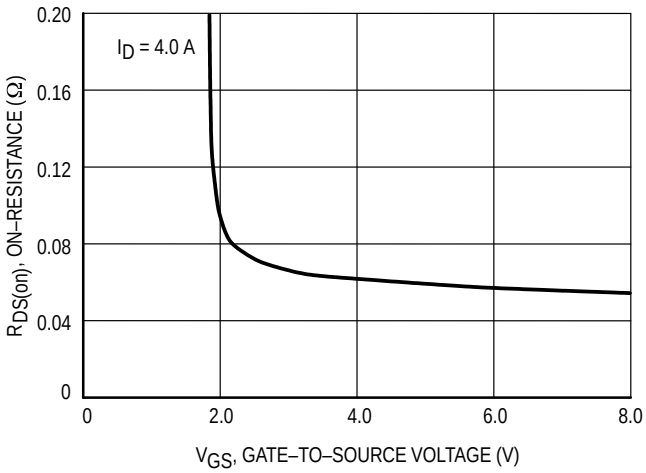


Figure 8. On–Resistance versus Gate–to–Source Voltage

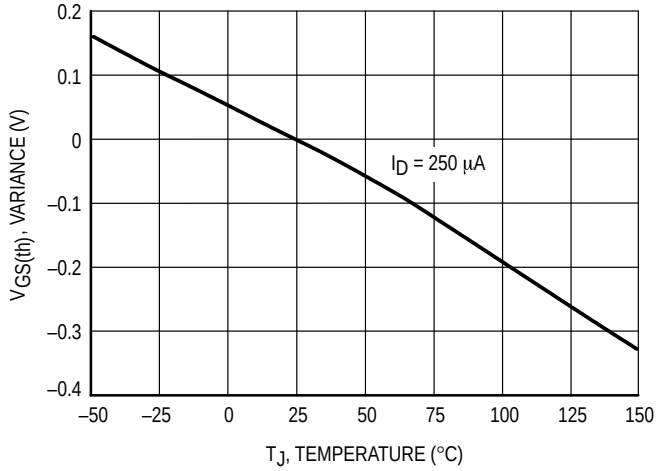


Figure 9. Threshold Voltage

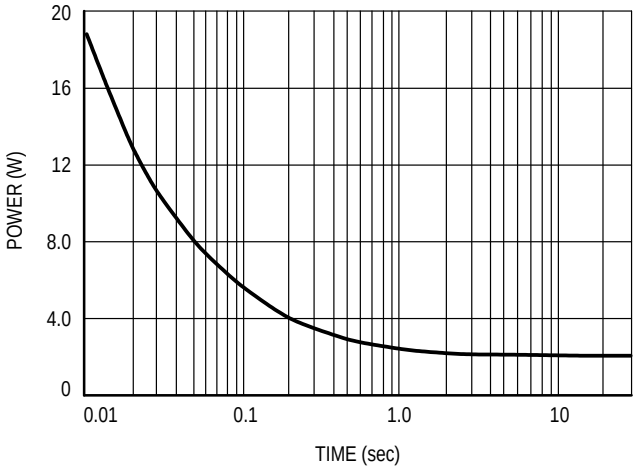


Figure 10. Single Pulse Power

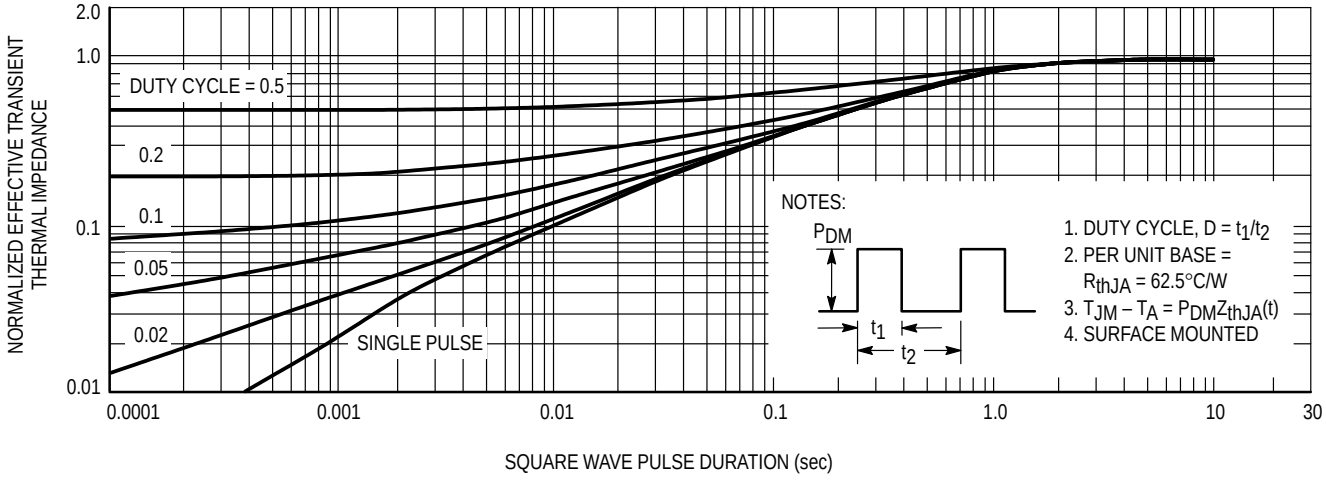


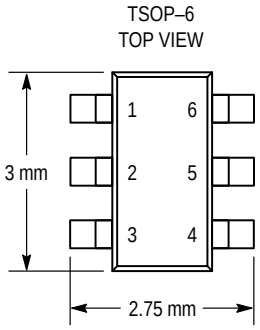
Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient

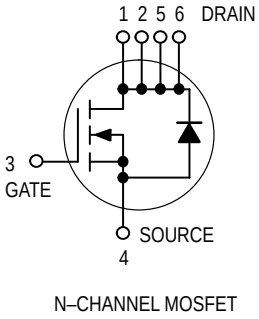
N–Channel Enhancement–Mode MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.070 @ V_{GS} = 4.5 V	± 1.7
	0.095 @ V_{GS} = 2.5 V	± 1.3

2.5–V Rated





Power Dissipation
MGSF3442XT1 – 0.95 W

Absolute Maximum Ratings (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain–Source Voltage	V_{DSS}	20	Vdc
Gate–Source Voltage — Continuous	V_{GS}	± 8.0	
Drain Current — Continuous @ T_A = 25°C — Pulsed Drain Current ($t_p \le 10$ μs)	I_D I_{DM}	1.7 20	A
Total Power Dissipation @ T_A = 25°C	P_D	950	mW
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Maximum Lead Temperature for Soldering Purposes, for 10 seconds	T_L	260	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction–to–Ambient (1)	$R_{\theta JA}$	132	°C/W

1. Surface Mounted on FR4 Board, t ≤ 5 sec.

Specifications (T_J = 25°C unless otherwise noted)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

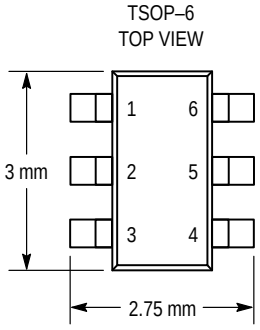
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μA)		$V_{(BR)DSS}$	20	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 70°C)		I_{DSS}	— —	— —	1.0 5.0	μAdc
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0)		I_{GSS}	—	—	±100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	0.6	—	—	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 4.5 Vdc, I_D = 1.7 A) (V_{GS} = 2.5 Vdc, I_D = 1.3 A)		$R_{DS(on)}$	— —	0.058 0.072	0.070 0.095	Ohms
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 5.0 V)	C_{iss}	—	90	—	pF
Output Capacitance	(V_{DS} = 5.0 V)	C_{oss}	—	50	—	
Transfer Capacitance	(V_{DG} = 5.0 V)	C_{rss}	—	10	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 1.0 A, V_{GEN} = 10 V, R_L = 10 Ω)	$t_{d(on)}$	—	8.0	20	ns
Rise Time		t_r	—	24	40	
Turn–Off Delay Time		$t_{d(off)}$	—	36	60	
Fall Time		t_f	—	10	20	
Gate Charge		Q_T	—	—	—	nC
SOURCE–DRAIN DIODE CHARACTERISTICS						
Continuous Current		I_S	—	—	1.0	A
Pulsed Current		I_{SM}	—	—	5.0	A
Forward Voltage(2)		V_{SD}	—	—	1.2	V

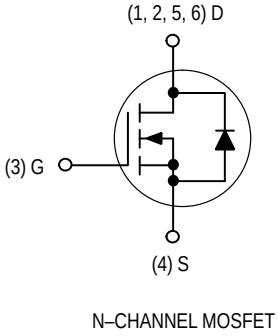
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

N–Channel Enhancement–Mode MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.065 @ V_{GS} = 10 V	± 4.2
	0.095 @ V_{GS} = 4.5 V	± 3.4





Power Dissipation
MGSF3454VT1 – 2.0 W

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain–Source Voltage		V_{DS}	± 30	V
Gate–Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C) (1)	T_A = 25°C	I_D	± 4.2	A
	T_A = 70°C		± 3.4	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction) (1)		I_S	± 1.7	
Maximum Power Dissipation (1)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	– 55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction–to–Ambient (1)	$R_{\theta JA}$	62.5	°C/W

1. Surface Mounted on FR4 Board, t ≤ 5 sec.

Specifications (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	1.0			V
Gate–Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1.0	μA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 70°C			25	
On–State Drain Current (1)	$I_{D(on)}$	V_{DS} = 5.0 V, V_{GS} = 10 V	15			A
Drain–Source On–State Resistance (1)	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4.2 A		0.050	0.065	Ω
		V_{GS} = 4.5 V, I_D = 3.4 A		0.070	0.095	
Forward Transconductance (1)	g_{FS}	V_{DS} = 10 V, I_D = 4.2 A		7.0		S
Diode Forward Voltage (1)	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V			1.2	V
Dynamic (2)						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 4.2 A		8.0	15	nC
Gate–Source Charge	Q_{gs}			1.8		
Gate–Drain Charge	Q_{gd}			1.3		
Turn–On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω, I_D ≅ 1.0 A, V_{GEN} = 10 V, R_G = 6.0 Ω		10	20	ns
Rise Time	t_r			15	30	
Turn–Off Delay Time	$t_{d(off)}$			20	35	
Fall Time	t_f			10	20	
Source–Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/μs		50	80	

1. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
2. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C unless otherwise noted)

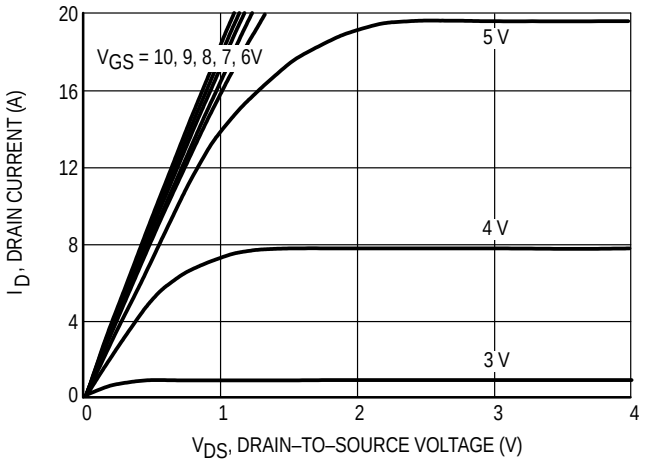


Figure 1. Output Characteristics

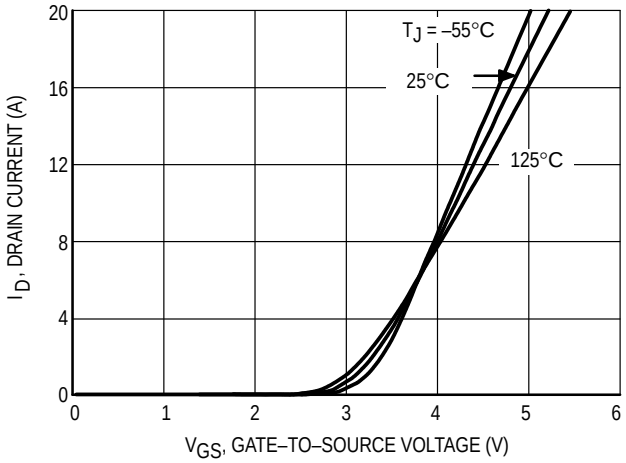


Figure 2. Transfer Characteristics

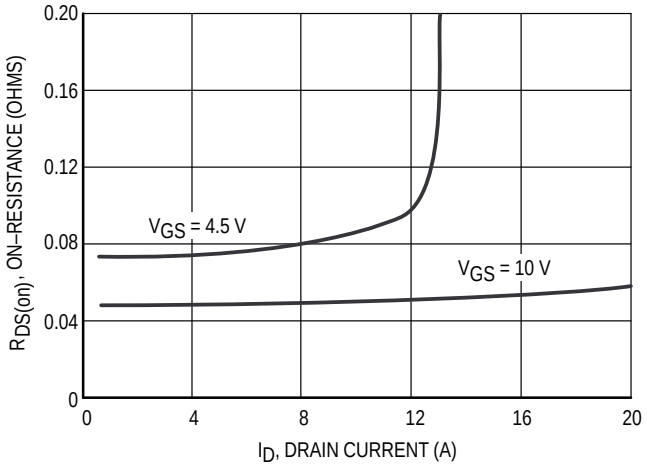


Figure 3. On–Resistance vs. Drain Current

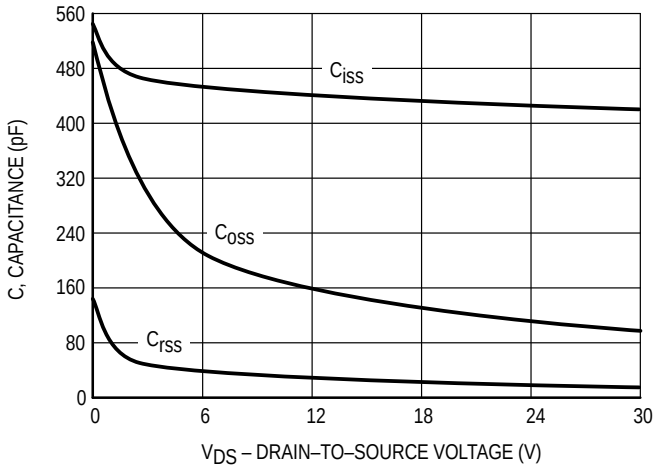


Figure 4. Capacitance

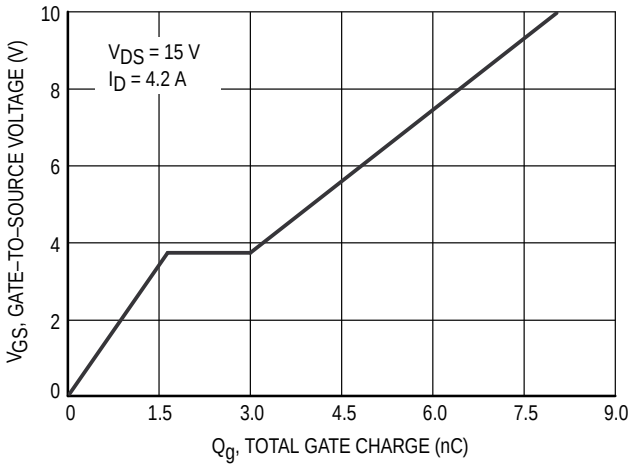


Figure 5. Gate Charge

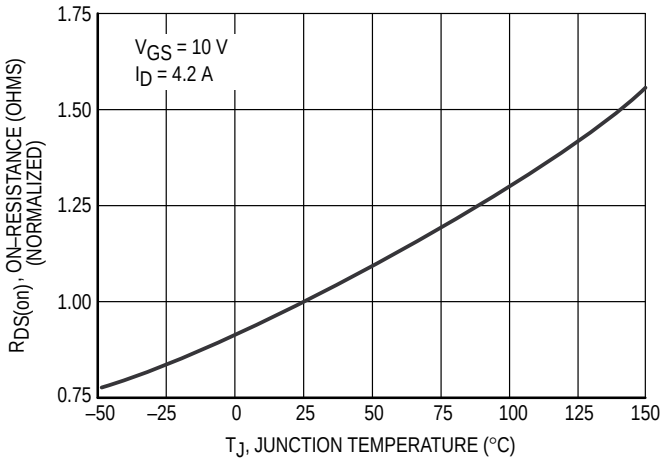


Figure 6. On–Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25°C unless otherwise noted)

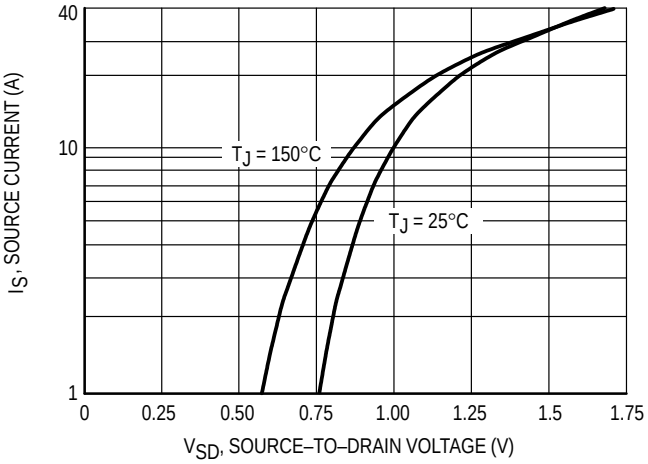


Figure 7. Source–Drain Diode Forward Voltage

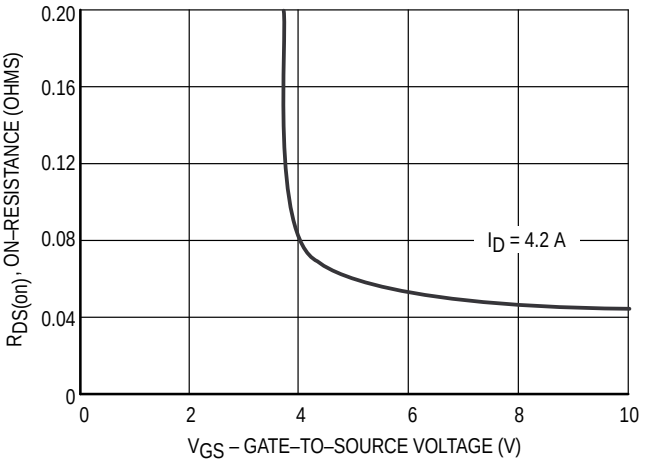


Figure 8. On–Resistance vs. Gate–to–Source Voltage

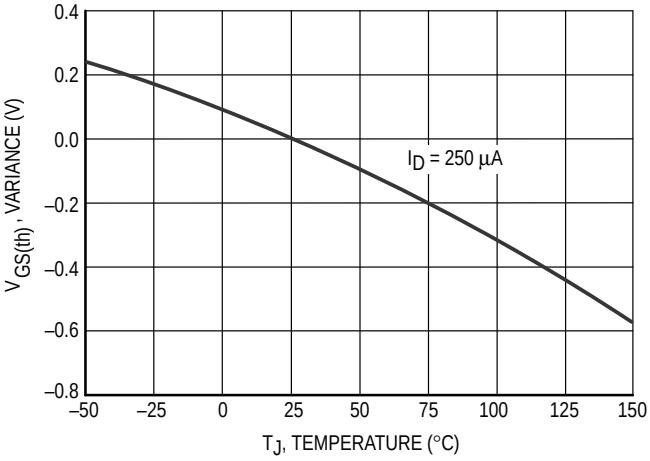


Figure 9. Threshold Voltage

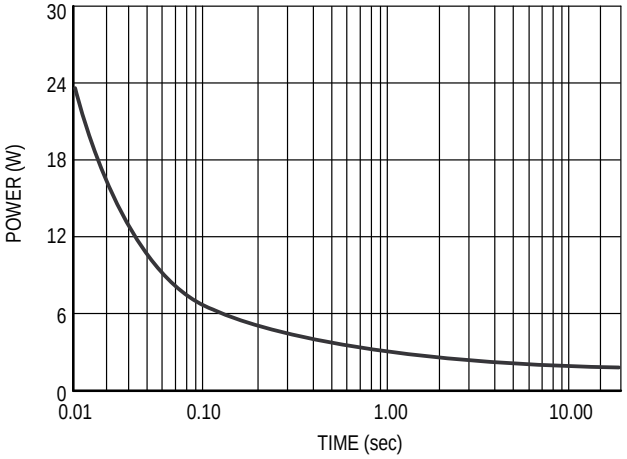


Figure 10. Single Pulse Power

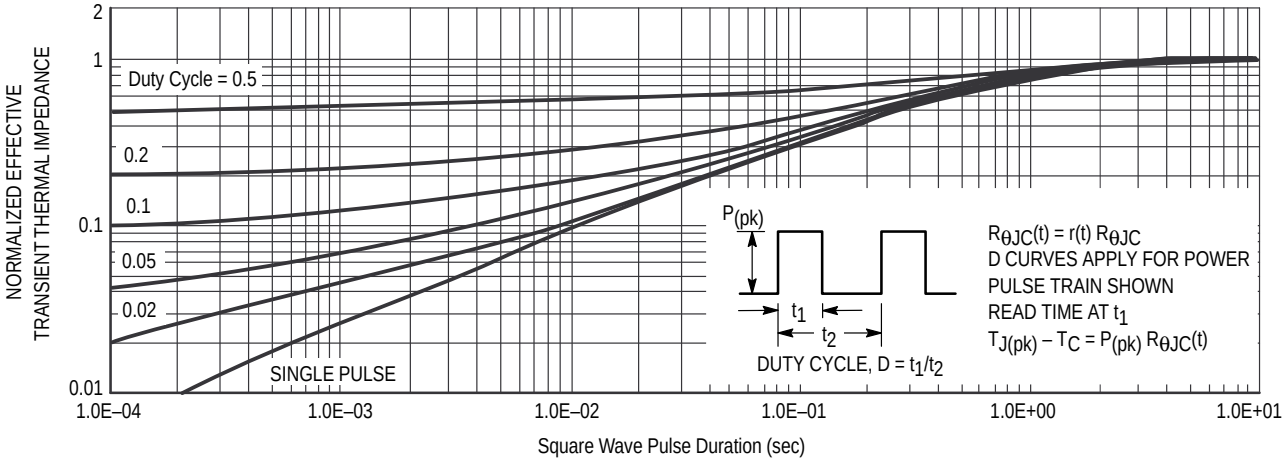
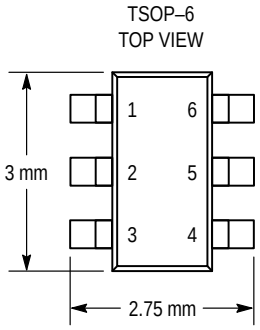


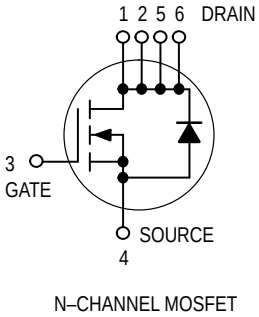
Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient

N–Channel Enhancement–Mode MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.065 @ V_{GS} = 10 V	± 1.75
	0.095 @ V_{GS} = 4.5 V	± 1.5





Power Dissipation
MGSF3454XT1 – 0.95 W

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain–Source Voltage	V_{DSS}	30	Vdc
Gate–Source Voltage — Continuous	V_{GS}	± 20	
Drain Current — Continuous @ T_A = 25°C — Pulsed Drain Current ($t_p \le 10$ μs)	I_D I_{DM}	1.75 20	A
Total Power Dissipation @ T_A = 25°C	P_D	950	mW
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Maximum Lead Temperature for Soldering Purposes, for 10 seconds	T_L	260	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction–to–Ambient (1)	$R_{\theta JA}$	132	°C/W

1. Surface Mounted on FR4 Board, t ≤ 5 sec.

Specifications (T_J = 25°C unless otherwise noted)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μA)		$V_{(BR)DSS}$	30	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 70°C)		I_{DSS}	— —	— —	1.0 25	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	±100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	—	—	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.75 A) (V_{GS} = 4.5 Vdc, I_D = 1.5 A)		$R_{DS(on)}$	— —	0.05 0.07	0.065 0.095	Ohms
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 5.0 V)	C_{iss}	—	345	—	pF
Output Capacitance	(V_{DS} = 5.0 V)	C_{oss}	—	215	—	
Transfer Capacitance	(V_{DG} = 5.0 V)	C_{rss}	—	140	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 1.0 A, V_{GEN} = 10 V, R_L = 10 Ω)	$t_{d(on)}$	—	10	—	ns
Rise Time		t_r	—	15	—	
Turn–Off Delay Time		$t_{d(off)}$	—	20	—	
Fall Time		t_f	—	10	—	
Gate Charge		Q_T	—	—	15	nC
SOURCE–DRAIN DIODE CHARACTERISTICS						
Continuous Current		I_S	—	—	1.0	A
Pulsed Current		I_{SM}	—	—	5.0	A
Forward Voltage(2)		V_{SD}	—	—	1.2	V

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

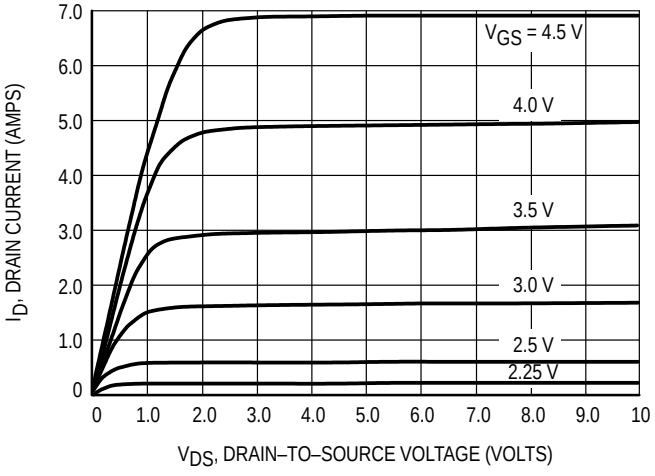


Figure 1. Output Characteristics

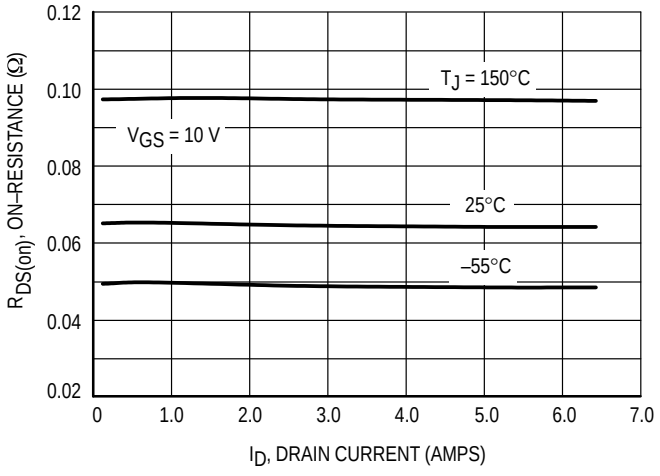


Figure 2. On–Resistance versus Drain Current

TYPICAL ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

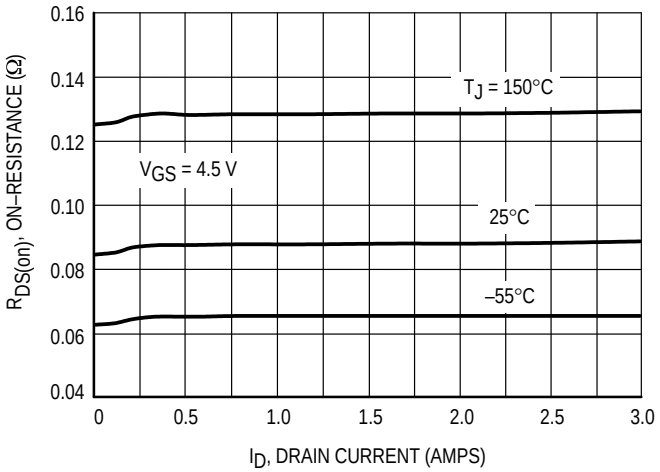


Figure 3. On–Resistance versus Drain Current

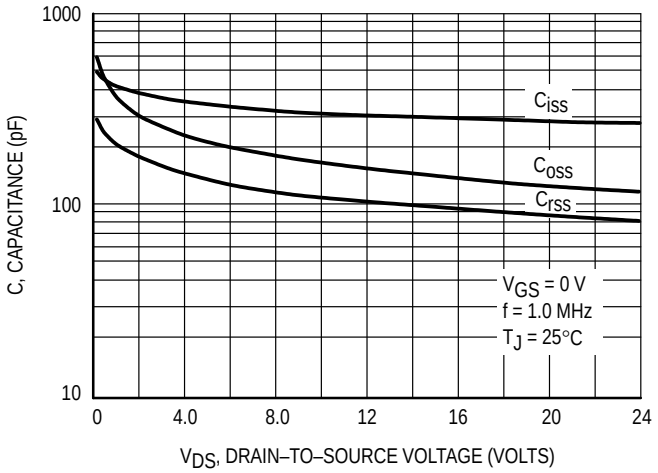


Figure 4. Capacitance

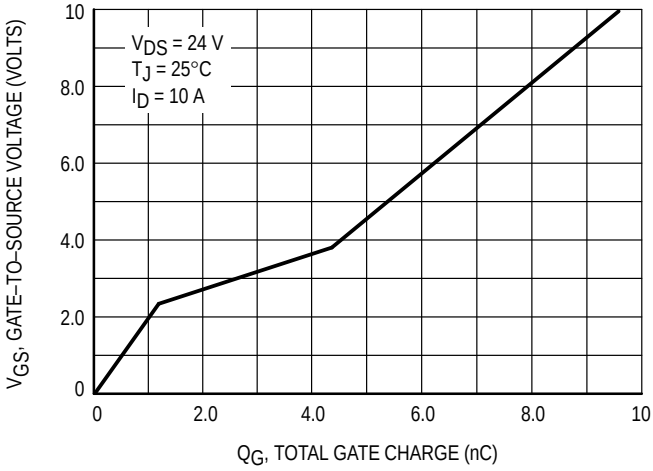


Figure 5. Gate Charge

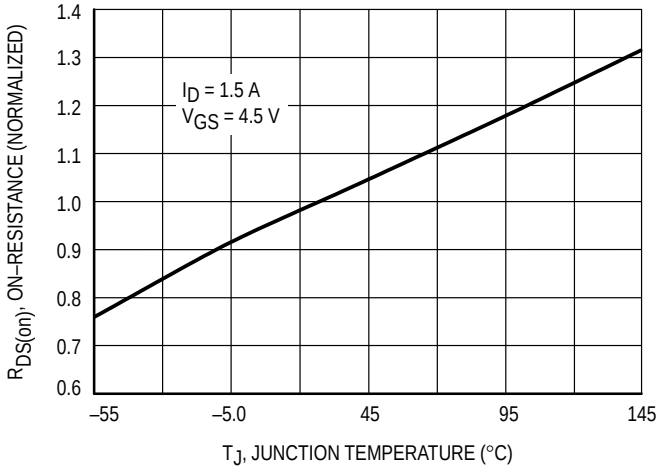


Figure 6. On–Resistance versus Junction Temperature

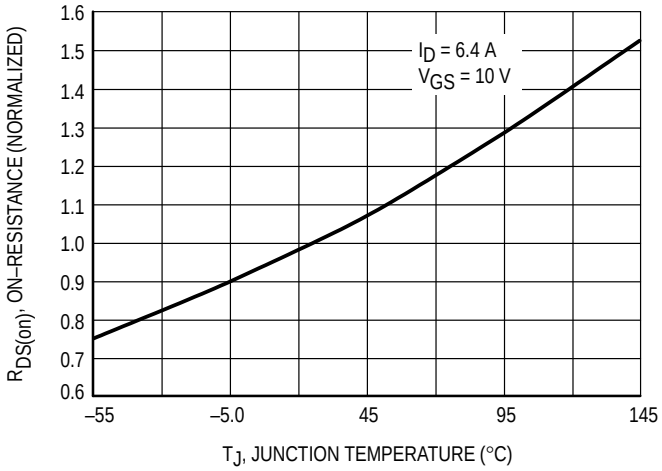


Figure 7. On–Resistance versus Junction Temperature

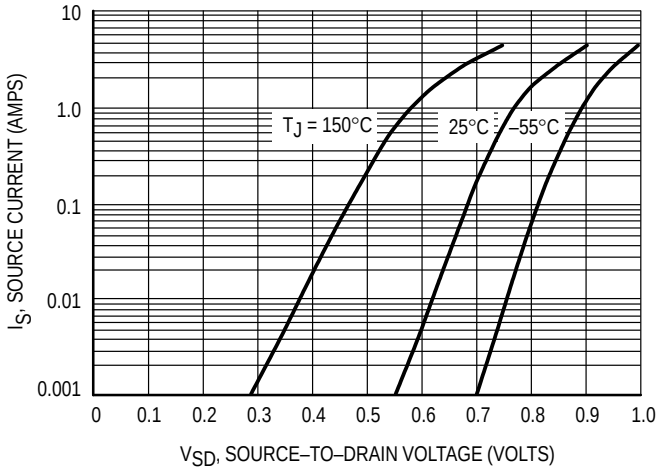


Figure 8. Source–Drain Diode Forward Voltage

TYPICAL ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

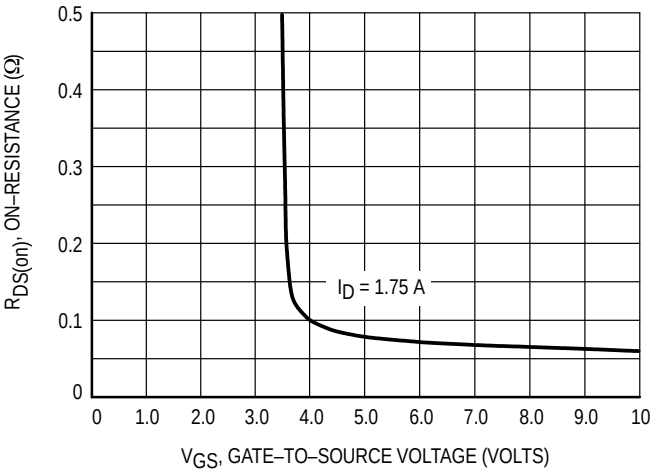


Figure 9. On–Resistance versus Gate–to–Source Voltage

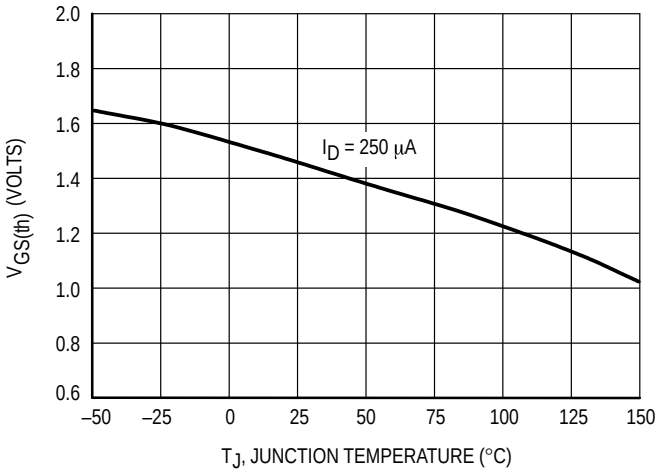


Figure 10. Threshold Voltage

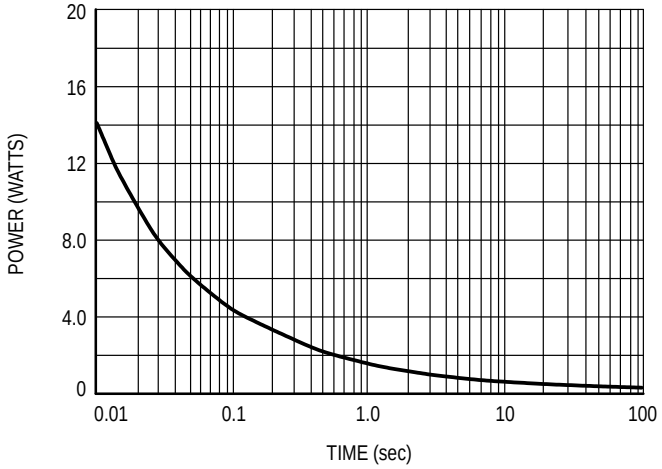


Figure 11. Single Pulse Power

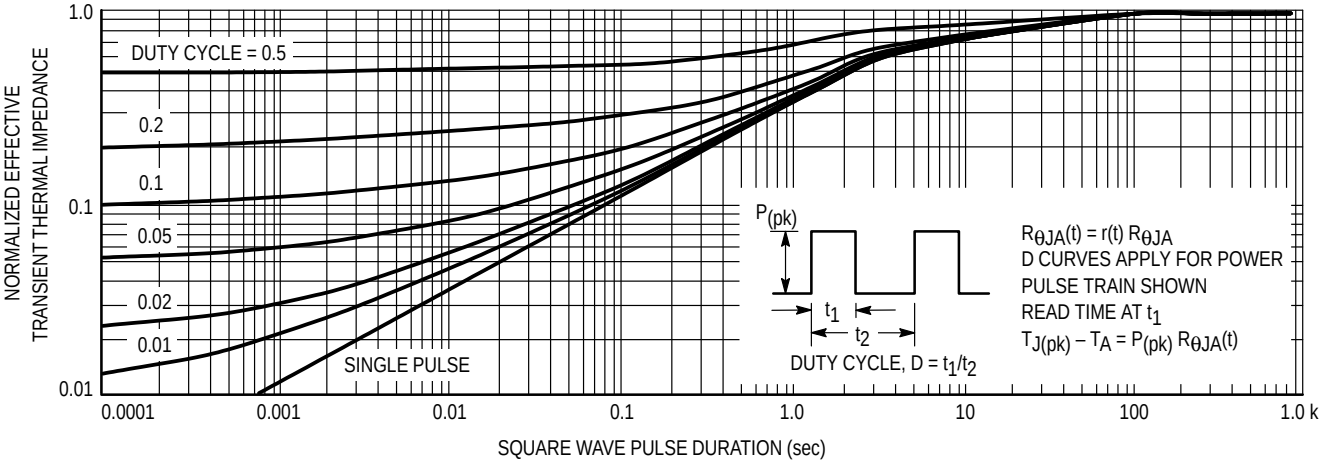
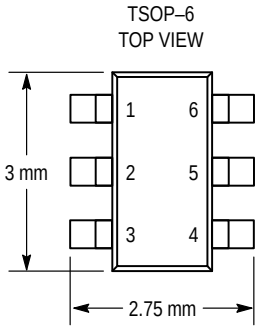


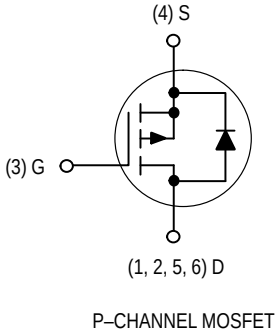
Figure 12. Normalized Thermal Transient Impedance, Junction–to–Ambient

P–Channel Enhancement–Mode MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
– 30	0.10 @ V_{GS} = –10 V	± 3.5
	0.19 @ V_{GS} = – 4.5 V	± 2.5





Power Dissipation
MGSF3455VT1 – 2.0 W

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain–Source Voltage		V_{DS}	– 30	V
Gate–Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C) (1)	T_A = 25°C	I_D	± 3.5	A
	T_A = 70°C		± 2.7	
Pulsed Drain Current		I_{DM}	± 20	
Continuous Source Current (Diode Conduction) (1)		I_S	– 1.7	
Maximum Power Dissipation (1)	T_A = 25°C	P_D	2.0	W
	T_A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	– 55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction–to–Ambient (1)	$R_{\theta JA}$	62.5	°C/W

1. Surface Mounted on FR4 Board, t ≤ 5 sec.

Specifications (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	–1.0			V
Gate–Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = – 30 V, V_{GS} = 0 V			–1.0	μA
		V_{DS} = – 30 V, V_{GS} = 0 V, T_J = 70°C			– 5.0	
On–State Drain Current (1)	$I_{D(on)}$	V_{DS} = – 5.0 V, V_{GS} = –10 V	–15			A
Drain–Source On–State Resistance (1)	$R_{DS(on)}$	V_{GS} = –10 V, I_D = – 3.5 A		0.080	0.100	Ω
		V_{GS} = – 4.5 V, I_D = 2.5 A		0.134	0.190	
Forward Transconductance (1)	g_{FS}	V_{DS} = –15 V, I_D = – 3.5 A		4.0		S
Diode Forward Voltage (1)	V_{SD}	I_S = –1.7 A, V_{GS} = 0 V			–1.2	V
Dynamic (2)						
Total Gate Charge	Q_g	V_{DS} = –10 V, V_{GS} = –10 V, I_D = – 3.5 A		5.1	10	nC
Gate–Source Charge	Q_{gs}			1.5		
Gate–Drain Charge	Q_{gd}			1.0		
Turn–On Delay Time	$t_{d(on)}$	V_{DD} = –10 V, R_L = 10 Ω I_D ≅ –1.0 A, V_{GEN} = –10 V, R_G = 6.0 Ω		10	20	ns
Rise Time	t_r			15	30	
Turn–Off Delay Time	$t_{d(off)}$			20	35	
Fall Time	t_f			10	20	
Source–Drain Reverse Recovery Time	t_{rr}	I_F = –1.7 A, di/dt = 100 A/μs		50	80	

1. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
2. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C unless otherwise noted)

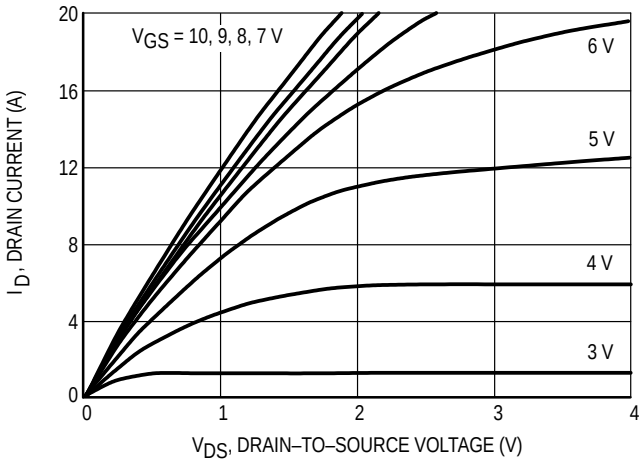


Figure 1. Output Characteristics

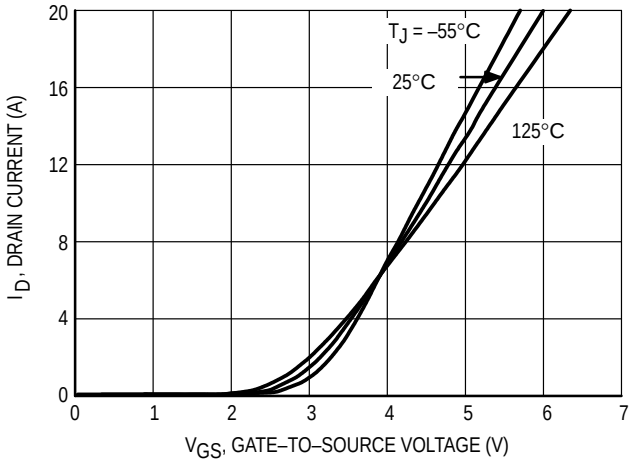


Figure 2. Transfer Characteristics

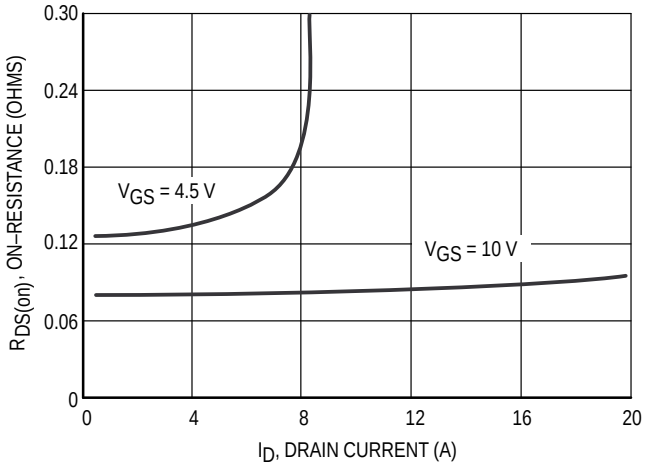


Figure 3. On–Resistance vs. Drain Current

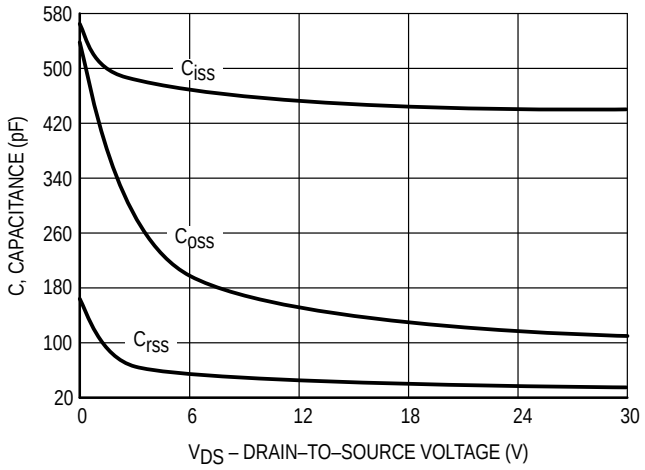


Figure 4. Capacitance

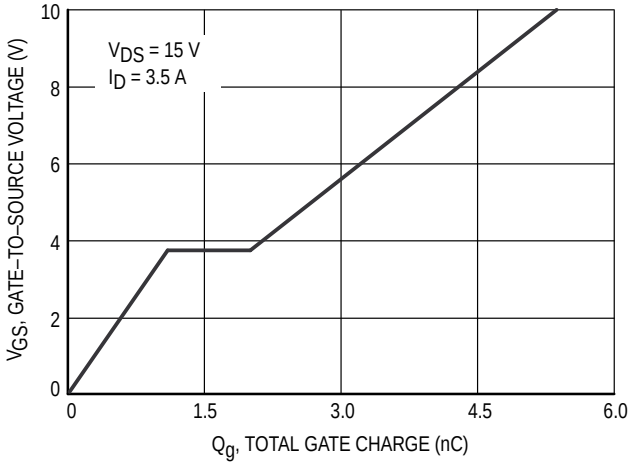


Figure 5. Gate Charge

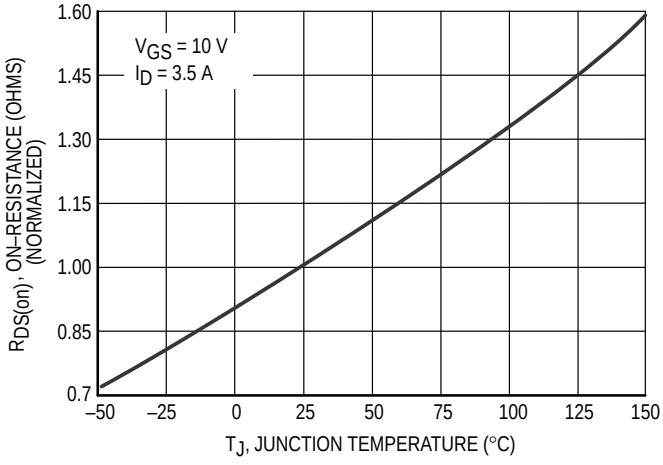


Figure 6. On–Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25°C unless otherwise noted)

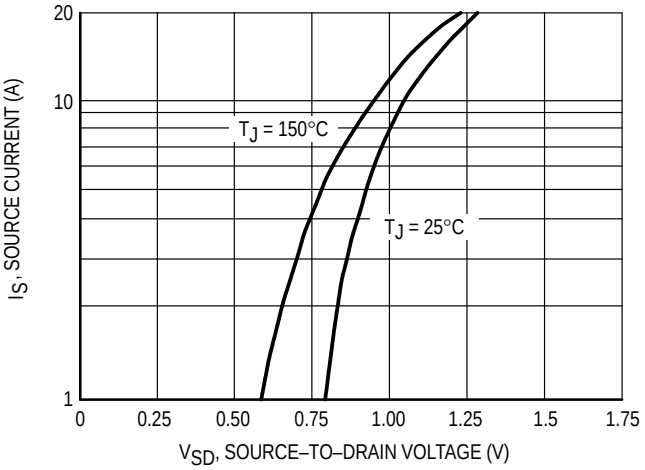


Figure 7. Source–Drain Diode Forward Voltage

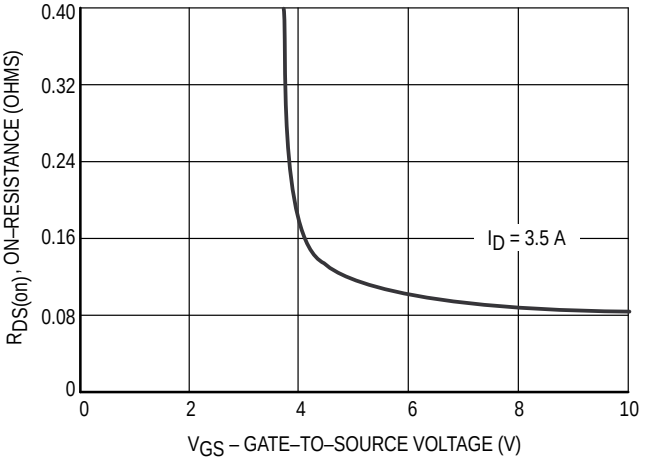


Figure 8. On–Resistance vs. Gate–to–Source Voltage

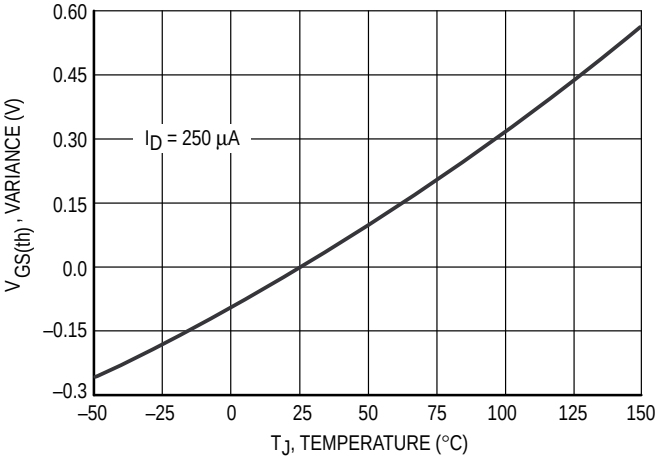


Figure 9. Threshold Voltage

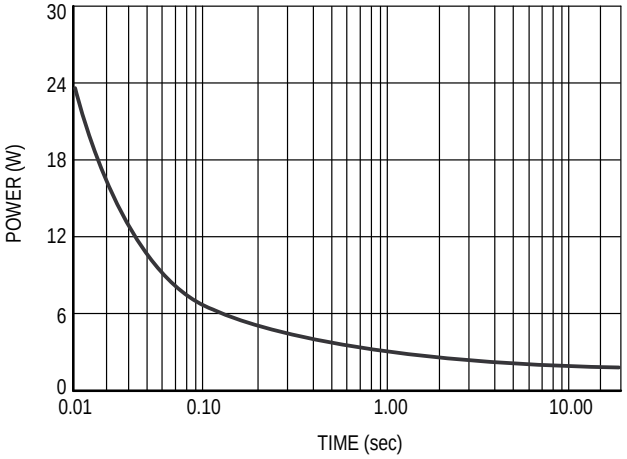


Figure 10. Single Pulse Power

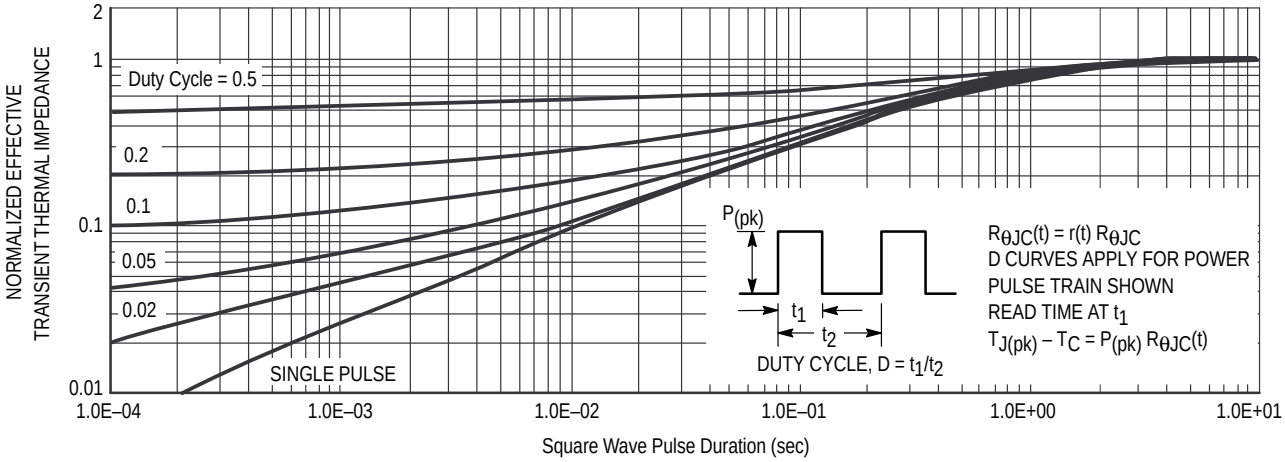
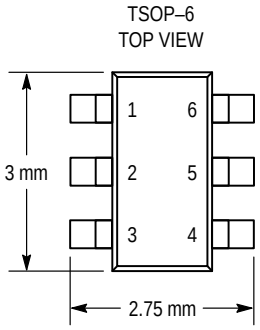


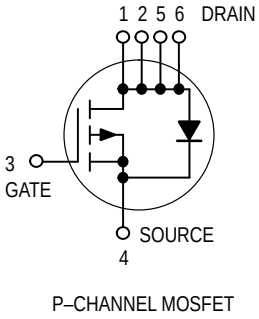
Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient

P–Channel Enhancement–Mode MOSFET

Product Summary

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.10 @ V_{GS} = 10 V	± 1.45
	0.19 @ V_{GS} = 4.5 V	± 1.2





P–CHANNEL MOSFET

Power Dissipation
MGSF3455XT1 – 0.95 W

Absolute Maximum Ratings (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain–Source Voltage	V_{DSS}	30	Vdc
Gate–Source Voltage — Continuous	V_{GS}	± 20	
Drain Current — Continuous @ T_A = 25°C — Pulsed Drain Current ($t_p \le 10$ μs)	I_D I_{DM}	1.45 10	A
Total Power Dissipation @ T_A = 25°C	P_D	950	mW
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Maximum Lead Temperature for Soldering Purposes, for 10 seconds	T_L	260	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction–to–Ambient (1)	$R_{\theta JA}$	132	°C/W

1. Surface Mounted on FR4 Board, t ≤ 5 sec.

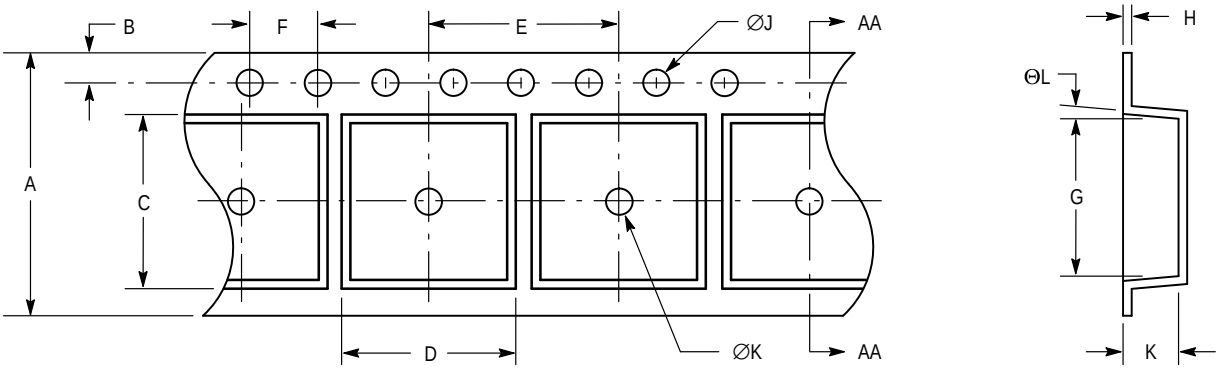
Specifications (T_J = 25°C unless otherwise noted)

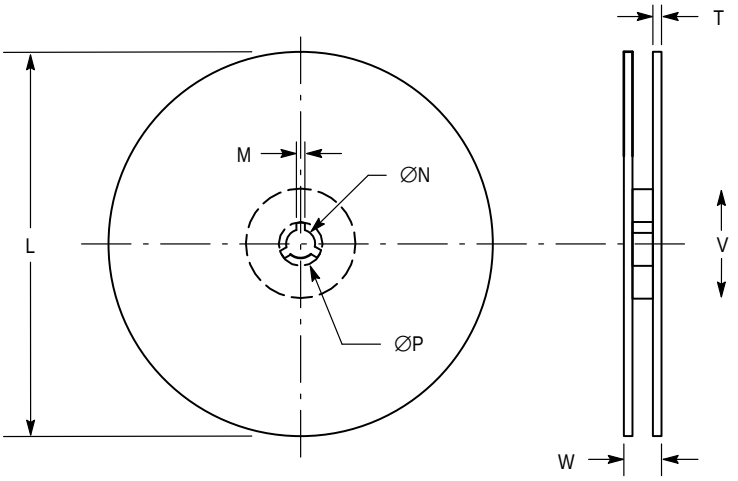
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

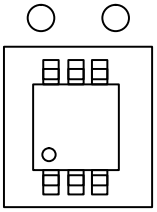
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 10 μA)		$V_{(BR)DSS}$	30	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 70°C)		I_{DSS}	— —	— —	1.0 5.0	μAdc
Gate–Body Leakage Current (V_{GS} = ± 820 Vdc, V_{DS} = 0)		I_{GSS}	—	—	±100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	—	—	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.45 A) (V_{GS} = 4.5 Vdc, I_D = 1.2 A)		$R_{DS(on)}$	— —	0.080 0.134	0.100 0.190	Ohms
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 5.0 V)	C_{iss}	—	90	—	pF
Output Capacitance	(V_{DS} = 5.0 V)	C_{oss}	—	50	—	
Transfer Capacitance	(V_{DG} = 5.0 V)	C_{rss}	—	10	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 1.0 A, V_{GEN} = 10 V, R_L = 10 Ω)	$t_{d(on)}$	—	10	20	ns
Rise Time		t_r	—	15	30	
Turn–Off Delay Time		$t_{d(off)}$	—	20	35	
Fall Time		t_f	—	10	20	
Gate Charge		Q_T	—	3000	—	pC
SOURCE–DRAIN DIODE CHARACTERISTICS						
Continuous Current		I_S	—	—	1.0	A
Pulsed Current		I_{SM}	—	—	5.0	A
Forward Voltage(2)		V_{SD}	—	0.85	—	V

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TSOP–6 Tape and Reel Options







PACKAGE ORIENTATION

QUANTITY PER REEL		
DEVICE	REEL SIZE	QUANTITY
MGSF34xxX–T1	7–inches	3,000
MGSF34xxX–T3	13–inches	10,000

	T1				T3			
	Millimeters		Inches		Millimeters		Inches	
Dim	Min	Max	Min	Max	Min	Max	Min	Max
A	7.70	8.30	0.303	0.327	7.70	8.30	0.303	0.327
B	1.65	1.85	0.065	0.073	1.65	1.85	0.065	0.073
C	3.10	3.30	0.122	0.130	3.10	3.30	0.122	0.130
D	3.05	3.25	0.120	0.128	3.05	3.25	0.120	0.128
E	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
F	3.90	4.10	0.154	0.161	3.90	4.10	0.154	0.161
G	3.10	3.30	0.122	0.130	3.10	3.30	0.122	0.130
H	0.17	0.23	0.007	0.009	0.17	0.23	0.007	0.009
ØJ	1.50	1.60	0.059	0.063	1.50	1.60	0.059	0.063
K	1.30	1.50	0.051	0.059	1.30	1.50	0.051	0.059
ØK	1.00	1.10	0.039	0.043	1.00	1.10	0.039	0.043
L	170	180	6.929	7.087	328	332	12.91	13.07
ΘL	—	3°	—	3°	—	3°	—	3°
M	1.50	2.50	0.059	0.098	1.50	2.50	0.059	0.098
ØN	12.8	13.2	0.504	0.520	12.8	13.2	0.504	0.520
ØP	21.5	22.5	0.846	0.886	21.5	22.5	0.847	0.886
T	1.00	2.00	0.039	0.078	1.00	2.00	0.039	0.078
V	53.0	54.0	2.087	2.126	53.0	54.0	2.087	2.126
W	7.90	8.90	0.311	0.350	24.4	16.4	0.961	1.039

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