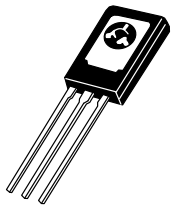
BD169

Plastic Medium Power Silicon NPN Transistor

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD169 is complementary with BD170

1.5 AMPERE
POWER TRANSISTOR
NPN SILICON
80 VOLTS
20 WATTS



CASE 77–09
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	
Collector–Base Voltage	V_{CBO}	80	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector Current	I_C	1.5	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 8	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 160	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	80	—	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	h_{FE}*	40 15	— —	
Collector–Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*	—	0.5	Vdc
Base–Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*	—	0.95	Vdc
Current Gain–Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2 Vdc, f = 1.0 MHz)	f_T	6.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

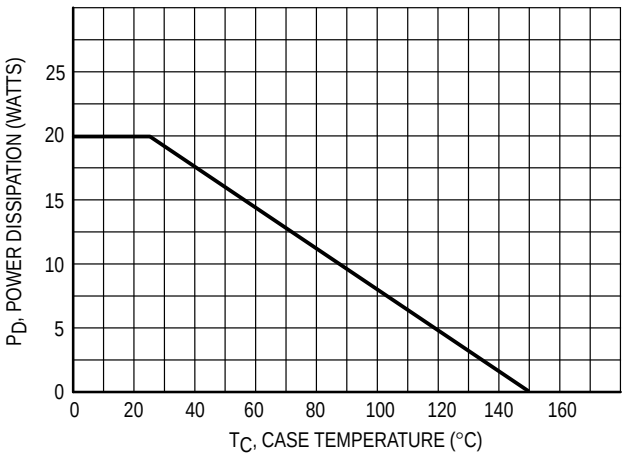


Figure 1. P_D – T_C Derating Curve

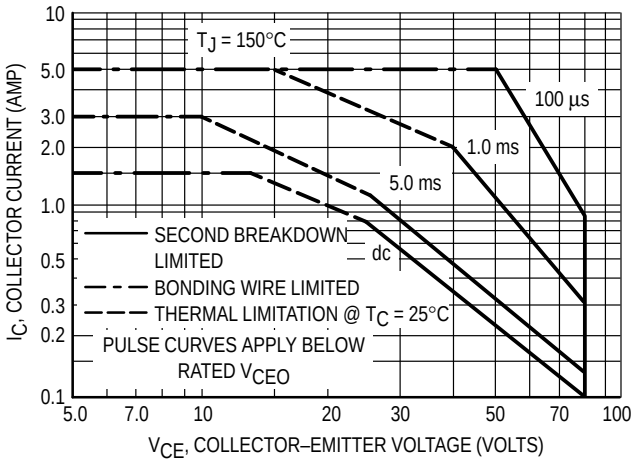


Figure 2. Safe Operating Area (see Note 1)

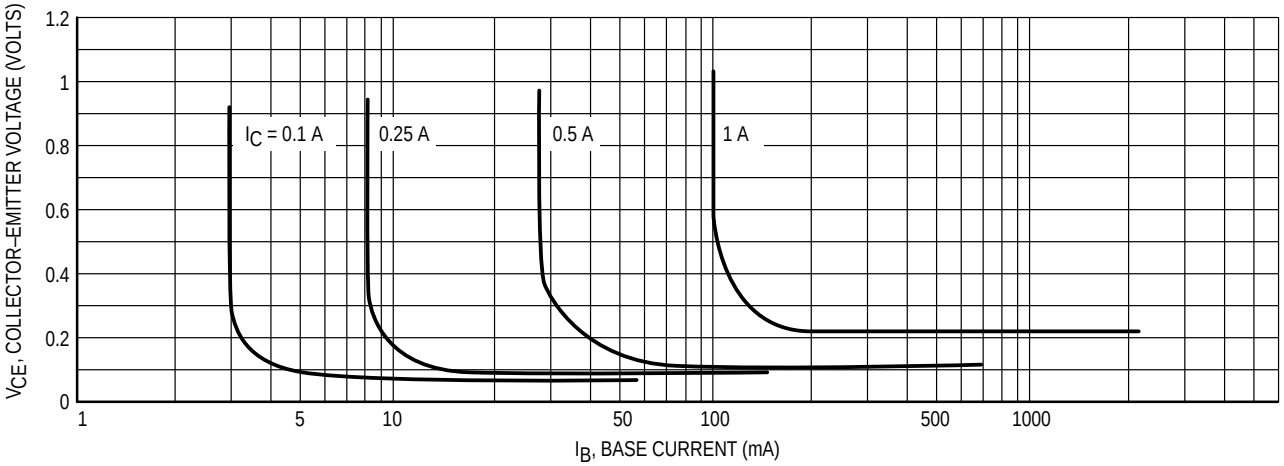


Figure 3. Collector Saturation Region

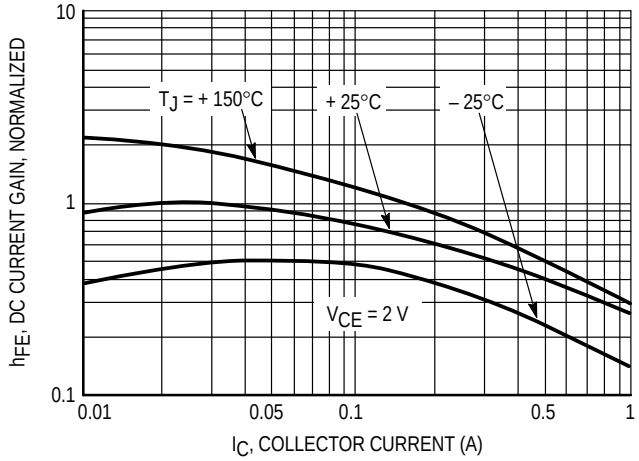


Figure 4. Current Gain

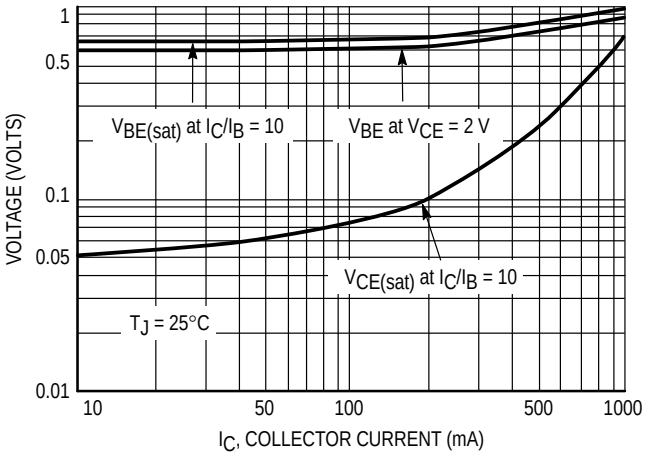


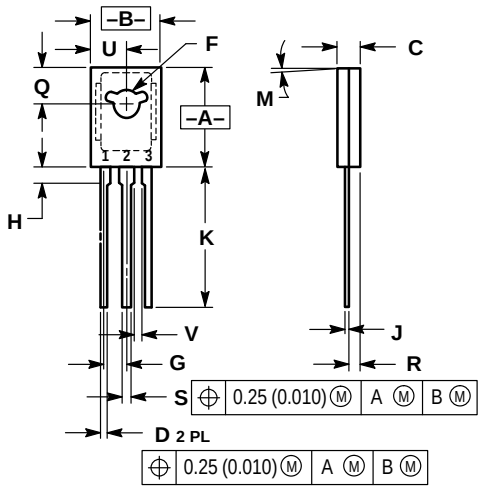
Figure 5. "On" Voltage

Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	—	1.02	—

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

CASE 77–09
TO–225AA TYPE
ISSUE W

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