Power MOSFET

30 V, 7.8 A, µCool™ Single N–Channel, 2x2 mm WDFN Package

Features

- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88
- Lowest R_{DS(on)} in 2x2 mm Package
- 1.8 V R_{DS(on)} Rating for Operation at Low Voltage Logic Level Gate Drive
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- This is a Pb-Free Device

Applications

- DC-DC Conversion
- Boost Circuits for LED Backlights
- Optimized for Battery and Load Management Applications in Portable Equipment such as, Cell Phones, PDA's, Media Players, etc.
- Low Side Load Switch

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage			V_{GS}	±8.0	V
Continuous Drain	Steady	$T_A = 25^{\circ}C$	I _D	6.0	Α
Current (Note 1)	State	T _A = 85°C		4.4	
	t ≤ 5 s	T _A = 25°C		7.8	
Power Dissipation (Note 1)	Steady State T _A = 25°C		P _D	1.92	W
	t ≤ 5 s			3.3	
Continuous Drain		$T_A = 25^{\circ}C$	I _D	3.6	Α
Current (Note 2)	Steady	$T_A = 85^{\circ}C$		2.6	
Power Dissipation (Note 2)	State T _A = 25°		P _D	0.70	W
Pulsed Drain Current	t _p = 10 μs		I_{DM}	28	Α
Operating Junction and Storage Temperature		T _J , T _{STG}	–55 to 150	°C	
Source Current (Body Diode) (Note 2)			I _S	3.0	Α
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

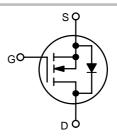
- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
- Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm2, 2 oz Cu.



ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX (Note 1)
	35 m Ω @ 4.5 V	
30 V	45 mΩ @ 2.5 V	7.8 A
	55 mΩ @ 1.8 V	



N-CHANNEL MOSFET





1 JBM• 6 5 4

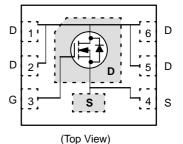
JB = Specific Device Code

= Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping [†]
NTLJS4159NT1G	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 3)	$R_{ heta JA}$	65	
Junction-to-Ambient - t ≤ 5 s (Note 3)	$R_{ heta JA}$	38	°C/W
Junction-to-Ambient - Steady State Min Pad (Note 4)	$R_{\theta JA}$	180	

- Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
 Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

MOSFET ELECTRICAL CHARACTERISTICS (T₁ = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = 250 μA, Ref to 25°C			20		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	I _{DSS} T _J = 25°C				1.0	μΑ
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	T _J = 125°C			10	1
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 0 \text{ V}$	±8.0 V			±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 25$	50 μΑ	0.4	0.7	1.0	V
Negative Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J				3.18		mV/°C
Drain-to-Source On-Resistance	R _{DS(on)}	$V_{GS} = 4.5, I_D = 2$	2.0 A		20.3	35	mΩ
		$V_{GS} = 2.5, I_D = 2$	2.0 A		25.8	45	1 !
		$V_{GS} = 1.8, I_D = 1$.8 A		35.2	55	1
Forward Transconductance	9 _{FS}	V _{DS} = 16 V, I _D = 2.0 A			5.3		S
CHARGES, CAPACITANCES AND GA	TE RESISTANO	CE					
Input Capacitance	C _{ISS}	$V_{GS} = 0 \text{ V, } f = 1.0 \text{ MHz,}$ $V_{DS} = 15 \text{ V}$			1045		pF
Output Capacitance	C _{OSS}				115.5		1
Reverse Transfer Capacitance	C _{RSS}				45.3		
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V},$ $I_D = 2.0 \text{ A}$			12.1	13	nC
Threshold Gate Charge	Q _{G(TH)}				1.2		1
Gate-to-Source Charge	Q_GS				1.9		1
Gate-to-Drain Charge	Q_{GD}				2.7		1
Gate Resistance	R_{G}				3.65		Ω
SWITCHING CHARACTERISTICS (No	ote 6)						
Turn-On Delay Time	t _{d(ON)}				6.8		ns
Rise Time	t _r	$V_{GS} = 4.5 \text{ V}, V_{DD} =$: 15 V,		12.4		1
Turn-Off Delay Time	t _{d(OFF)}	$I_D = 2.0 \text{ A}, R_G = 3.0 \Omega$			26		1
Fall Time	t _f				5.1		1
DRAIN-SOURCE DIODE CHARACTE	RISTICS						
Forward Recovery Voltage	V_{SD}		T _J = 25°C		0.71	1.2	.,
,			T _J = 125°C		0.58		_
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V}, d_{ISD}/d_t = 100 \text{ A}/\mu\text{s},$ $I_S = 1.0 \text{ A}$			15	35	
Charge Time	ta				9.0		ns
Discharge Time	t _b				6.0		1
Reverse Recovery Time	Q_{RR}				7.0		nC

- 5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

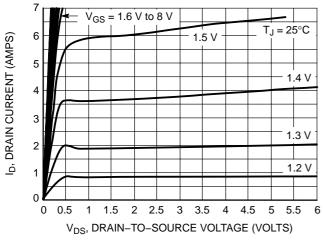
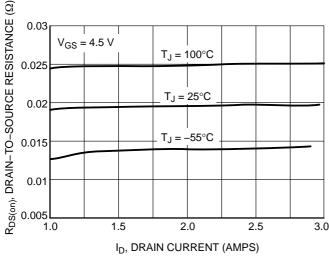


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



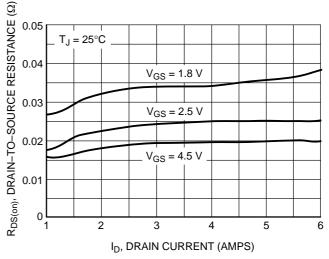
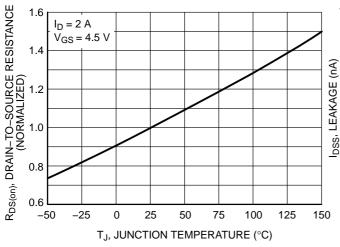


Figure 3. On-Resistance versus Drain Current

Figure 4. On-Resistance versus Drain Current and Gate Voltage



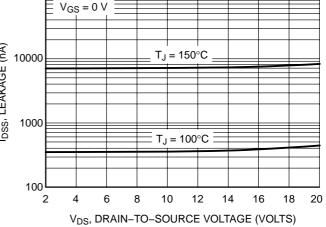
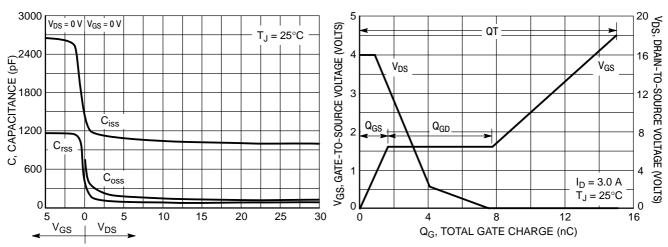


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current versus Voltage

100000

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

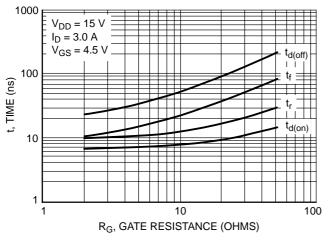


Figure 9. Resistive Switching Time Variation versus Gate Resistance

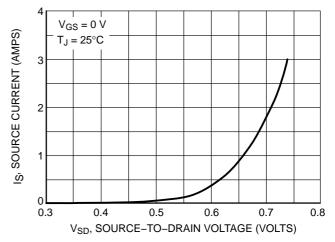


Figure 10. Diode Forward Voltage versus Current

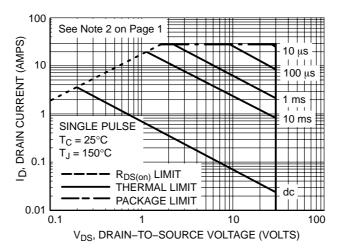


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

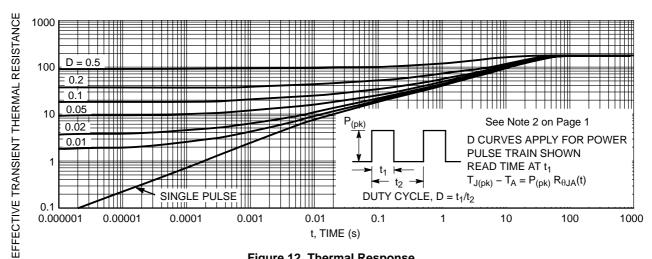
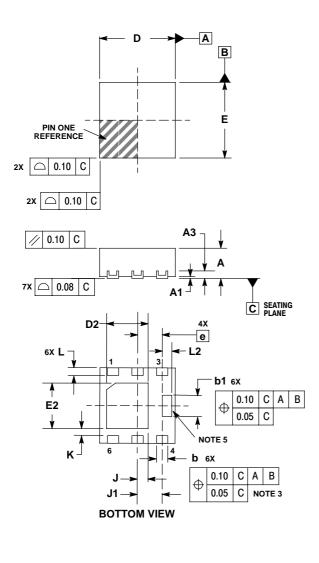


Figure 12. Thermal Response

PACKAGE DIMENSIONS

WDFN6, 2x2 CASE 506AP-01 **ISSUE A**

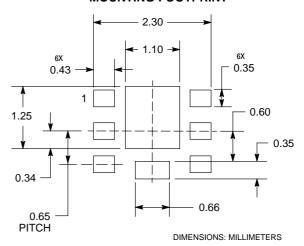


NOTES

- DIMENSIONING AND TOLERANCING PER ASME Y14 5M 1994
- CONTROLLING DIMENSION: MILLIMETERS.
- 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL
- 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 5. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL
- LEAD IS CONNECTED TO TERMINAL LEAD # 4. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

	MILLIMETERS		
DIM	MIN	MAX	
Α	0.70	0.80	
A1	0.00	0.05	
A3	0.20	REF	
b	0.25	0.35	
b1	0.51	0.61	
D	2.00 BSC		
D2	1.00	1.20	
E	2.00 BSC		
E2	1.10	1.30	
е	0.65 BSC		
K	0.15 REF		
L	0.20	0.30	
L2	0.20	0.30	
J	0.27 REF		
J1	0.65 REF		

SOLDERMASK DEFINED **MOUNTING FOOTPRINT**



 μ Cool is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and un are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice on semiconductor and are registered readerlands of semiconductor Components industries, Ltc (SCILLC). Solitude services the inject to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082-1312 USA Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Japan: ON Semiconductor, Japan Customer Focus Center 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051 Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative