

MNLMX2315-X REV 1A1

 Original Creation Date: 09/05/97
 Last Update Date: 03/16/99
 Last Major Revision Date: 02/08/99

PLL FREQUENCY SYNTHESIZER
General Description

The LMX2315 is a high performance frequency synthesizer with integrated prescalers designed for RF operation up to 1.2 GHz. They are fabricated using National's ABiC IV BiCMOS process.

A 64/65 or a 128/129 divide ratio can be selected for the LMX2315 RF synthesizer at input frequencies of up to 1.2 GHz. Using a proprietary digital phase locked loop technique, the LMX2315's linear phase detector characteristics can generate very stable, low noise signals for controlling a local oscillator.

Serial data is transferred into the LMX2315 via a three line MICROWIRE(TM) interface (Data Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2315 features very low current consumption, typically 6 mA.

The LMX2315, is available in a SOIC 20-pin surface mount ceramic package.

Industry Part Number

LMX2315

NS Part Numbers

LMX2315WG-QML

Prime Die

LMX2315

Controlling Document

SEE FEATURES SECTION:

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+105
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+105
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+105
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+105
11	Switching tests at	-55

Features

- RF operation up to 1.2 GHz.
- 2.7V to 5.5V operation.
- Low current consumption.
- Dual modulus prescaler: 64/65 or 128/129
- Internal balanced, low leakage charge pump.
- Power down feature for sleep mode:
I_{cc} = 30 uA (typ) at V_{cc} = 3V
- Small-outline ceramic surface mount SOIC, 0.300" wide.
- CONTROLLING DOCUMENT:
LMX2315WG-QML 5962-9855001QXA

Applications

- Satellite Communications Payloads
- Navigation Systems
- Military Wireless Communications

(Absolute Maximum Ratings)

(Note 1)

Power Supply Voltage	
Vcc	-0.3V to +6.5V
Vp	-0.3V to +6.5V
Voltage on Any Pin	
with Gnd = 0V (Vi)	-0.3V to +6.5V
Storage Temperature Range (Ts)	-65 C to +150 C
Power Dissipation	
(Note 2)	
Pd	1 Watt
Junction Temperature	
(Note 2)	
Tj	+150 C
Lead Temperature (Tl)	
(Solder, 4 sec.)	+260 C
Thermal Resistance	
(Note 2)	
ThetaJA	
(Still Air @ 0.5W)	120 C/W
(500LF/Min Air Flow @ 0.5W)	86 C/W
ThetaJC	19 C/W
Package Weight	
(Typical)	600mg
ESD Tolerance	
(Note 3)	Less Than 500V

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{dmax} = (T_{jmax} - TA) / \Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
- Note 3: This device is a high performance RF integrated circuit with an ESD rating <500V and is ESD sensitive. Handling and assembly of this device should be done at ESD workstations.

Recommended Operating Conditions

Power Supply Voltage	
Vcc	2.7V to 5.5V
Vp	Vcc to +5.5V
Operating Temperature (TA)	-55 C to +105 C

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_{cc} = 5.5V$, $V_p = 5.5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
I _{cc}	Power Supply Current	$V_{cc} = 5.5V$			8.5		mA	1, 3
					9.5		mA	2
I _{cc-pwdn}	Power Down Current	$V_{cc} = 2.7V$			180		uA	1, 2, 3
		$V_{cc} = 5.5V$			350		uA	1, 2, 3
V _{osc}	Oscillator Sensitivity	OSCin			0.5		V _{pp}	1, 2, 3
V _{IH}	High Level Input Voltage	$V_{cc} = V_p = 2.7V$	1, 4		0.7V _{cc}		V	1, 2, 3
V _{IL}	Low Level Input Voltage	$V_{cc} = V_p = 2.7V$	1, 4			0.3V _{cc}	V	1, 2, 3
I _{IH}	High Level Input Current (Clock Data)	$V_{IH} = V_{cc} = 5.5V$			-1.0	1.0	uA	1, 2, 3
I _{IL}	Low Level Input Current (Clock Data)	$V_{IL} = 0, V_{cc} = 5.5V$			-1.0	1.0	uA	1, 2, 3
I _{IH}	Oscillator Input Current	$V_{IH} = V_{cc} = 5.5V$				100	uA	1, 2, 3
I _{IL}	Oscillator Input Current	$V_{IL} = 0, V_{cc} = 5.5V$			-100		uA	1, 2, 3
I _{IH}	High Level Input Current (LE, PC, PWDN)	$V_{IH} = V_{cc} = 5.5V$			-1.0	1.0	uA	1, 2, 3
I _{IL}	Low Level Input Current (LE, PC, PWDN)	$V_{IL} = 0, V_{cc} = 5.5V$			-100	1.0	uA	1, 2, 3
ID _{O-Tri}	Charge Pump TRI-STATE Current	$0.5V \leq V_{do} \leq 3.1V, V_{cc} = V_p = 3.6V$			-2.5	2.5	nA	1, 3
					-25	25	nA	2
ID _{O-Source}	Charge Pump Output Current	$V_{cc} = V_p = 2.7V, V_{do} = 1.35V$			-3.2		mA	1, 2, 3
		$V_{cc} = V_p = 5.0V, V_{do} = 2.5V$			-8.0		mA	1, 2, 3
ID _{O-Sink}	Charge Pump Output Current	$V_{cc} = V_p = 2.7V, V_{do} = 1.35V$				3.2	mA	1, 2, 3
		$V_{cc} = V_p = 5.0V, V_{do} = 2.5V$				8.0	mA	1, 2, 3

Electrical Characteristics

DC PARAMETERS: (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_{cc} = 5.5V$, $V_p = 5.5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IDO vs VDO	Charge Pump Output Current Magnitude Variation vs Voltage	$V_{cc} = V_p = 5.0V$, $0.5V \leq V_{do} \leq 4.5V$				15	%	1, 2, 3
IDOsink vs IDOsource	Charge Pump Output Current Sink vs Source Mismatch	$V_{cc} = V_p = 5.0V$, $V_{DO} = 2.5V$				10	%	1, 2, 3
VOH	High Level Output Voltage	$I_{OH} = -1.0mA$	2		$V_{cc} - 0.8$		V	1, 2, 3
VOL	Low Level Output Voltage	$I_{OL} = 1.0mA$	2			0.4	V	1, 2, 3
VOH (OSCout)	High Level Output Voltage	$I_{OH} = -200\mu A$, $V_{cc} = V_p = 3.0V$			$V_{cc} - 0.8$		V	1, 2, 3
VOL (OSCout)	Low Level Output Voltage	$I_{OL} = 200\mu A$, $V_{cc} = V_p = 3.0V$				0.4	V	1, 2, 3
IOL	Open Drain Output Current (PHP)	$V_{OL} = 0.4V$	4		1.0		mA	1, 2, 3
IOH	Open	$V_{OH} = 5.5V$				100	μA	1, 2, 3

Electrical Characteristics

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: $V_{cc} = 2.7V$, $V_p = 2.7V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tCS	Data to Clock Setup Time	See Data Input Timing for Figure 3			50		nS	9, 10, 11
tCH	Data to Clock Hold Time	See Data Input Timing for Figure 3			10		nS	9, 10, 11
tCWH	Clock Pulse Width High	See Data Input Timing for Figure 3			50		nS	9, 10, 11
tCWL	Clock Pulse Width Low	See Data Input Timing for Figure 3			50		nS	9, 10, 11
tES	Clock to Enable Setup Time	See Data Input Timing for Figure 3			50		nS	9, 10, 11
tEW	Enable Pulse Width	See Data Input Timing for Figure 3			50		nS	9, 10, 11
fIN	Maximum Operating Frequency		4			1.2	GHz	9, 10, 11
Pfin	Input Sensitivity	$V_{cc} = 2.7V$	4		-15	+5	dBm	9, 10, 11
		$V_{cc} = 5.5V$	4		-9	+6	dBm	9, 10
			4		-7	+6	dBm	11
	Locktime	Freq. Jump 51MHz ($f = 864$ to 915 MHz), lock time within ± 5 KHz, $V_{cc} = V_p = 5.0V$	3			500	μ S	9
	Phase Noise	$f_{op} = 900$ MHz at 1KHz offset, $V_{cc} = V_p = 5.0V$	3			-70	dBc	9
		$f_{op} = 900$ MHz at 10KHz offset, $V_{cc} = V_p = 5.0V$	3			-70	dBc	9
	Spurs	$f_{op} = 900$ MHz, $f_{ref} = 200$ KHz, $V_{cc} = V_p = 5.0V$	3			-60	dBc	9

Note 1: Except fIN and OSCin.
 Note 2: Except OSCout.
 Note 3: QMLV/MLS only
 Note 4: Used as Setup Condition

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06346HRA3	CERPACK, 20 LEAD GULL WING
AN00035A	(LMX2305/15/25) TIMING DIAGRAM
P000390A	CERAMIC SOIC (WG), 20 LEAD (PINOUT)
WG20ARB	CERPACK, 20 LEAD GULL WING (P/P DWG)

See attached graphics following this page.

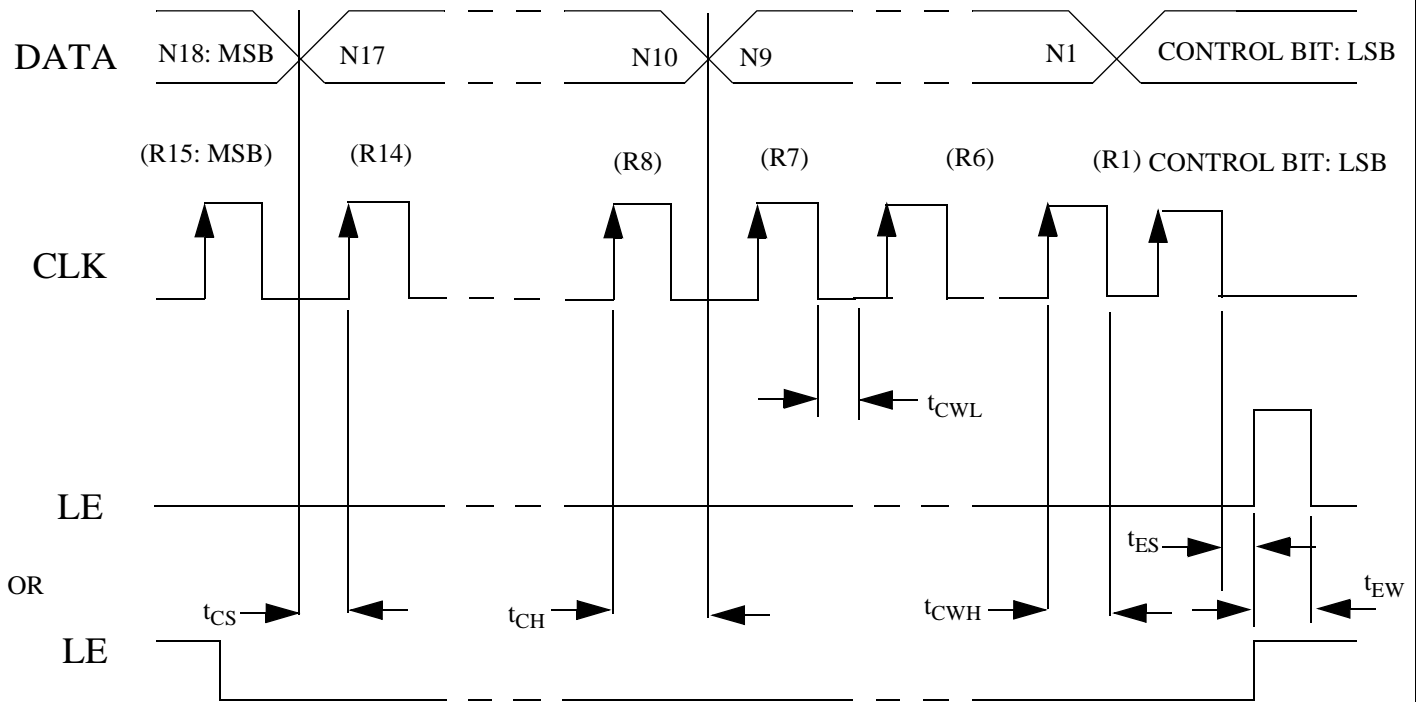
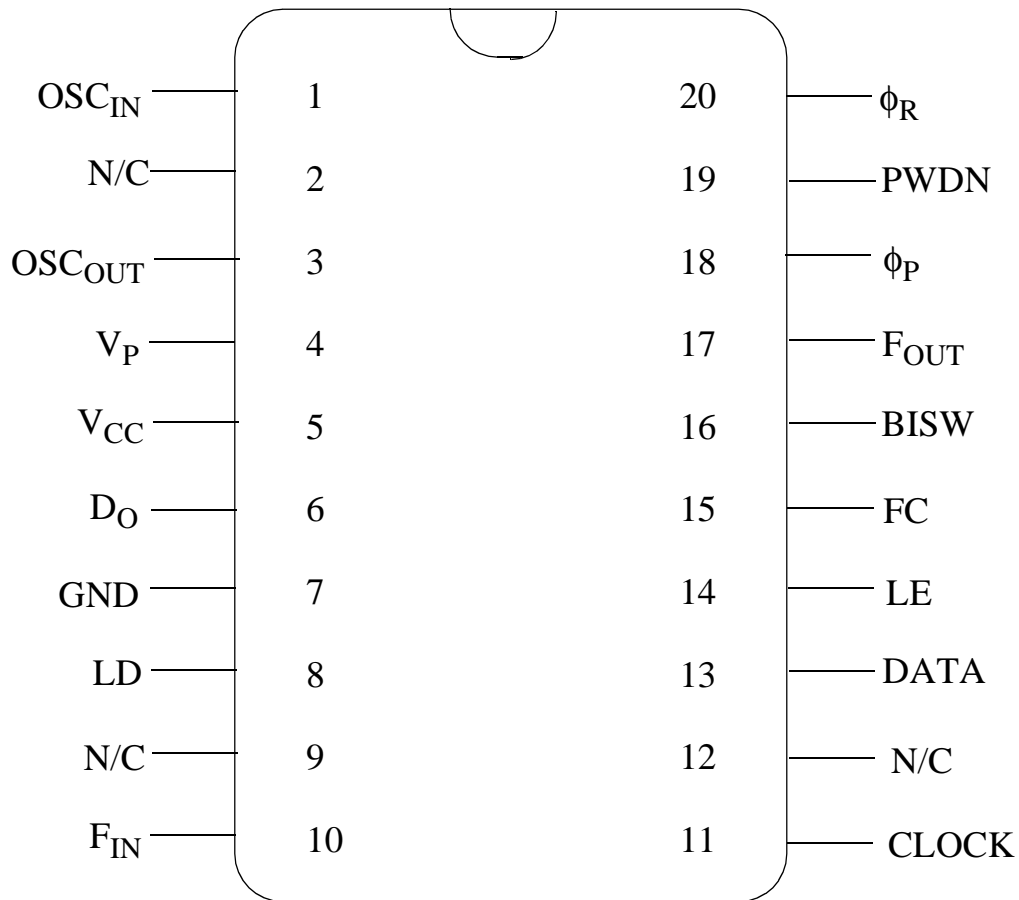


figure 3

AN00035A

Notes:

1. Parenthesis data indicates programmable reference divider data.
2. Data shifted into register in clock rising edges.
3. Data is shifted in MSB first.



LMX2315WG
20 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000390A

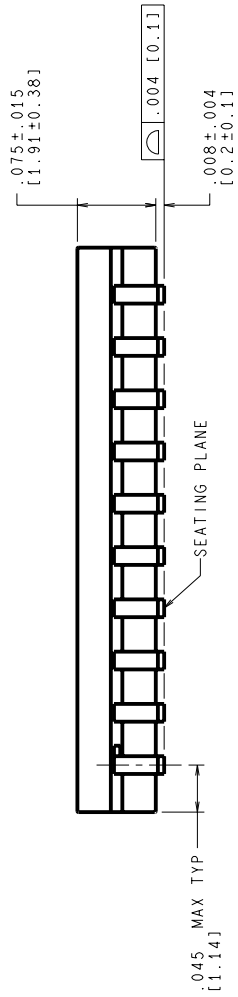
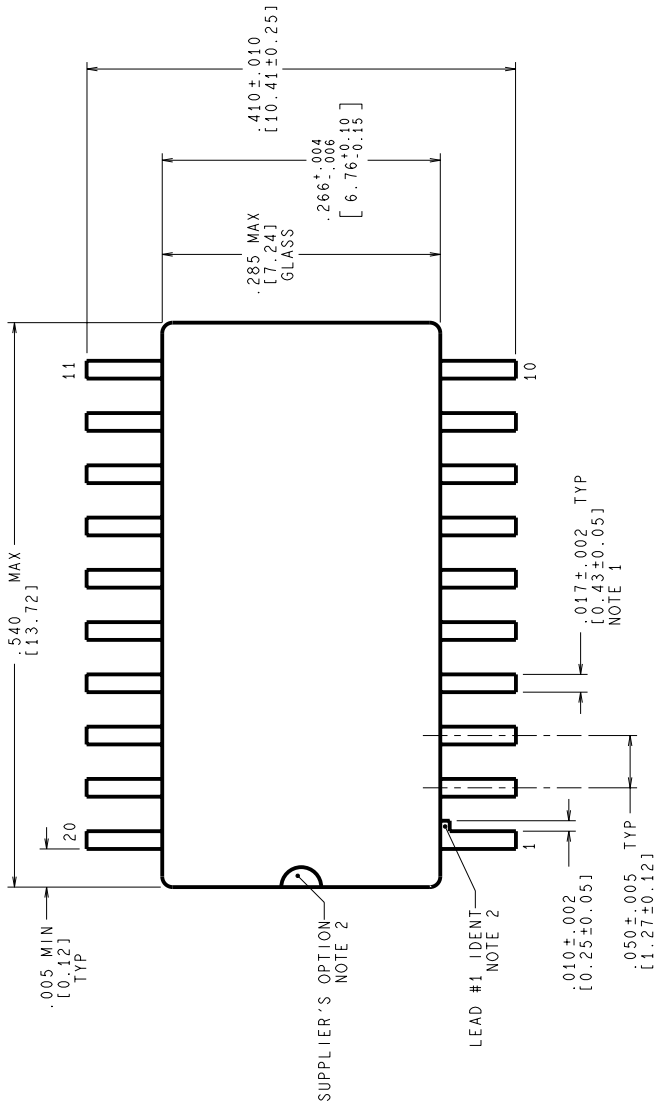


National Semiconductor™

MIL/AEROSPACE OPERATIONS
 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050

REVISIONS

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11842	10/13/1997	TL/KH
B	DIM .410 WAS .391; UPDATE NOTE 3.	12013	06/15/1998	MS/



MIL-PRF-38535
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN () ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
- LEAD IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
- NO JEDEC REGISTRATION AS OF JUNE 1998.

APPROVALS	DATE
DESIGN	10/13/1997
DRWG. ENG'G	
PRODUCTION	
SCALE	N/A
SIZE	C
DRAWING NUMBER	(SC)MKT-WG20A
REV	B

DO NOT SCALE DRAWING SHEET 1 of 1

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**CERPACK,
20 LEAD,
GULL WING**

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002486	03/16/99	Rose Malone	Initial Release of MDS:
1A1	M0003258	03/16/99	Rose Malone	Update MDS: MNLX2315-X, Rev. 0A0 to MNLX2315-X, Rev. 1A1. Moved Reference to Controlling Document to Features Section. Added Power Dissipation and Junction Temperature reference to Absolute Section. Changed Electrical Conditions for VIH, VIL, IDO-Tri, IDO vs VDO, IDOsink vs IDOsource, VOH(OSCout), VOL(OSCout) and IOL. Added NOTE 4 to VIH, VIL, IOL, fIN and Pfin. Updated B/I graphic.