National Semiconductor

MILITARY DATA SHEET

MNLMF60CM-50-X REV 0AL

Original Creation Date: 08/21/95
Last Update Date: 08/21/95
Last Major Revision Date: 08/21/95

6th ORDER SWITCHED CAPACITOR BUTTERWORTH LOWPASS FILTER

Industry Part Number

LMF60CMJ-50

NS Part Numbers

LMF60CMJ50/883

Prime Die

LMF60-50

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = 5V, V- = -5V, fCLK = 500KHz

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
fclk	Clock Frequency Range		1			1.5	MHz	1, 2, 3
Is+	Supply Current					7.0	mA	1
						12.0	mA	2, 3
Is-	Supply Current				-7.0		mA	1
					-12		mA	2, 3
Ho	DC Gain	Resource ≤ 2K Ohms			-0.26	0.10	dB	1
		Resource ≤ 2K Ohms			-0.30	0.10	dB	2, 3
fclk/fc	Clock to Cutoff Frequency Ratio				48.608	49.392		1
					48.51	49.49		2, 3
Amin	Stopband Attenuation	@ 2 X fc			36		dB	1, 2, 3
Vos	DC Offset Voltage				-100	100	mV	1, 2, 3
Vo	Output Voltage Swing				-4.2	3.9	V	1
					-4.0	3.7	V	2, 3
	Additional Magnitude Response Test Points	fin = 12KHz			-9.91	-8.99	dB	1
					-9.95	-8.95	dB	2, 3
		fin = 9KHz			-1.03	-0.71	dB	1
					-1.07	-0.67	dB	2, 3
fclk	Clock Frequency Range		1, 2			750	KHz	1, 2, 3
Is+	Supply Current		2			5.0	mA	1
			2			6.5	mA	2, 3
Is-	Supply Current		2		-5.0		mA	1
			2		-6.5		mA	2, 3
Ho	DC Gain	Resource ≤ 2K Ohm	2		-0.26	o.10	dB	1
		Resource ≤ 2K Ohm	2		-0.30	0.10	dB	2, 3
fclk/fc	Clock to Cutoff Frequency Ratio		2		48.608	49.392		1
			2		48.51	49.49		2, 3
Amin	Stopband Attenuation	@ 2 X fc	2		36		dB	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = 5V, V- = -5V, fCLK = 500KHz

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vos	DC Offset Voltage		2		-60	60	mV	1, 2, 3
Vo	Output Voltage Swing		2		-2.0	1.4	V	1
			2		-1.8	1.2	V	2, 3
	Additional Magnitude Response Test Points	fin = 6KHz	2		-9.91	-8.99	dB	1
			2		-9.95	-8.95	dB	2, 3
		fin = 4.5KHz	2		-1.03	-0.71	dB	1
			2		-1.07	-0.67	dB	2, 3

DC: OP AMP PARAMETERS

Vos	Input Offset Voltage	V+ = +5V, V- = -5V			-20	20	mV	1, 2, 3
		V+ = 2.5V, V- = -2.5V			-20	20	mV	1, 2, 3
CMRR	CMRR Op Amp 2 Only	Test Input Range: -2.2V to 1.8V, V+ = +5V, V- = -5V				55	dB	1, 2, 3
CMRR	CMRR Op Amp 2 Only	Test Input Range: -2.2V to 1.8V, V+ = 2.5V, V- = -2.5V				55	dB	1, 2, 3
Vo-	Output Voltage Swing	Rl = 5K Ohm, V+ = +5V, V- = -5V				-4.2	V	1
						-4.0	V	2, 3
		Rl = 5K Ohm, V+ = 2.5V, V- = -2.5V				-1.8	V	1
						-1.6	V	2, 3
Vo+	Output Voltage Swing	Rl = 5K Ohm, V+ = +5V, V- = -5V			3.8		V	1
					3.6		V	2, 3
		Rl = 5K Ohm, V+ = 2.5V, V- = -2.5V			1.3		V	1
					1.1		V	2, 3

Electrical Characteristics

DC LOGIC INPUT-OUTPUT PARAMETER: SCHMITT TRIGGER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V- = 0V, VLsh = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vt+	Positive Going Threshold Voltage Clock In Pin	V+ = 10V	3		6.1	8.8	V	1
			3		6.0	8.9	V	2, 3
		V- = 5V	3		3.0	4.3	V	1
			3		2.9	4.4	V	2, 3
Vt-	Negative Going Threshold Voltage Clock In Pin	V+ = 10V	3		1.4	3.8	V	1
			3		1.3	3.9	V	2, 3
		V- = 5V	3		0.7	1.9	V	1
			3		0.6	2.0	V	2, 3
Vt+	Hysteresis Clock In Pin	V+ = 10V	4		2.3	7.4	V	1
			4		2.1	7.6	V	2, 3
Vt-	Hysteresis Clock In Pin	V- = 5V	4		1.1	3.6	V	1
			4		0.9	3.8	V	2, 3
Voh	Logical "1" Output Voltage Clock R Pin	Io = -10uA, V+ = 10V			9.1		V	1
					9.0		V	2, 3
		Io = -10uA, V+ = 5V			4.6		V	1
					4.5		V	2, 3
Vol	Logical "0" Output Voltage Clock R Pin	Io = 10uA, V+ = 10V				0.9	V	1
						1.0	V	2, 3
		Io = 10uA, V+ = 5V				0.4	V	1
						0.5	V	2, 3
Isource	Output Source Current Clock R Pin	CLK R Shorted to V-, V+ = 10V			4.9		mA	1
					3.7		mA	2, 3
		CLK R Shorted to V-, V+ = 5V			1.6		mA	1
					1.2		mA	2, 3
Isink	Output Sink Current Clock R Pin	CLK R Shorted to V+, V+ = 10V			4.9		mA	1
					3.7		mA	2, 3
		CLK R Shorted to V+, V+ = 5V			1.6		mA	1
					1.2		mA	2, 3

Electrical Characteristics

DC LOGIC INPUT-OUTPUT PARAMETER: TTL CLOCK INPUT, CLK R PIN

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V- = 0V, VLsh = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	Logical "1" Clock R Pin Input Voltage	V+ = +5, V- = -5V	3		2.0		V	1, 2, 3
		V+ = 2.5, V- = -2.5V	3		2.0		V	1, 2, 3
Vil	Logical "0" Clock R Pin Input Voltage	V+ = +5V, V- = -5V	3			0.8	V	1, 2, 3
		V+ = +2.5V, V- = -2.5V	3			0.6	V	1
			3			0.4	V	2, 3

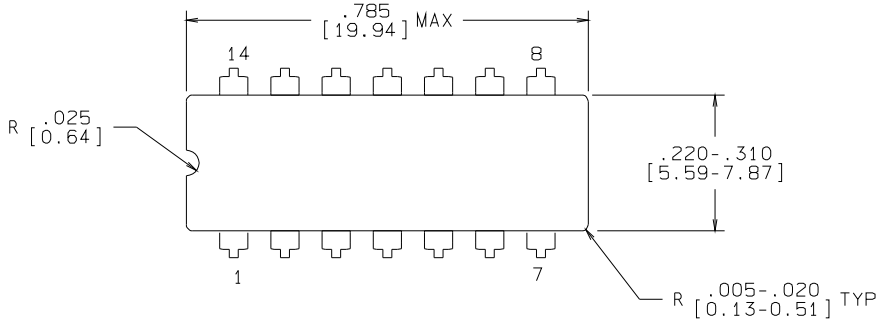
Note 1: Inversely tested.
Note 2: V+ = 2.5V, V- = -2.5V, fCLK = 250KHz.
Note 3: Parameter tested go-no-go only.
Note 4: Guaranteed by V+ and V-.

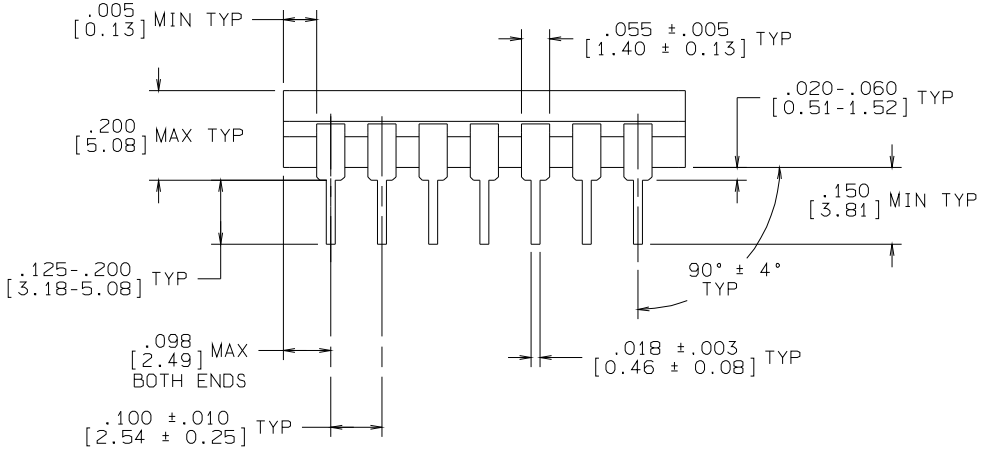
Graphics and Diagrams

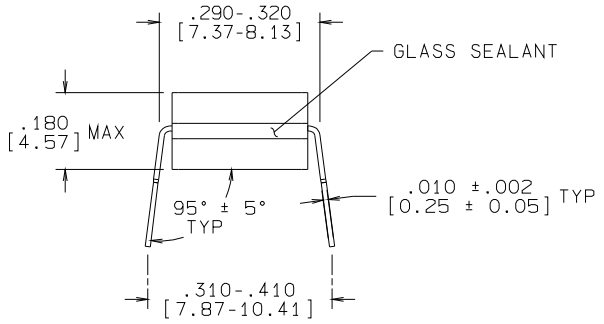
GRAPHICS#	DESCRIPTION
06093HR	(blank)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH [MM]

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CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1