National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM119-X REV 0D0

Original Creation Date: 08/29/95
Last Update Date: 05/06/97
Last Major Revision Date: 08/29/95

HIGH SPEED DUAL COMPARATOR

General Description

The LM119 precision high speed dual comparator is fabricated on a single monolithic chip. It is designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Furthermore it has a higher gain and lower input current than other devices. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA.

Industry Part Number

LM119

Prime Die

LM119

NS Part Numbers

LM119E/883
LM119H/883
LM119J/883
LM119W/883

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Two independent comparators
- Operates from a single 5V supply
- Typically 80nS response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1uA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 is fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices.

(Absolute Maximum Ratings)
(Note 1)

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 3)	±15V
ESD Tolerance (Note 4)	800V
Power Dissipation (Note 2)	500mW
Output Short Circuit Duration	10 Sec.
Maximum Junction Temperature	150 C
Storage Temperature Range	-65 C to 150 C
Lead Temperature	
Soldering, (10 seconds)	260 C
Thermal Resistance	
ThetaJA	
E Package (Still Air)	89 C/W
E Package (500LF/Min Air flow)	63 C/W
H Package (Still Air)	162 C/W
H Package (500LF/Min Air flow)	88 C/W
J Package (Still Air)	94 C/W
J Package (500LF/Min Air flow)	52 C/W
W Package (Still Air)	215 C/W
W Package (500LF/Min Air flow)	132 C/W
ThetaJC	
E Package	5 C/W
H Package	31 C/W
J Package	10.9 C/W
W Package	12.3 C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 4: Human body model, 1.5K Ohm in series with 100pF.

Recommended Operating Conditions

Operating Temperature Range

$-55\ C \leq TA \leq 125\ C$

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcm = 0V.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc+	Positive Supply Current	+Vcc = ±15V, V+ = 5.6V thru 1.4K Ohms, Vout = LOW				11	mA	1
		+Vcc = ±15V, V+ = 5.6V thru 1.4K Ohms, Vout = LOW				11.5	mA	2
Icc-	Negative Supply Current	±Vcc = ±15V, V+ = 5.6V thru 1.4K Ohms, Vout = LOW			-4.2		mA	1
		±Vcc = ±15V, V+ = 5.6V thru 1.4K Ohms, Vout = LOW			-4.5		mA	2
Ileak	Output Leakage Current	+Vcc = 15V, -Vcc = -1V Vgrd = 0V, Vout = 35V, Vin = 5mV				1.8	uA	1
						9.5	uA	2
						10	uA	3
Iib	Input Bias Current	±Vcc = ±15V				0.475	uA	1
		±Vcc = ±15V				0.95	uA	2, 3
		V+ = 5V, V- = 0V, Vcm = 1.5V				0.475	uA	1
						0.95	uA	2, 3
Vio	Input Offset Voltage	V+ = 5V, V- = 0V, Vcm = 1V, Rs = 5K Ohms			-3.8	3.8	mV	1
					-6.8	6.8	mV	2, 3
		V+ = 5V, V- = 0V, Vcm = 3V, Rs = 5K Ohms			-3.8	3.8	mV	1
					-6.8	6.8	mV	2, 3
		±Vcc = ±15V, Vcm = 12V, Rs = 5K Ohms			-3.8	3.8	mV	1
		±Vcc = ±15V, Vcm = 12V, Rs = 5K Ohms			-6.8	6.8	mV	2, 3
		±Vcc = ±15V, Vcm = -12V, Rs = 5K Ohms			-3.8	3.8	mV	1
		±Vcc = ±15V, Vcm = -12V, Rs = 5K Ohms			-6.8	6.8	mV	2, 3
Iio	Input Offset Current	V+ = 5V, V- = 0V, Vcm = 1V			-75	75	nA	1
					-100	100	nA	2, 3
		V+ = 5V, V- = 0V, Vcm = 3V			-75	75	nA	1
					-100	100	nA	2, 3
		±Vcc = ±15V, Vcm = 12V			-75	75	nA	1
		±Vcc = ±15V, Vcm = 12V			-100	100	nA	2, 3
		±Vcc = ±15V, Vcm = -12V			-75	75	nA	1
		±Vcc = ±15V, Vcm = -12V			-100	100	nA	2, 3

Electrical Characteristics

DC PARAMETERS:(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcm = 0V.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vsat	Output Saturation Voltage	V+ = 5V, V- =0V, Il = 4mA	3			0.4	V	1, 2
			3			0.6	V	3
		Vcc = ±15V, Il = 25mA, Vin = -5mV				1.5	V	1
Avs	Voltage Gain	±Vcc = ±15V, Delta Vout = 12V, Rl = 1.4K Ohms	1, 4		10.5		V/mV	4
		±Vcc = ±15V, Delta Vout = 12V, Rl = 1.4K Ohms	1, 4		10		V/mV	5, 6
		V+ = 5V, V- = 0V, Delta Vout + 4.5V, Rl = 1.4K Ohms	2, 4		8		V/mV	4
			2, 4		5		V/mV	5
			2, 4		5.8		V/mV	6

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcm = 0V. "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI)."

Icc+	Positive Supply Current	+Vcc = ±15V, V+ = 5.6V thru 1.4K Ohms, Vout = LOW			-1	1	mA	1
Icc-	Negative Supply Current	+Vcc = ±15V, V+ = 5.6V thru 1.4K Ohms, Vout = LOW			-0.5	0.5	mA	1
Vio	Input Offset Voltage	V+ = 5V, V - = 0V, Vcm = 1V, Rs = 5K Ohms			-0.4	0.4	mV	1

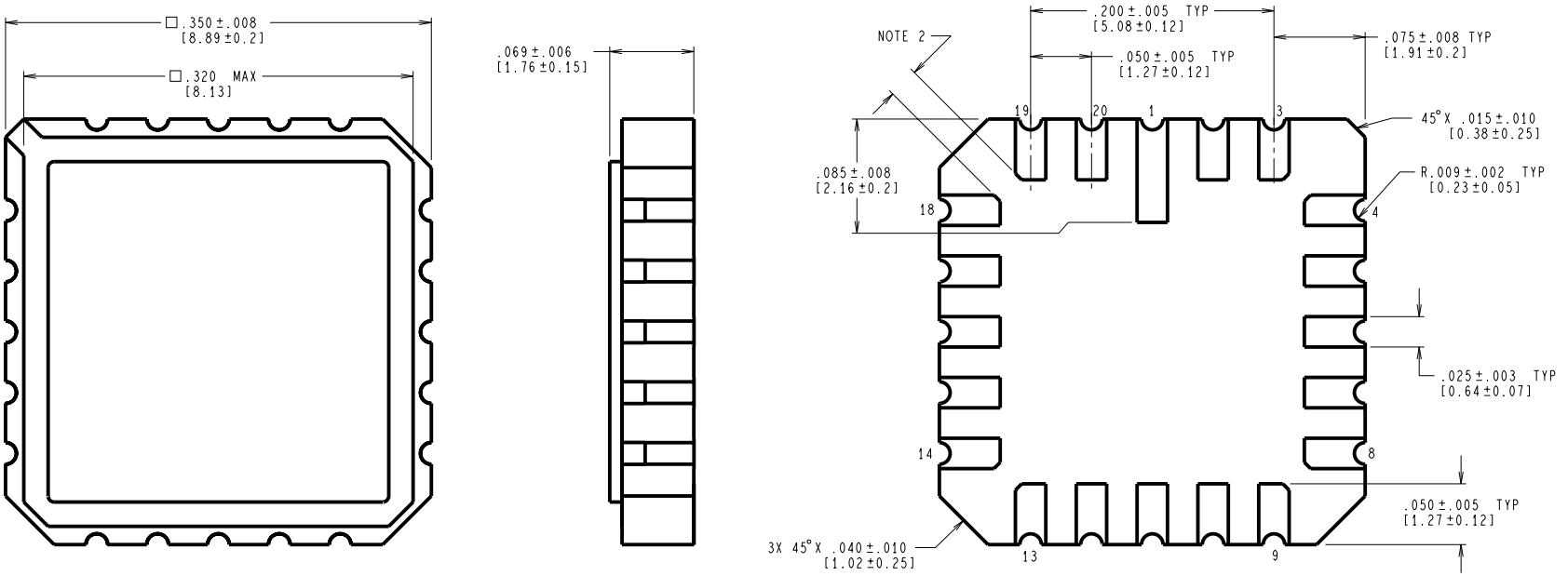
Note 1: Gain is computed with an output swing from +13.5V to +1.5V.
Note 2: Gain is computed with an output swing from +5.0V to +0.5V.
Note 3: Output is monitored by measuring Vin with limits from 0 to 6mV at all temps.
Note 4: Datalog reading in K = V/mV.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LDLESS CHIP CARRIER, TYPE C 20 TERMINAL(P/P DWG)
H10CRE	(blank)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
W10ARE	(blank)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

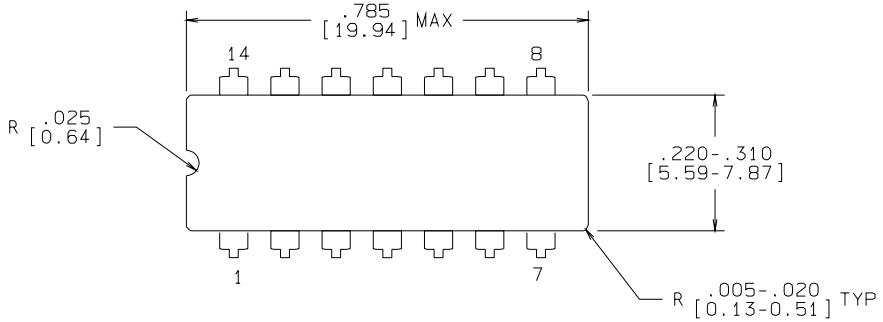
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

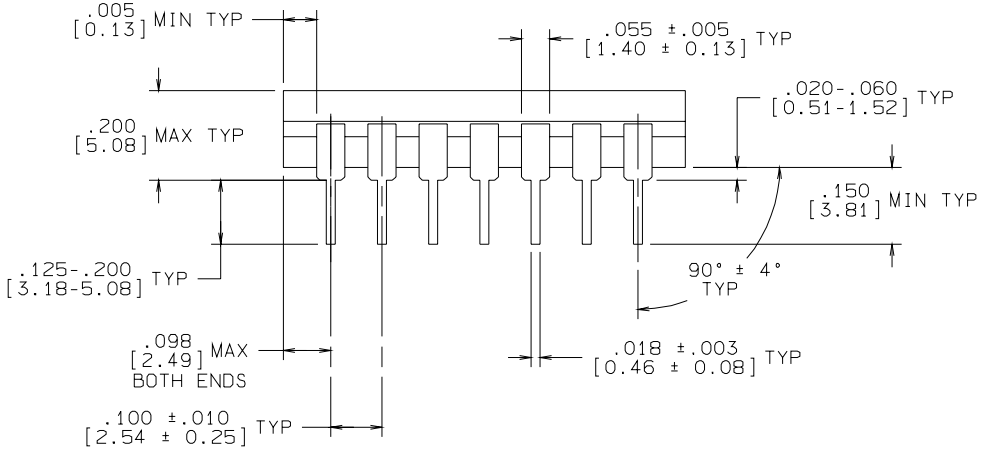
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

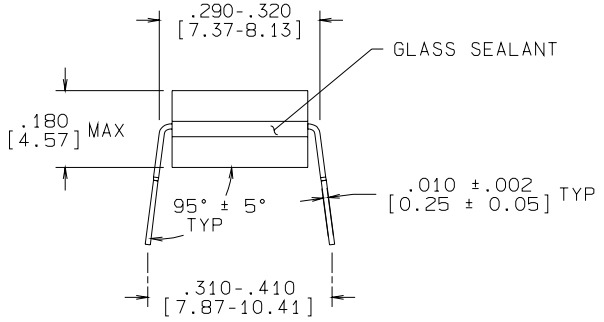
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0D0	M0001370	05/06/97	Barbara Lopez	Added Power Dissipation - Note 2 in Absolute section. Renumbered all other notes. Archive MDS - MNLM119-X Rev. 0C0. Release MDS - MNLM119-X Rev. 0D0.