

MNLF198-X REV 1AL

 Original Creation Date: 06/20/95
 Last Update Date: 08/24/98
 Last Major Revision Date: 06/25/98

MONOLITHIC SAMPLE AND HOLD
Industry Part Number

LF198

NS Part Numbers

LF198H/883

Prime Die

LF198

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_{CC} = \pm 15V$, $R_L = 10K$, $V_{in} = 0V$, $C_{hold} = 0.01\mu F$, Logic Reference Pin = 0V, Logic Pin = 4V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
I _{cc+}	Positive Supply Current	+V _{CC} = 15V, -V _{CC} = -15V				5.5	mA	1, 2
						6.5	mA	3
		+V _{CC} = 18V, -V _{CC} = -18V, Mode = "Sample"				5.5	mA	1, 2
						6.5	mA	3
		+V _{CC} = 18V, -V _{CC} = -18V, Mode = "Hold"				5.5	mA	1, 2
						6.5	mA	3
I _{cc-}	Negative Supply Current	+V _{CC} = 15V, -V _{CC} = -15V			-5.5		mA	1, 2
					-6.5		mA	3
		+V _{CC} = 18V, -V _{CC} = -18V, Mode = "Sample"			-5.5		mA	1, 2
					-6.5		mA	3
		+V _{CC} = 18V, -V _{CC} = -18V, Mode = "Hold"			-5.5		mA	1, 2
					-6.5		mA	3
V _{os}	Input Offset Voltage	+V _{CC} = 3V, -V _{CC} = -7V			-3	3	mV	1
					-5	5	mV	2, 3
		+V _{CC} = 15V, -V _{CC} = -15V			-3	3	mV	1
					-5	5	mV	2, 3
		+V _{CC} = 3.5V, -V _{CC} = -26.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+V _{CC} = 18V, -V _{CC} = -18V			-3	3	mV	1
					-5	5	mV	2, 3
		+V _{CC} = 3.5V, -V _{CC} = -32.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+V _{CC} = 26.5V, -V _{CC} = 3.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+V _{CC} = 32.5V, -V _{CC} = -3.5V, Logic = 2.5V			-3	3	mV	1
					-5	5	mV	2, 3
		+V _{CC} = 7V, -V _{CC} = -3V			-3	3	mV	1
					-5	5	mV	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_{CC} = \pm 15V$, $R_L = 10K$, $V_{in} = 0V$, $C_{hold} = 0.01\mu F$, Logic Reference Pin = 0V, Logic Pin = 4V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
I _b	Input Bias Current	+V _{CC} = 3V, -V _{CC} = -7V			-25	25	nA	1
					-75	75	nA	2, 3
		+V _{CC} = 15V, -V _{CC} = -15V			-25	25	nA	1
					-75	75	nA	2, 3
		+V _{CC} = 3.5V, -V _{CC} = -32.5V			-25	25	nA	1
					-75	75	nA	2, 3
		+V _{CC} = 32.5V, -V _{CC} = -3.5V			-25	25	nA	1
					-75	75	nA	2, 3
		+V _{CC} = 7V, -V _{CC} = -3V			-25	25	nA	1
					-75	75	nA	2, 3
I _{leak} (CAP)	Leakage Current Into Hold Capacitor	+V _{CC} = 3V, -V _{CC} = -7V			-100	100	pA	1
		+V _{CC} = 3.5V, -V _{CC} = -32.5V			-100	100	pA	1
		+V _{CC} = 32.5V, -V _{CC} = -3.5V			-100	100	pA	1
		+V _{CC} = 7V, -V _{CC} = -3V			-100	100	pA	1
V _{hs}	Hold Step	+V _{CC} = 15V, -V _{CC} = -15V			-2	2	mV	1
					-5.6	5.6	mV	2, 3
		+V _{CC} = 3.5V, -V _{CC} = -26.5V			-2.5	2.5	mV	1
					-5.6	5.6	mV	2, 3
		+V _{CC} = 26.5V, -V _{CC} = -3.5V			-2.5	2.5	mV	1
					-5.6	5.6	mV	2, 3
A _e	Gain Error	+V _{CC} = 7V, -V _{CC} = -3V				0.02	%	1
						0.06	%	2, 3
		+V _{CC} = 3.5V, -V _{CC} = -26.5V				0.005	%	1
						0.02	%	2, 3
		+V _{CC} = 32.5V, -V _{CC} = -3.5V				0.005	%	1
						0.06	%	2, 3
		+V _{CC} = 26.5V, -V _{CC} = -3.5V				0.005	%	1
						0.02	%	2, 3

Electrical Characteristics

AC/DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_{CC} = \pm 15V$, $R_L = 10K$, $V_{in} = 0V$, $C_{hold} = 0.01\mu F$, Logic Reference Pin = 0V, Logic Pin = 4V

AC: $V_{CC} = \pm 15V$, $R_L = 10K$, $V_{in} = 0V$, $C_{hold} = 0.01\mu F$, Logic Reference Pin = 0V, Logic Pin = 4V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Z _i	Input Impedance	+V _{CC} = 8V, -V _{CC} = -28V			10		G Ohm	1
					0.8		G Ohm	2, 3
		+V _{CC} = 28V, -V _{CC} = -8V			10		G Ohm	1
					0.8		G Ohm	2, 3
Z _o	Output Impedance	+V _{CC} = 18V, -V _{CC} = -18V				2	Ohm	1
						4	Ohm	2, 3
I _{CHARGE}	Capacitor Charging Current	+V _{CC} = 8V, -V _{CC} = -28V			-25	-4.5	mA	1
					-25	-3	mA	2, 3
		+V _{CC} = 28V, -V _{CC} = -8V			4.5	25	mA	1
					3	25	mA	2, 3
LOGIC	Logic Pin Current	+V _{CC} = 18V, -V _{CC} = -18V, Mode = "Sample", Logic = 7V				10	uA	1, 2, 3
		+V _{CC} = 18V, -V _{CC} = -18V, Mode = "Hold", Logic = -30V				1	uA	1
						0.5	uA	2, 3
V _{os}	Input Offset Voltage	+V _{CC} = 15V, -V _{CC} = -15V, ID _{RI} VE = +1mA			-3.5	3.5	mV	1
					-6	6	mV	2, 3
Delta V _{os}	Input Offset Voltage	+V _{CC} = 15V, -V _{CC} = -15V, ID _{RI} VE = +1mA to -1mA			-1.1	1.1	mV	1
					-2	2	mV	2, 3
I _{os} +	Output Short Circuit Current	+V _{CC} = 18V, -V _{CC} = -18V			7	20	mA	1
I _{os} -	Output Short Circuit Current	+V _{CC} = 18V, -V _{CC} = -18V			-25	7	mA	1
I _{LOGICref}	Logic Reference Pin Current	+V _{CC} = 18V, -V _{CC} = -18V, Mode = "Sample", Logic = 7V			-1	1	uA	1
					-0.5	5	uA	2, 3
		+V _{CC} = 18V, -V _{CC} = -18V, Mode = "Hold", Logic = -30V				10	uA	1, 2, 3
PSRR	Power Supply Rejection Ratio	+V _{CC} = 10V, -V _{CC} = -15V			80		dB	1
					74		dB	2, 3
		+V _{CC} = 15V, -V _{CC} = -10V			80		dB	1
					74		dB	2, 3

Electrical Characteristics

AC/DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_{CC} = \pm 15V$, $R_L = 10K$, $V_{in} = 0V$, $Chold = 0.01\mu F$, Logic Reference Pin = 0V, Logic Pin = 4V

AC: $V_{CC} = \pm 15V$, $R_L = 10K$, $V_{in} = 0V$, $Chold = 0.01\mu F$, Logic Reference Pin = 0V, Logic Pin = 4V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
FTRR	Feedthrough Rejection Ratio	$+V_{CC} = 3.5V$, $-V_{CC} = -32.5V$			86		dB	1
					74		dB	2, 3
		$+V_{CC} = 32.5V$, $-V_{CC} = -3.5V$			86		dB	1
					74		dB	2, 3
Vth	Differential Logic Level		1		0.8	2.4	V	1
Taq	Acquisition Time	$\Delta V_{out} = 10V$, $Chold = 1000pF$	2			6	μS	1
		$Chold = 0.01\mu F$				25	μS	1
Vos(2nd Stg)	2nd Stage VOS	$+V_{CC} = 3.5V$, $-V_{CC} = -32.5V$			-35	+35	mV	1
					-50	+50	mV	2, 3
		$+V_{CC} = 3V$, $-V_{CC} = -7V$			-35	+35	mV	1
					-50	+50	mV	2, 3
		$+V_{CC} = 32.5V$, $-V_{CC} = -3.5V$			-35	+35	mV	1
					-50	+50	mV	2, 3
		$+V_{CC} = 7V$, $-V_{CC} = -3V$			-35	+35	mV	1
					-50	+50	mV	2, 3

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_{CC} = \pm 15V$, $R_L = 10K$, $V_{in} = 0V$, $Chold = 0.01\mu F$, Logic Reference Pin = 0V, Logic Pin = 4V. "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI)."

Vos	Input Offset Voltage	$+V_{CC} = 15V$, $-V_{CC} = -15V$			-0.5	0.5	mV	1
Ib	Input Bias Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$			-2.5	2.5	nA	1

Note 1: Parameter tested go-no-go only.

Note 2: Sample test only Group A. Subgroup 4, SS=116/0 or 100% if not <116 pcs.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05022HR	(blank)
H08CRE	(blank)

See attached graphics following this page.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1AL	M0002942	08/24/98	Rose Malone	Updated MDS: MNLF198-X Rev. 0BL to MNLF198-X Rev. 1AL. TYPO: Vhs, Condition +Vcc = 25.5V, -Vcc = -3.5V Changed min. from -5.5 to -5.6, typo made at the time of RETS to MDS conversion.