National Semiconductor

# MICROCIRCUIT DATA SHEET

## MNCLC532A-X REV 0A0

Original Creation Date: 07/17/98
Last Update Date: 04/05/99
Last Major Revision Date: 09/24/98

# HIGH-SPEED 2:1 ANALOG MULTIPLEXER

## General Description

The CLC532 is a high-speed 2:1 multiplexer with active input and output stages. The CLC532 also employs a closed-loop design which dramatically improves accuracy. This accurate monolithic device is constructed using an advanced high-performance bipolar process.

The CLC532 has been specifically designed to provide settling times of 17ns to 0.01%. This design, coupled with the adjustable noise bandwidth, makes the CLC532 an ideal choice for infrared and CCD imaging systems. Channel-to-channel isolation is better than 80dB @ 10MHz. Low distortion (80dBc) and spurious signal levels make the CLC532 a very suitable choice for both I/Q processors and receivers.

## Industry Part Number

CLC532A

## NS Part Numbers

CLC532AE-QML**
CLC532AJ-QML*

## Prime Die

UB1451A

## Controlling Document

5962-9203501MCA*, M2A**

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## Processing

MIL-STD-883, Method 5004

## Quality Conformance Inspection

MIL-STD-883, Method 5005

| Subgrp | Description | Temp (°C) |
|---|---|---|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |

## Features

- 12-bit settling (0.01%) - 17ns
- Low noise - 32uVrms
- High isolation - 80dB @ 10MHz
- Low distortion - 80dB @ 5MHz
- Adjustable bandwidth - 190MHz (max)

## Applications

- Infrared system multiplexing
- CCD sensor signals
- Radar I/Q switching
- High definition video HDTV
- Test and calibration

# (Absolute Maximum Ratings)

(Note 1)

| | | |
|---|---|---|
| Positive Supply Voltage (+Vcc) | | -0.5V to +7.0V |
| Negative Supply Voltage (-Vee) | | +0.5V to -7.0V |
| Differential Voltage Between Any Two Ground Pins | | 200mV |
| Analog Input Voltage Range | | -Vee to +Vcc |
| Digital Input Voltage Range | | -Vee to +Vcc |
| Maximum Power Dissipation (Pd) (Note 2) | | |
| Ceramic DIP | | 1.76 W |
| LCC | | 3.0 W |
| Output Current (Iout) | | 36mA |
| Output Short Circuit Duration (output shorted to GND) | | Infinite |
| Junction Temperature (Tj) | | +175 C |
| Storage Temperature Range | | -65 C to +150 C |
| Lead Temperature (soldering, 10 seconds) | | +300 C |
| Thermal Resistance | | |
| Junction -to-ambient | (ThetaJA) | |
| Ceramic DIP | (Still Air) | TBD |
| | (500 LFPM) | TBD |
| LCC | (Still Air) | TBD |
| | (500 LFPM) | TBD |
| Junction -to-case | (ThetaJC) | |
| Ceramic DIP | | TBD |
| LCC | | TBD |
| Package Weight (Typical) | | |
| Ceramic DIP | | 2190 mg |
| LCC | | TBD |
| ESD Tolerance (Note 3) | | |
| ESD Rating | | 500 V |

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

## Recommended Operating Conditions

| | |
|---|---|
| Positive Supply Voltage (+Vcc) | +5.0V |
| Negative Supply Voltage (-Vee) | -5.2V or -5.0V |
| Differential Voltage Between Any Two Ground Pins | 10mV |
| Analog Input Voltage Range | $\pm$2V |
| SELECT Input Voltage Range (TTL Mode) | 0V to +3.0V |
| SELECT Input Voltage Range (ECL Mode) | -2.0V to 0V |
| COMPENSATION Capacitance Range (Ccomp) | 0pF to 100pF |
| Ambient Operating Temperature Range (Ta) | -55 C to +125 C |

# Electrical Characteristics

## DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: +Vs = +5.0V, -Vs = -5.2V, Rin = 50Ohms, Rl = 500Ohms, Ccomp = 10pF, and ECL mode, pin 6 = no connection. See figure 3. -55 C ≤ Ta ≤ +125 C (Note 3).

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| IBN | Input Bias Current | | | | -120 | +120 | uA | 1, 2 |
| | | | | | -250 | +250 | uA | 3 |
| Voo | Output Offset Voltage | | | | -3.5 | +3.5 | mV | 1, 2 |
| | | | | | -6.5 | +6.5 | mV | 3 |
| Icc | Supply Current | Vcc = +5V, Vin = 0V, no load | | | 18 | 28 | mA | 1 |
| | | | | | 16 | 25 | mA | 2 |
| | | | | | 18 | 30 | mA | 3 |
| Iee | Supply Current | Vee = -5.2V, Vin = 0V, no load | | | -30 | -19 | mA | 1 |
| | | | | | -26 | -16 | mA | 2 |
| | | | | | -31 | -19 | mA | 3 |
| PSRR | Power Supply Rejection Ratio | | | | | -63 | dB | 1 |
| | | | | | | -64 | dB | 2 |
| | | | | | | -60 | dB | 3 |
| GA | Gain Accuracy | ±2V | | | .988 | 1.000 | V/V | 1, 2, 3 |
| SSBW | Small Signal Bandwidth | -3 dB Bandwidth, Vout < 0.1 Vpp | | | 140 | | MHz | 4 |
| | | | 2 | | 110 | | MHz | 5 |
| | | | 2 | | 140 | | MHz | 6 |
| GFP | Gain Flatness Peaking | Vout < 0.1 Vpp, at 0.1 MHz to 200 MHz | | | | 0.7 | dB | 4 |
| | | | 2 | | | 0.8 | dB | 5 |
| | | | 2 | | | 0.7 | dB | 6 |
| GFR | Gain Flatness Rolloff | Vout < 0.1 Vpp, at 0.1 MHz to 100 MHz | | | -1.8 | | dB | 4 |
| | | | 2 | | -2.6 | | dB | 5 |
| | | | 2 | | -1.8 | | dB | 6 |
| HD2 | 2nd Harmonic Distortion | 2 Vpp at 5 MHz | | | | -67 | dBc | 4 |
| | | | 2 | | | -67 | dBc | 5, 6 |
| HD3 | 3rd Harmonic Distortion | 2 Vpp at 5 MHz | | | | -68 | dBc | 4 |
| | | | 2 | | | -68 | dBc | 5, 6 |

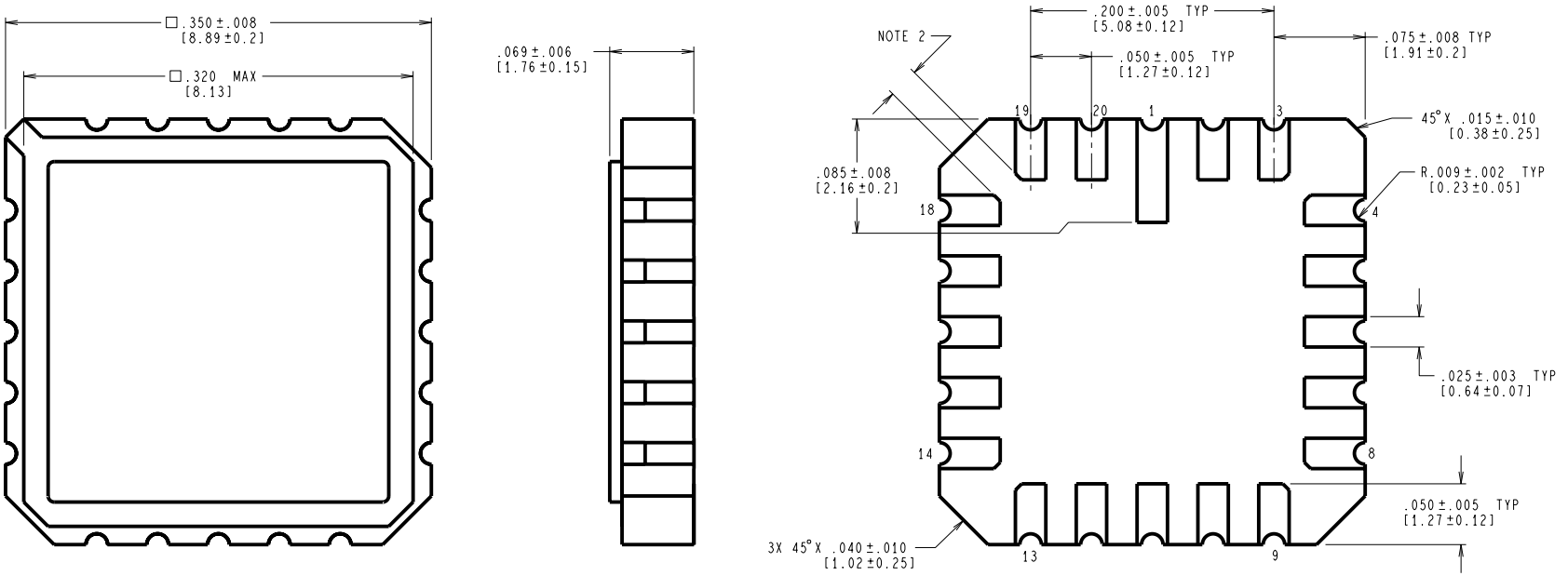
Note 1: If not tested, shall be guaranteed to the limits specified in table I
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

## Graphics and Diagrams

| GRAPHICS# | DESCRIPTION |
|---|---|
| 07067HRA2 | CERDIP (J), 14 LEAD (B/I CKT) |
| 07074HRA2 | LCC (E), TYPE C, 20 TERMINAL (B/I CKT) |
| E20ARE | LCC (E), TYPE C, 20 TERMINAL(P/P DWG) |
| J14ARH | CERDIP (J), 14 LEAD (P/P DWG) |
| P000398A | CERDIP (J), 14 LEAD (PINOUT) |
| P000399A | LCC (E), TYPE C, 20 TERMINAL (PINOUT) |

**See attached graphics following this page.**

| REVISIONS | | | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
| E | REVISE AND REDRAW. | 10005 | 02/10/94 | DEG/ |




CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

| APPROVALS | DATE |
|---|---|
| DRAWN: Dwayne Grady | 02/10/94 |
| DFTG. CHK. | |
| ENGR. CHK. | |
| APPROVAL | |

PROJECTION INCH [MM]

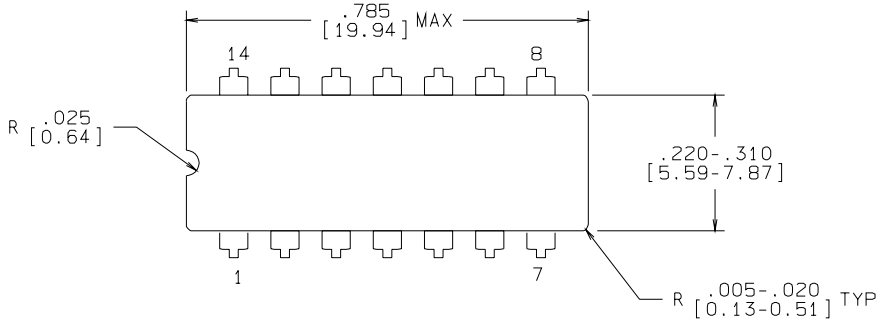
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

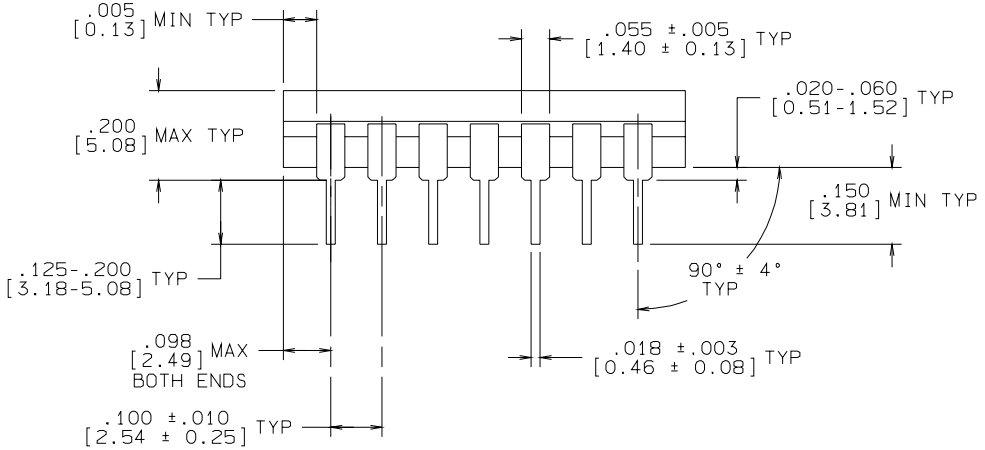
# LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

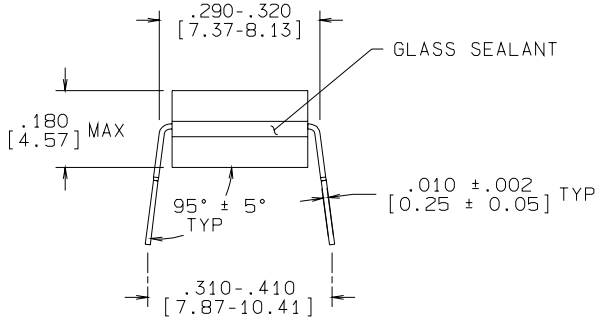
| SCALE | SIZE | DRAWING NUMBER | REV |
|---|---|---|---|
| N/A | C | MKT-E20A | E |

DO NOT SCALE DRAWING | SHEET 1 of 1

| REVISIONS | | | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
| H | REVISE PER CURRENT STD; REDRAW | 10001 | 09/15/93 | TL/ |




CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

| APPROVALS | DATE |
|---|---|
| DRAWN T. LEQUANG | 09/15/93 |
| DFTG. CHK. | |
| ENGR. CHK. | |
| APPROVAL | |

PROJECTION

INCH
[MM]

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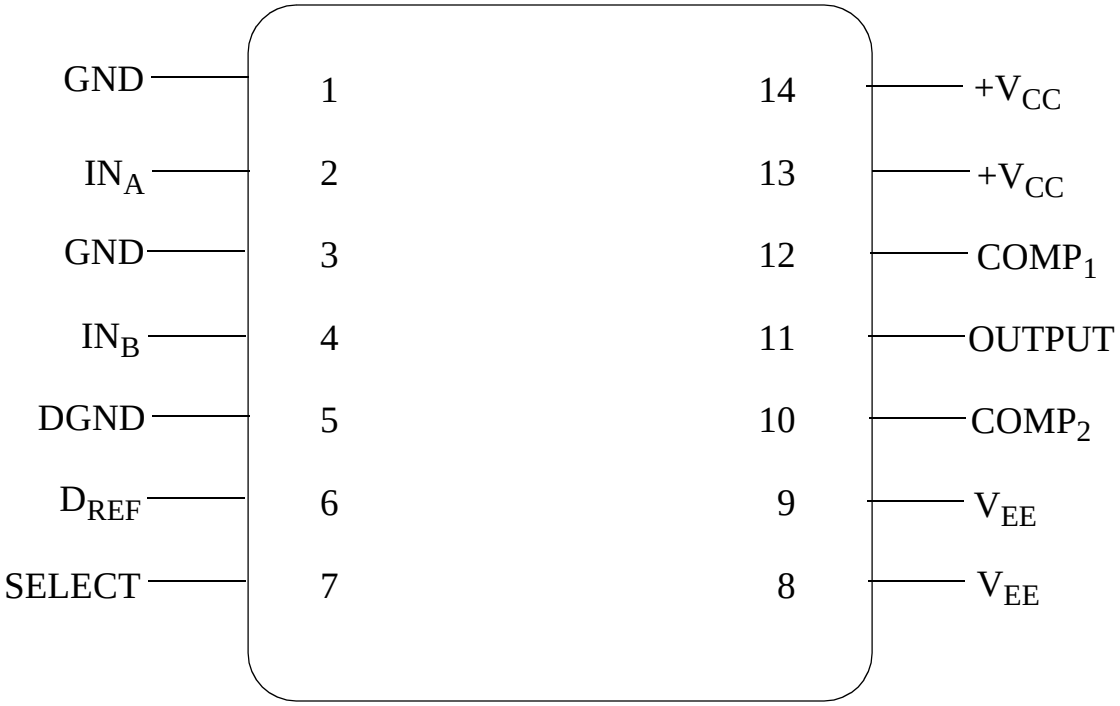
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

# CERDIP (J), 14 LEAD,

| SCALE | SIZE | DRAWING NUMBER | REV |
|---|---|---|---|
| N/A | B | MKT-J14A | H |

DO NOT SCALE DRAWING | SHEET 1 OF 1




# CLC532J
# 14 - LEAD DIP
# CONNECTION DIAGRAM
# TOP VIEW
# P000398A

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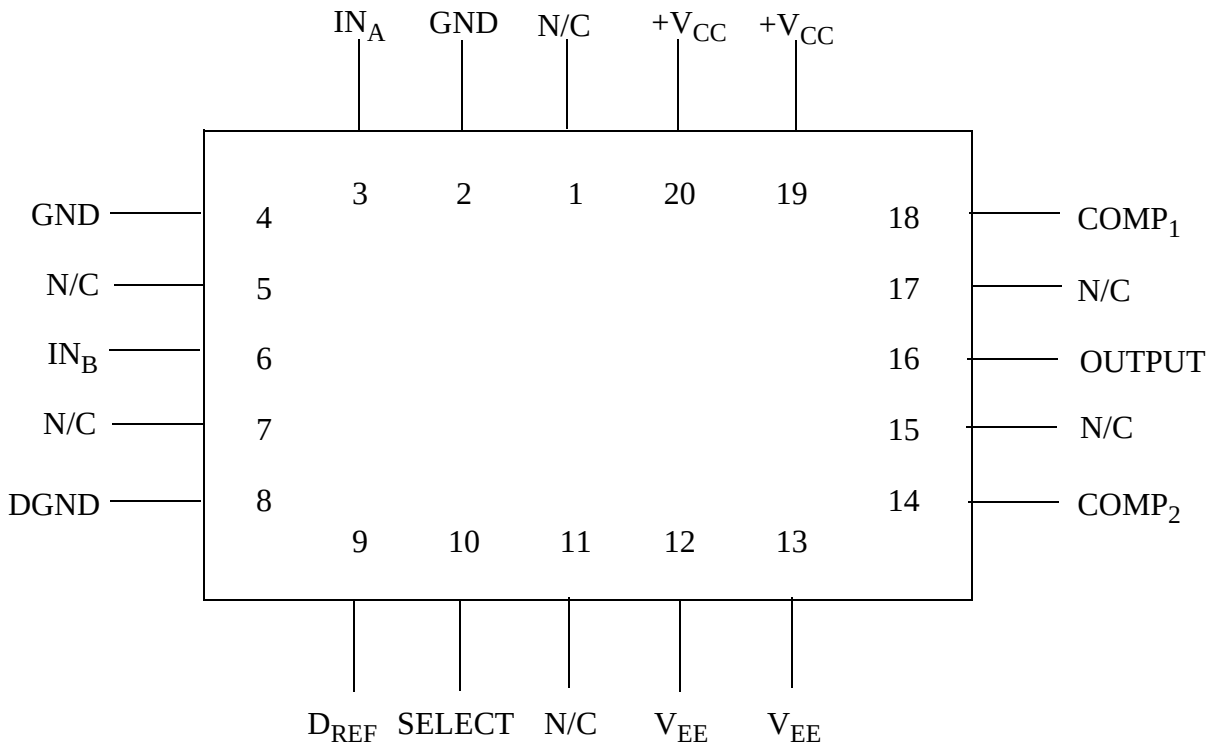
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050




# CLC532E
# 20 - LEAD LCC
# CONNECTION DIAGRAM
# TOP VIEW
# P000399A

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## Revision History

| Rev | ECN # | Rel Date | Originator | Changes |
|---|---|---|---|---|
| 0A0 | M0003339 | 04/05/99 | Shaw Mead | Initial MDS Release |