National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC520A-X REV 0A0

Original Creation Date: 08/04/98
Last Update Date: 04/27/99
Last Major Revision Date: 08/04/98

AMPLIFIER WITH VOLTAGE CONTROLLED GAIN, AGC+AMP

General Description

The CLC520 is a wideband DC-coupled amplifier with voltage-controlled gain (AGC). The amplifier has a high-impedance differential signal input, a high-bandwidth gain control input and a single-ended voltage output. Signal channel performance is outstanding with 160MHz small signal bandwidth, 0.5 degree linear phase deviation (to 60MHz) and 0.04% signal nonlinearity at 4Vpp output.

Gain-control is very flexible. Maximum gain may be set over a nominal range of 2 to 100 with one external resistor. In addition, the gain-control input provides more than 40dB of voltage-controlled gain adjustment from the maximum gain setting. For example, a CLC520 may be set for a maximum gain of 2 (or 6dB) for a voltage-controlled gain range from 6dB to less than -34dB. Alternatively, the CLC520 could be set for a maximum gain of 100 (40dB) for a voltage-controlled gain range from 40dB to less than 0dB.

Besides being flexible, the gain-control is easy to use. Gain-control bandwidth is superb, 100MHz, simplifying AGC/ALC loop stabilization. Since the gain is minimum with a zero volt input and maximum with a +2 volt input, driving the control input is simple.

Industry Part Number

CLC520A

NS Part Numbers

CLC520AJ-QML

Prime Die

UB1278A

Controlling Document

5962-9169401MCA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 160MHz, -3dB bandwidth
- 2000V/usec slew rate
- 0.04% signal nonlinearity at 4Vpp output
- -43dB feedthrough at 30MHz
- User adjustable gain range
- Differential voltage input and single-ended voltage output

Applications

- Wide-bandwidth AGC systems
- Automatic signal-leveling
- Video signal processing
- Voltage controlled filters
- Differential amplifier
- Amplitude modulation

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (V±)	±7V dc
Output Current (Iout)	70mA
Common Mode Input Voltage (Vcm)	V±
Differential Input Voltage	10V
Gain Controlled Input Voltage	V±
Referenced Input Voltage (Vref)	V±
Maximum Power Dissipation (Pd) (Note 2)	1.2W
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C to +150 C
Lead Temperature (soldering, 10 seconds)	+300 C
Thermal Resistance	
Junction -to-ambient (ThetaJA)	
Ceramic DIP (Still Air)	98 C/W
(500 LFPM)	63 C/W
Junction -to-case (ThetaJC)	
Ceramic DIP	23 C/W
Package Weight (Typical)	
Ceramic DIP	2160 mg
ESD Tolerance (Note 3)	
ESD Rating	500 V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100 pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (V±)	±5V dc
Gain Range (Av)	±2 to ±100
Reference Input Voltage (Vref)	±150mV
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Static and DC Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = +5V dc, Av = +10, load resistance (Rl) = 100 Ohms, feedback resistance (Rf) = 1 KOhms, and gain setting resistance (Rg) = 182 Ohms. -55 C ≤ Ta ≤ +125 C. (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (noninverting)				-28	+28	uA	1, 2
					-61	+61	uA	3
-Iin	Input Bias Current (inverting)				-28	+28	uA	1, 2
					-61	+61	uA	3
Voo	Output Offset Voltage				-120	+120	mV	1
					-150	+150	mV	2, 3
TC (+Iin)	Average +Input Bias Current Drift		1		-165	+165	nA/C	2
			1		-415	+415	nA/C	3
TC (-Iin)	Average -Input Bias Current Drift		1		-165	+165	nA/C	2
			1		-415	+415	nA/C	3
TC (Voo)	Average Output Offset Voltage Drift		1		-300	+300	uV/C	2
			1		-400	+400	uV/C	3
+Vo	Output Voltage Swing	No Load	1		+3.2		V	1
			1		+3.0		V	2, 3
-Vo	Output Voltage Swing	No Load	1			-3.2	V	1
			1			-3.0	V	2, 3
Icc	Quiescent Supply Current	No Load				38	mA	1, 2, 3
PSS	Power Supply Sensitivity	V+ = +4.5V to +5.0V, V- = -4.5V to -5.0V, output referred dc				-31	dB	1, 2, 3
Vg	Gain Controlled Input Voltage		1		0	2	V	1, 2, 3
CMRR	Common Mode Rejection Ratio	Vcm = 1.0V	1		59		dB	1, 2, 3
Iio	Input Offset Current		1			2	uA	1, 2
			1			4	uA	3
TC (Iio)	Average Input Offset Current Drift		1			20	uA/C	2
			1			40	uA/C	3
GACCU	Gain Accuracy	Av = 20dB, Rf = 1KOhms, Rg = 182Ohms	1		-0.5	+0.5	dB	1, 2
			1		-1.0	+1.0	dB	3
SGNL	Integral Signal Nonlineraity	Vout = 4Vpp	1			0.1	%	1, 3
			1			0.2	%	2

Electrical Characteristics

DC PARAMETERS: Static and DC Characteristics(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = +5V dc, Av = +10, load resistance (Rl) = 100 Ohms, feedback resistance (Rf) = 1 KOhms, and gain setting resistance (Rg) = 182 Ohms. -55 C ≤ Ta ≤ +125 C. (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Vdm	Differential Voltage Range	Rg = 182Ohms	1		+250		mV	1, 3
			1		+210		mV	2
-Vdm	Differential Voltage Range	Rg = 182Ohms	1			-250	mV	1, 3
			1			-210	mV	2
Rin	Signal Input Resistance		1		100		KOhms	1, 2
			1		50		KOhms	3
Cin	Signal Input Capacitance		1			2	pF	1, 2, 3
Rinc	Gain Controlled Input Resistance		1		600		Ohms	1, 2
			1		535		Ohms	3
Cinc	Gain Controlled Input Capacitance		1			2	pF	1, 2, 3
+Vcm	Common Mode Voltage Range	No Load	1		+2		V	1, 2
			1		+1.4		V	3
-Vcm	Common Mode Voltage Range	No Load	1			-2	V	1, 2
			1			-1.4	V	3
+Iout	Output Current		1		+50		mA	1, 2
			1		+30		mA	3
-Iout	Output Current		1			-50	mA	1, 2
			1			-30	mA	3
Rout	Output Impedance	At dc	1			0.2	Ohms	1, 2
			1			0.3	Ohms	3

Electrical Characteristics

AC PARAMETERS: Frequency Domain Response

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±5V dc, gain setting voltage (Vg) = +1.1V, Av = 10V/V, load resistance (Rl) = 100 Ohms, feedback resistance (Rf) = 1 KOhms, and gain setting resistance (Rg) = 182 Ohms -55 C ≤ Ta ≤ +125 C (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
GFPL	Gain Flatness Peaking Low	0.1MHz to 30MHz, Vout < 0.5 Vpp				0.3	dB	4
			2			0.4	dB	5, 6
GFPH	Gain Flatness Peaking High	0.1MHz to 200MHz, Vout < 0.5 Vpp				0.5	dB	4
			2			0.7	dB	5, 6
GFR	Gain Flatness Rolloff	0.1MHz to 30MHz, Vout < 0.5 Vpp				0.3	dB	4
			2			0.4	dB	5, 6
		0.1MHz to 60MHz, Vout < 0.5 Vpp				1.0	dB	4
			2			1.3	dB	5, 6
SSBW	Small Signal Bandwidth	-3dB bandwidth, Vout < 0.5Vpp			120		MHz	4
			2		120		MHz	5
			2		110		MHz	6
LSBW	Large Signal Bandwidth	-3dB bandwidth, Vout < 4Vpp	1		100		MHz	4, 5
			1		85		MHz	6
SBWC	Gain Control Channel Small Signal Bandwidth	-3dB bandwidth, Vout < 0.5Vpp, Vin = +0.2V, Vg = +1V dc	1		80		MHz	4, 5, 6
LPD	Linear Phase Deviation	0.1MHz to 60MHz	1			1	Deg	4
			1			1.2	Degrees	5, 6
FDTH	Feedthrough	Vin = -22dBm at 30MHz, Vg = 0V	1			-35	dB	4, 5, 6

Electrical Characteristics

AC PARAMETERS: Time Domain Response

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vs = ±5V dc, gain setting voltage (Vg) = +1.1V, Av = 10V/V, load resistance (Rl) = 100 Ohms, feedback resistance (Rf) = 1 KOhms, and gain setting resistance (Rg) = 182 Ohms -55 C ≤ Ta ≤ +125 C (Note 3) .

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	2nd Harmonic Distortion	2 VPP, 20MHz				-40	dBc	4
			2			-35	dBc	5
			2			-40	dBc	6
HD3	3rd Harmonic Distortion	2 VPP, 20MHz				-50	dBc	4
			2			-45	dBc	5
			2			-50	dBc	6
SNF	Equivalent Output Noise Floor	0.1MHz to 200MHz	1			-130	dBm/Hz	4, 6
			1			-129	dBm/Hz	5
INV	Equivalent Output Integrated Noise	1MHz to 200MHz	1			1000	uV	4, 6
			1			1100	uV	5
TRS	Rise and Fall Time	0.5V step, Cl < 10pF, measured between 10% and 90%	1			3	ns	9, 10
			1			3.7	ns	11
TRL	Rise and Fall Time	4V step, Cl < 10pF, measured between 90% and 10%	1			5	ns	9, 10, 11
tS	Settling Time	2V step at 0.1% of the final value, Cl < 10pF	1			18	ns	9, 10, 11
OS	Overshoot	0.5V step, Cl < 10pF	1			15	%	9, 10, 11
+SR	Slew Rate	Rising Edge, measured at ±1V with 4V step, Cl < 10pF	1		1450		V/us	9, 10, 11
-SR	Slew Rate	Falling Edge, measured at ±1V with 4V step, Cl < 10pF	1		1450		V/us	9, 10, 11

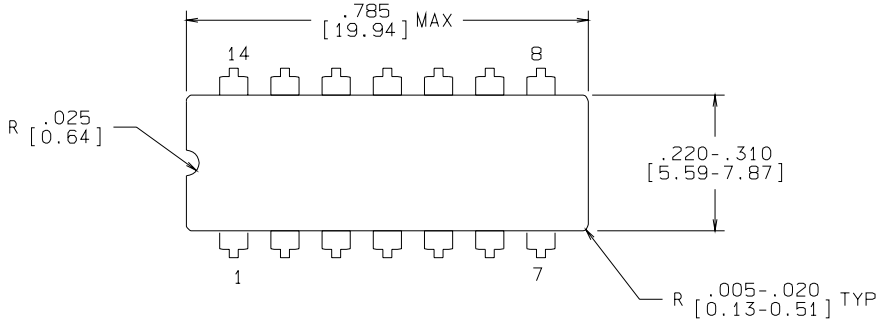
Note 1: If not tested, shall be guaranteed to the limits specified in table I herein.
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

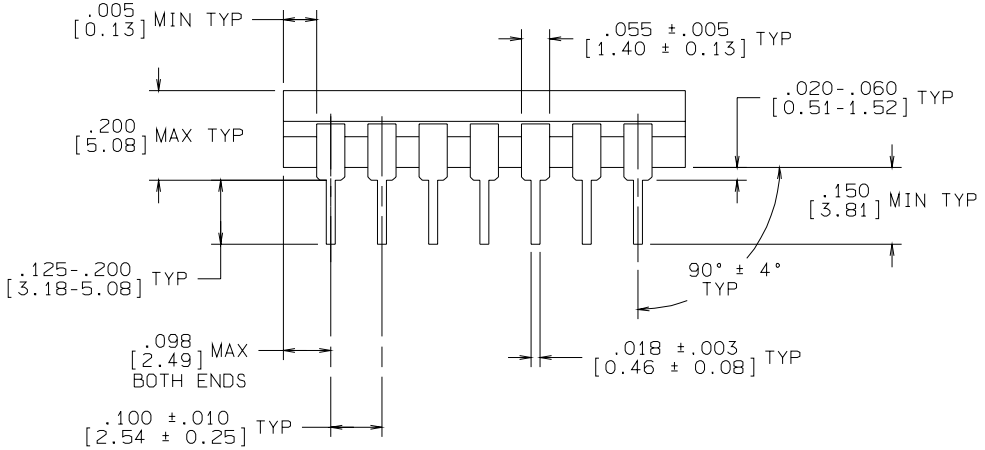
Graphics and Diagrams

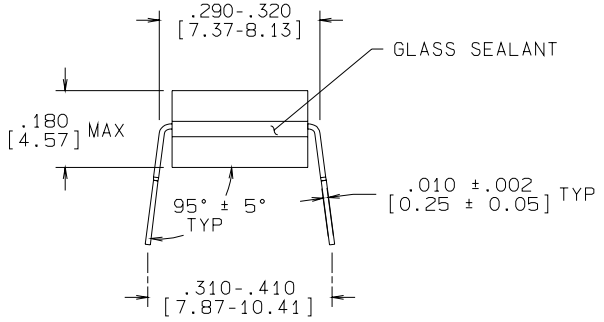
GRAPHICS#	DESCRIPTION
07079HRA2	CERDIP (J), 14 LEAD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000403A	CERDIP (J),14 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

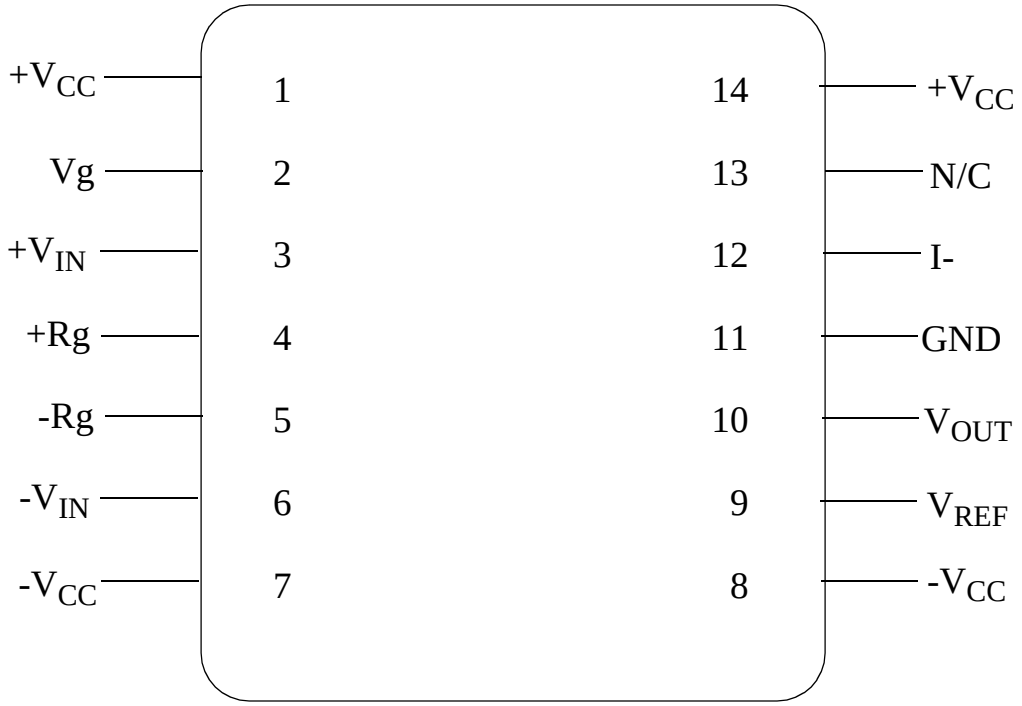
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC520J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000403A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003379	04/27/99	Shaw Mead	Initial MDS Release