

LMC7101

Tiny Low Power Operational Amplifier with Rail-To-Rail Input and Output

General Description

The LMC7101 is a high performance CMOS operational amplifier available in the space saving SOT 23-5 Tiny package. This makes the LMC7101 ideal for space and weight critical designs. The performance is similar to a single amplifier of the LMC6482/4 type, with rail-to-rail input and output, high open loop gain, low distortion, and low supply currents.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

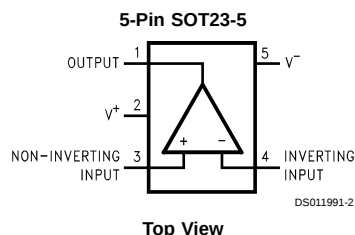
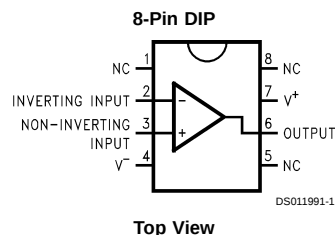
Features

- Tiny SOT23-5 package saves space—typical circuit layouts take half the space of SO-8 designs
- Guaranteed specs at 2.7V, 3V, 5V, 15V supplies
- Typical supply current 0.5 mA at 5V
- Typical total harmonic distortion of 0.01% at 5V
- 1.0 MHz gain-bandwidth
- Similar to popular LMC6482/4
- Input common-mode range includes V^- and V^+
- Tiny package outside dimensions—120 x 118 x 56 mils, 3.05 x 3.00 x 1.43 mm

Applications

- Mobile communications
- Notebooks and PDAs
- Battery powered products
- Sensor interface

Connection Diagrams



Package	Ordering Information	NSC Drawing Number	Package Marking	Supplied As
8-Pin DIP	LMC7101AIN	N08E	LMC7101AIN	Rails
8-Pin DIP	LMC7101BIN	N08E	LMC7101BIN	Rails
5-Pin SOT 23-5	LMC7101AIM5	MA05A	A00A	250 Units on Tape and Reel
5-Pin SOT 23-5	LMC7101BIM5	MA05A	A00B	250 Units on Tape and Reel
5-Pin SOT 23-5	LMC7101AIM5X	MA05A	A00A	3k Units Tape and Reel
5-Pin SOT 23-5	LMC7101BIM5X	MA05A	A00B	3k Units Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Difference Input Voltage	$\pm$ Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin	± 5 mA
Current at Output Pin (Note 3)	± 35 mA
Current at Power Supply Pin	35 mA
Lead Temp. (Soldering, 10 sec.)	260°C

Storage Temperature Range	-65°C to +150°C
Junction Temperature (Note 4)	150°C

Recommended Operating Conditions (Note 1)

Supply Voltage	$2.7V \leq V^+ \leq 15.5V$
Junction Temperature Range	$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$
LMC7101AI, LMC7101BI	
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M05A Package, 5-Pin Surface Mt.	325°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$. **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 2.7V$	0.11	6	9	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1			$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current		1.0	64	64	pA max
I_{OS}	Input Offset Current		0.5	32	32	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0V \leq V_{CM} \leq 2.7V$ $V^+ = 2.7V$	70	55	50	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = V$ For CMRR ≥ 50 dB	0.0	0.0	0.0	V min
			3.0	2.7	2.7	V max
PSRR	Power Supply Rejection Ratio	$V^+ = 1.35V$ to $1.65V$ $V^- = -1.35V$ to $-1.65V$ $V_{CM} = 0$	60	50	45	dB min
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$R_L = 2\text{ k}\Omega$	2.45	2.15	2.15	V min
			0.25	0.5	0.5	V max
		$R_L = 10\text{ k}\Omega$	2.68	2.64	2.64	V min
			0.025	0.06	0.06	V max
I_S	Supply Current		0.5	0.81 0.95	0.81 0.95	mA max
SR	Slew Rate	(Note 8)	0.7			V/ μs
GBW	Gain-Bandwidth Product		0.6			MHz

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L = 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11	4	7	mV

3V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L = 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
				6	9	max
TCV_{OS}	Input Offset Voltage Average Drift		1			$\mu\text{V}/^\circ\text{C}$
I_B	Input Current		1.0	64	64	pA max
I_{OS}	Input Offset Current		0.5	32	32	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 3\text{V}$ $V^+ = 3\text{V}$	74	64	60	db min
V_{CM}	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{ dB}$	0.0	0.0	0.0	V min
			3.3	3.0	3.0	V max
PSRR	Power Supply Rejection Ratio	$V^+ = 1.5\text{V to } 7.5\text{V}$ $V^- = -1.5\text{V to } -7.5\text{V}$ $V_O = V_{CM} = 0$	80	68	60	dB min
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$R_L = 2\text{ k}\Omega$	2.8	2.6	2.6	V min
			0.2	0.4	0.4	V max
		$R_L = 600\Omega$	2.7	2.5	2.5	V min
			0.37	0.6	0.6	V max
I_S	Supply Current		0.5	0.81	0.81	mA
				0.95	0.95	max

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L = 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 5\text{V}$	0.11	3 5	7 9	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			$\mu\text{V}/^\circ\text{C}$
I_B	Input Current		1	64	64	pA max
I_{OS}	Input Offset Current		0.5	32	32	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 5\text{V}$	82	65 60	60 55	db min
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 5\text{V}$ to 15V $V^- = 0\text{V}$, $V_O = 1.5\text{V}$	82	70 65	65 62	dB min
-PSRR	Negative Power Supply Rejection Ratio	$V^- = -5\text{V}$ to -15V $V^+ = 0\text{V}$, $V_O = -1.5\text{V}$	82	70 65	65 62	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{ dB}$	-0.3	-0.20 0.00	-0.20 0.00	V min
			5.3	5.20 5.00	5.20 5.00	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$R_L = 2\text{ k}\Omega$	4.9	4.7 4.6	4.7 4.6	V min
			0.1	0.18 0.24	0.18 0.24	V max
		$R_L = 600\Omega$	4.7	4.5 4.24	4.5 4.24	V min
			0.3	0.5 0.65	0.5 0.65	V max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0\text{V}$	24	16 11	16 11	mA min
		Sinking, $V_O = 5\text{V}$	19	11 7.5	11 7.5	mA min
I_S	Supply Current		0.5	0.85 1.0	0.85 1.0	mA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L = 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	$F = 10\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 4.0\text{ V}_{PP}$	0.01			%
SR	Slew Rate		1.0			V/ μs
GBW	Gain Bandwidth Product		1.0			MHz

15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 15\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L = 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11			mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			$\mu\text{V}/^\circ\text{C}$
I_B	Input Current		1.0	64	64	pA max
I_{OS}	Input Offset Current		0.5	32	32	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 15\text{V}$	82	70 65	65 60	dB min
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 5\text{V}$ to 15V $V^- = 0\text{V}$, $V_O = 1.5\text{V}$	82	70 65	65 62	dB min
-PSRR	Negative Power Supply Rejection Ratio	$V^- = -5\text{V}$ to -15V $V^+ = 0\text{V}$, $V_O = -1.5\text{V}$	82	70 65	65 62	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5\text{V}$ For CMRR $\geq 50\text{ dB}$	-0.3	-0.20 0.00	-0.20 0.00	V min
			15.3	15.20 15.00	15.20 15.00	V max
A_V	Large Signal Voltage Gain	$R_L = 2\text{ k}\Omega$ Sourcing (Note 7)	340	80 40	80 40	V/mV
		Sinking	24	15 10	15 10	
		$R_L = 600\Omega$ Sourcing (Note 7)	300	34	34	V/mV
		Sinking	15	6	6	
C_{IN}	Input Capacitance		3			pF
V_O	Output Swing	$V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$	14.7	14.4 14.2	14.4 14.2	V min
			0.16	0.32 0.45	0.32 0.45	V max
		$V^+ = 15\text{V}$ $R_L = 600\Omega$	14.1	13.4 13.0	13.4 13.0	V min
			0.5	1.0 1.3	1.0 1.3	V max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0\text{V}$ (Note 9)	50	30 20	30 20	mA min
		Sinking, $V_O = 12\text{V}$ (Note 9)	50	30 20	30 20	mA min
I_S	Supply Current		0.8	1.50 1.71	1.50 1.71	mA max

15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 15\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L = 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
SR	Slew Rate	$V^+ = 15\text{V}$ (Note 8)	1.1	0.5 0.4	0.5 0.4	V/ μs min
GBW	Gain-Bandwidth Product	$V^+ = 15\text{V}$	1.1			MHz
ϕ_m	Phase Margin		45			Deg
G_m	Gain Margin		10			dB
e_n	Input-Referred Voltage Noise	$F = 1\text{ kHz}$ $V_{CM} = 1\text{V}$	37			$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
i_n	Input-Referred Current Noise	$F = 1\text{ kHz}$	1.5			$\frac{\text{fA}}{\sqrt{\text{Hz}}}$
T.H.D.	Total Harmonic Distortion	$F = 10\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 8.5\text{ V}_{PP}$	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 3: Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C .

Note 4: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $PD = (T_{J(\text{max})} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 1.5\text{V}$ and R_L connect to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 12.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

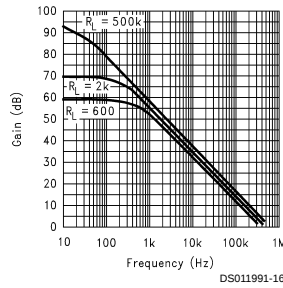
Note 8: $V^+ = 15\text{V}$. Connected as a Voltage Follower with a 10V step input. Number specified is the slower of the positive and negative slew rates. $R_L = 100\text{ k}\Omega$ connected to 7.5V . Amp excited with 1 kHz to produce $V_O = 10\text{ V}_{PP}$.

Note 9: Do not short circuit output to V^+ when V^+ is greater than 12V or reliability will be adversely affected.

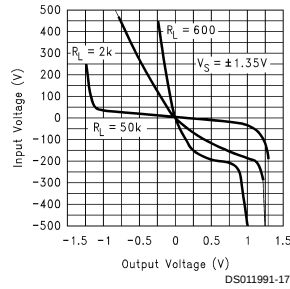
Typical Performance Characteristics $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless specified

2.7V PERFORMANCE

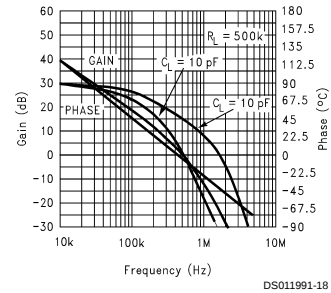
**Open Loop
Frequency Response (2.7V)**



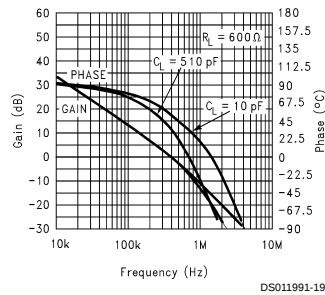
**Input Voltage vs
Output Voltage (2.7V)**



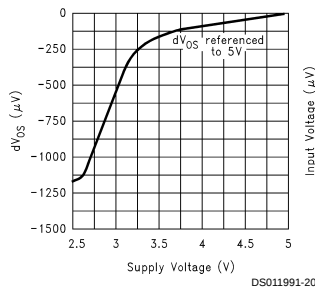
**Gain and Phase vs
Capacitance Load (2.7V)**



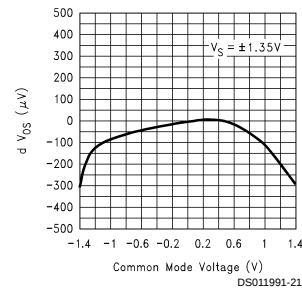
**Gain and Phase vs
Capacitance Load (2.7V)**



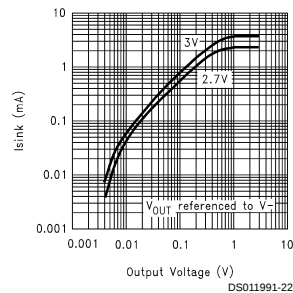
**dV_{OS} vs
Supply Voltage**



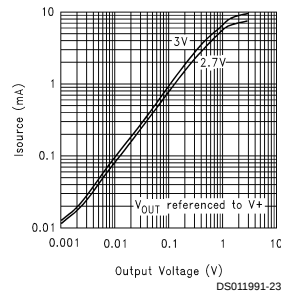
**dV_{OS} vs Common
Mode Voltage (2.7V)**



**Sinking Current vs
Output Voltage (2.7V)**



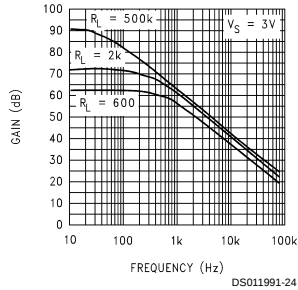
**Sourcing Current vs
Output Voltage (2.7V)**



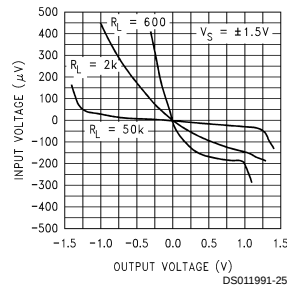
Typical Performance Characteristics Single Supply, $T_A = 25^\circ\text{C}$ unless specified

3V PERFORMANCE

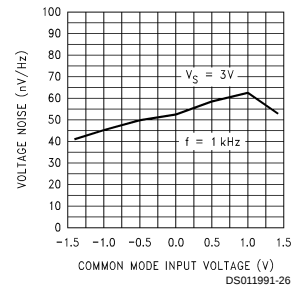
**Open Loop
Frequency Response (3V)**



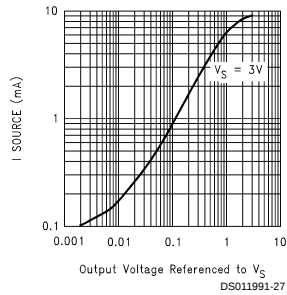
**Input Voltage vs
Output Voltage (3V)**



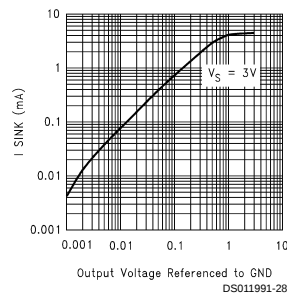
**Input Voltage Noise
vs Input Voltage (3V)**



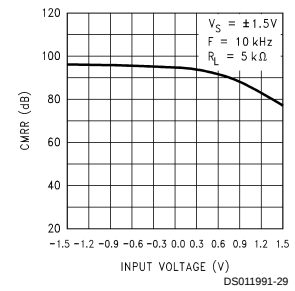
**Sourcing Current
vs Output Voltage (3V)**



**Sinking Current vs
Output Voltage (3V)**

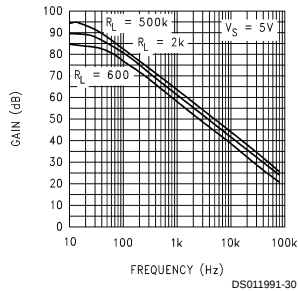


CMRR vs Input Voltage (3V)

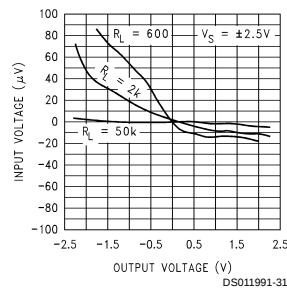


5V PERFORMANCE

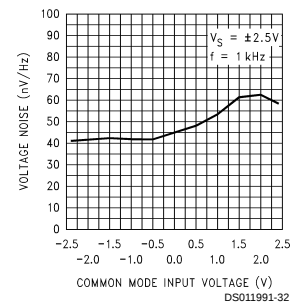
**Open Loop
Frequency Response (5V)**



**Input Voltage vs
Output Voltage (5V)**

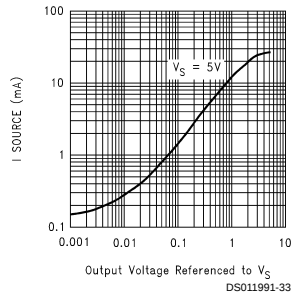


**Input Voltage Noise
vs Input Voltage (5V)**

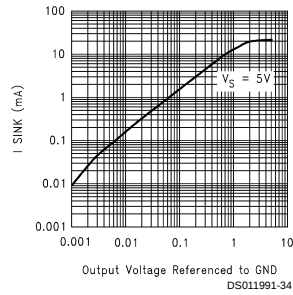


5V PERFORMANCE (Continued)

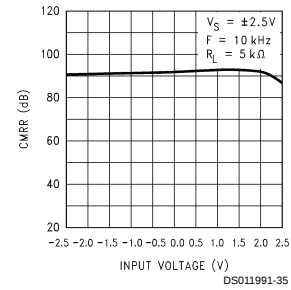
Sourcing Current vs Output Voltage (5V)



Sinking Current vs Output Voltage (5V)

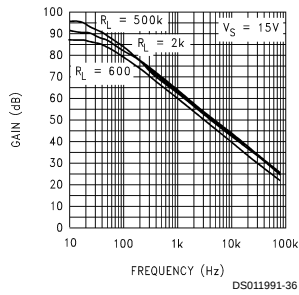


CMRR vs Input Voltage (5V)

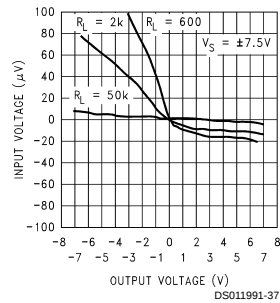


Typical Performance Characteristics $V_S = +15V$, Single Supply, $T_A = 25^\circ\text{C}$ unless specified

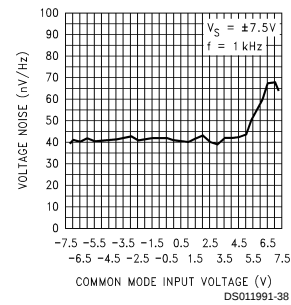
Open Loop Frequency Response (15V)



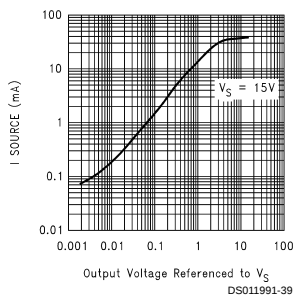
Input Voltage vs Output Voltage (15V)



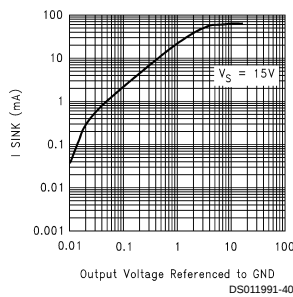
Input Voltage Noise vs Input Voltage (15V)



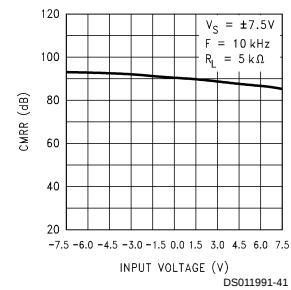
Sourcing Current vs Output Voltage (15V)



Sinking Current vs Output Voltage (15V)

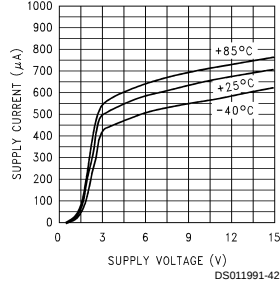


CMRR vs Input Voltage (15V)

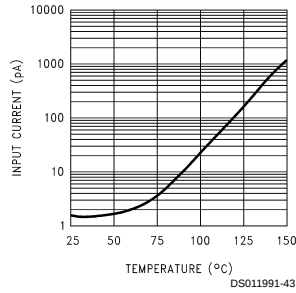


Typical Performance Characteristics $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless specified (Continued)

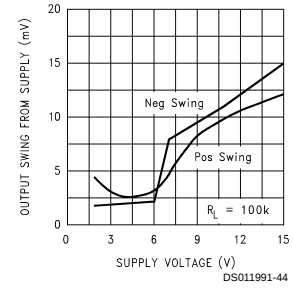
Supply Current vs Supply Voltage



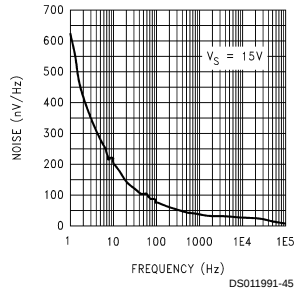
Input Current vs Temperature



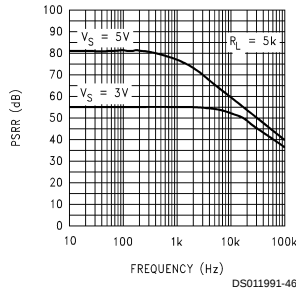
Output Voltage Swing vs Supply Voltage



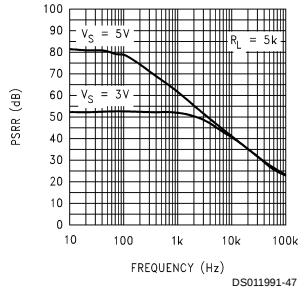
Input Voltage Noise vs Frequency



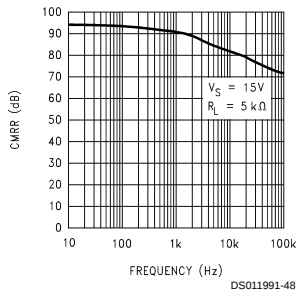
Positive PSRR vs Frequency



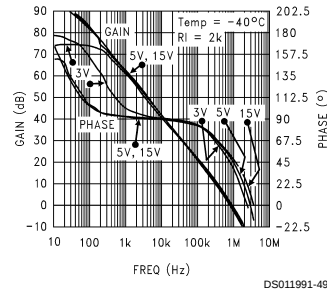
Negative PSRR vs Frequency



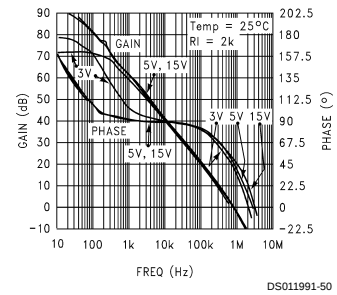
CMRR vs Frequency



Open Loop Frequency Response @ $-40^\circ C$

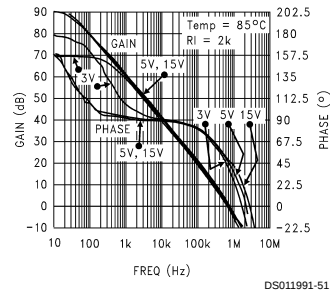


Open Loop Frequency Response @ $25^\circ C$



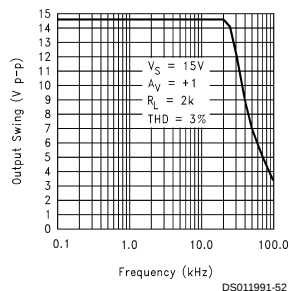
Typical Performance Characteristics $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless specified (Continued)

Open Loop Frequency Response @ $85^\circ C$



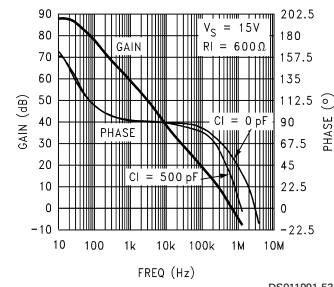
DS011991-51

Maximum Output Swing vs Frequency



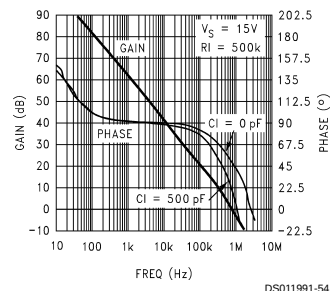
DS011991-52

Gain and Phase vs Capacitive Load



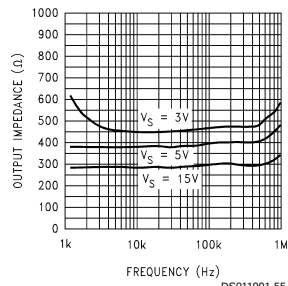
DS011991-53

Gain and Phase vs Capacitive Load



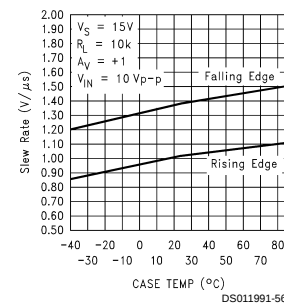
DS011991-54

Output Impedance vs Frequency



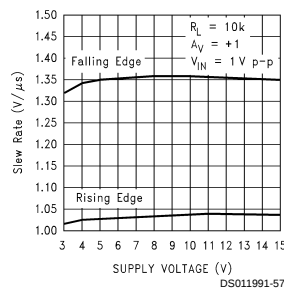
DS011991-55

Slew Rate vs Temperature



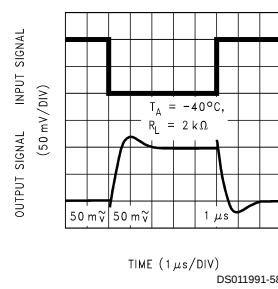
DS011991-56

Slew Rate vs Supply Voltage



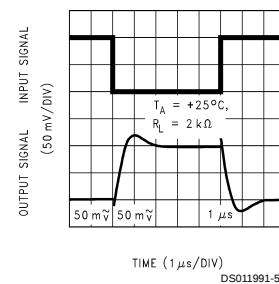
DS011991-57

Inverting Small Signal Pulse Response



DS011991-58

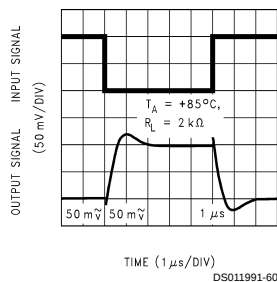
Inverting Small Signal Pulse Response



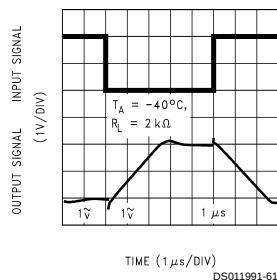
DS011991-59

Typical Performance Characteristics $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless specified (Continued)

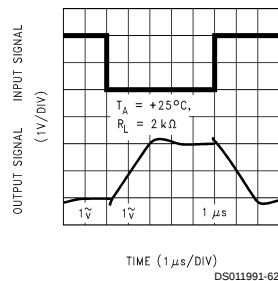
Inverting Small Signal Pulse Response



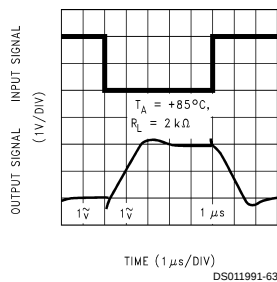
Inverting Large Signal Pulse Response



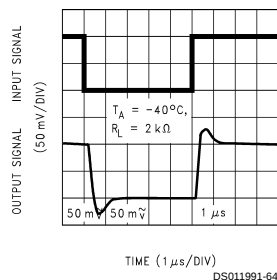
Inverting Large Signal Pulse Response



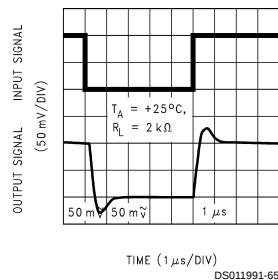
Inverting Large Signal Pulse Response



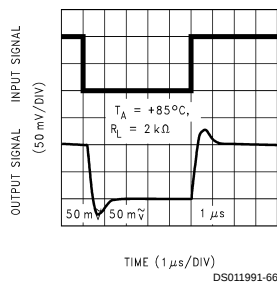
Non-Inverting Small Signal Pulse Response



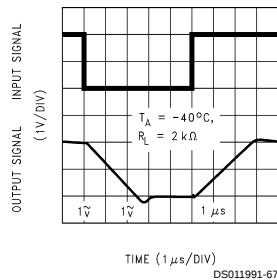
Non-Inverting Small Signal Pulse Response



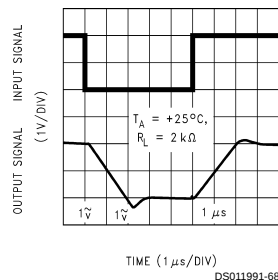
Non-Inverting Small Signal Pulse Response



Non-Inverting Large Signal Pulse Response

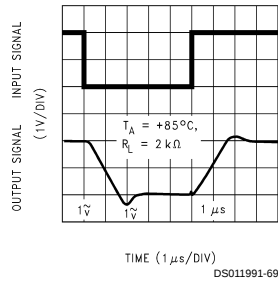


Non-Inverting Large Signal Pulse Response

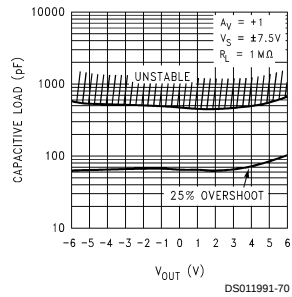


Typical Performance Characteristics $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless specified (Continued)

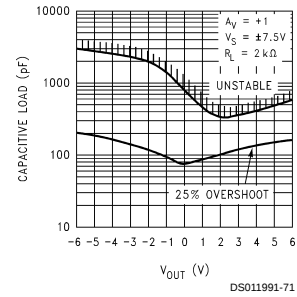
Non-Inverting Large Signal Pulse Response



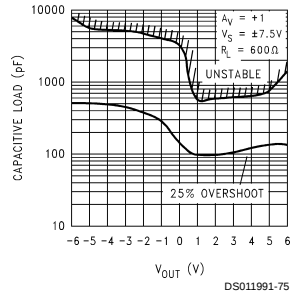
Stability vs Capacitive Load



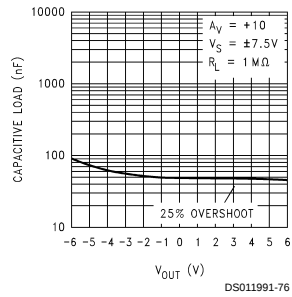
Stability vs Capacitive Load



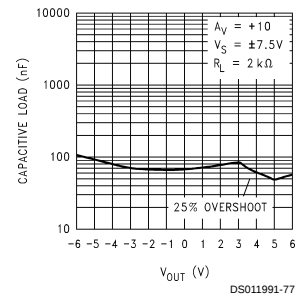
Stability vs Capacitive Load



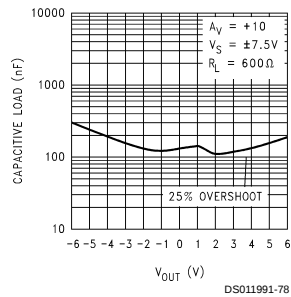
Stability vs Capacitive Load



Stability vs Capacitive Load



Stability vs Capacitive Load



4.0 Capacitive Load Tolerance

(Continued)

nation of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in *Figure 4*. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

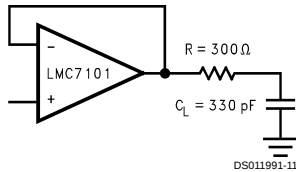


FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

5.0 Compensating for Input Capacitance when Using Large Value Feedback Resistors

When using very large value feedback resistors, (usually > 500 kΩ) the large feedback resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in *Figure 5*), C_f is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

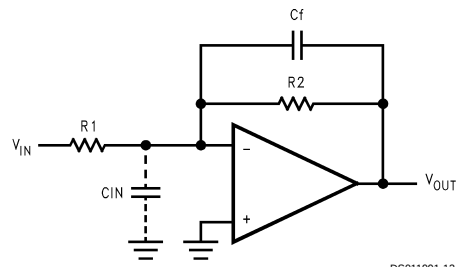


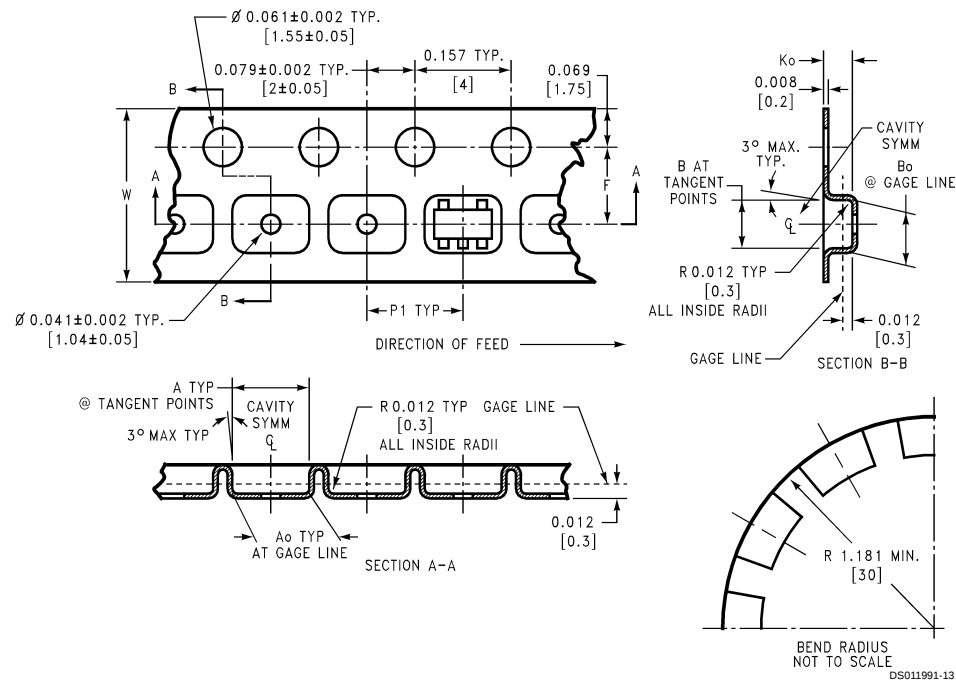
FIGURE 5. Cancelling the Effect of Input Capacitance

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

Tape Section	# Cavities	Cavity Status	Cover Tape Status
Leader (Start End)	0 (min)	Empty	Sealed
	75 (min)	Empty	Sealed
Carrier	3000	Filled	Sealed
	250	Filled	Sealed
Trailer (Hub End)	125 (min)	Empty	Sealed
	0 (min)	Empty	Sealed

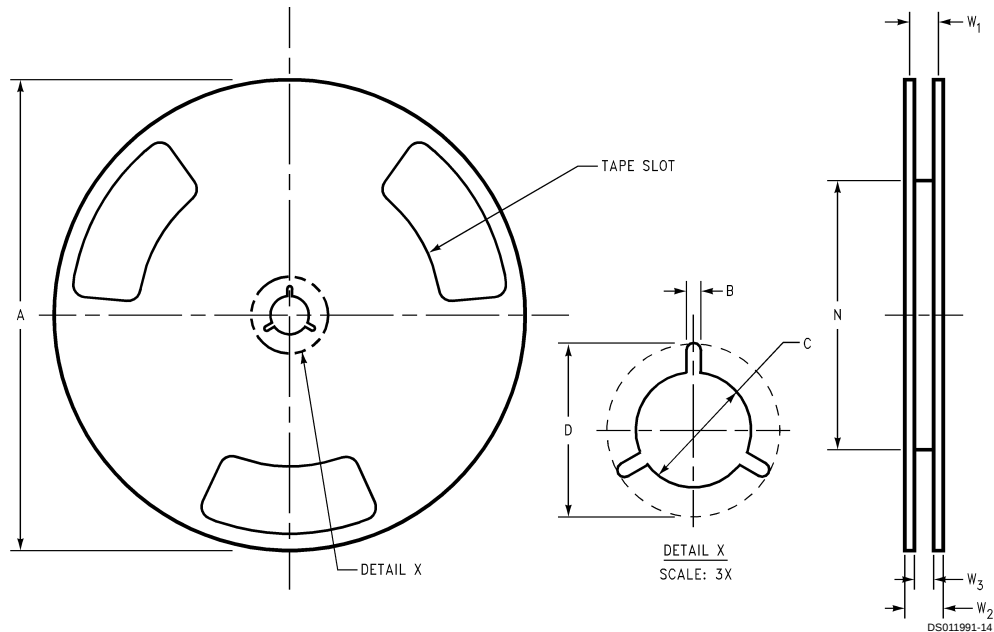
TAPE DIMENSIONS



8 mm	0.130 (3.3)	0.124 (3.15)	0.130 (3.3)	0.126 (3.2)	0.138 $\pm$ 0.002 (3.5 $\pm$ 0.05)	0.055 $\pm$ 0.004 (1.4 $\pm$ 0.11)	0.157 (4)	0.315 $\pm$ 0.012 (8 $\pm$ 0.3)
Tape Size	DIM A	DIM A _o	DIM B	DIM B _o	DIM F	DIM K _o	DIM P1	DIM W

SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS



8 mm	7.00	0.059	0.512	0.795	2.165	0.331 + 0.059/-0.000	0.567	W1 + 0.078/-0.039
	330.00	1.50	13.00	20.20	55.00	8.40 + 1.50/-0.00	14.40	W1 + 2.00/-1.00
Tape Size	A	B	C	D	N	W1	W2	W3

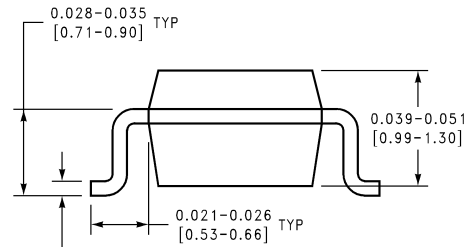
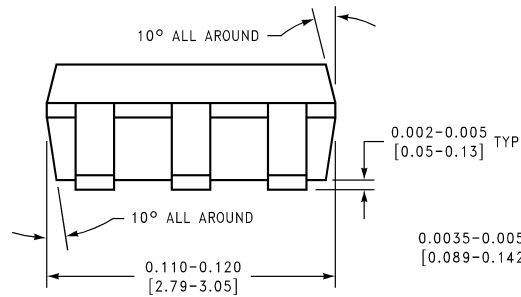
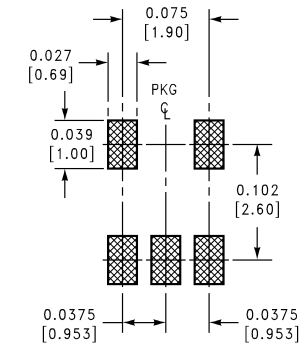
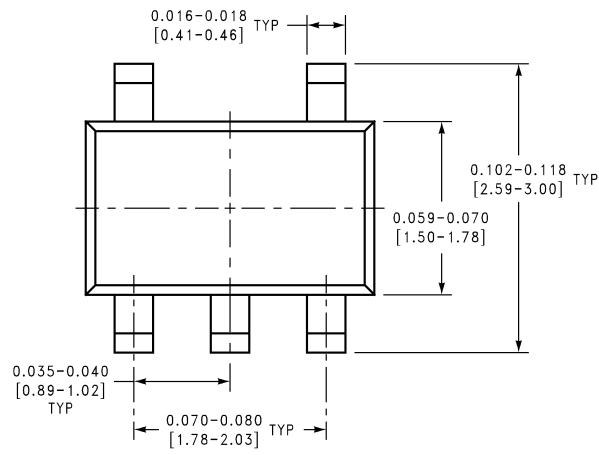
6.0 SPICE Macromodel

A SPICE macromodel is available for the LMC7101. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current

- Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Physical Dimensions inches (millimeters) unless otherwise noted



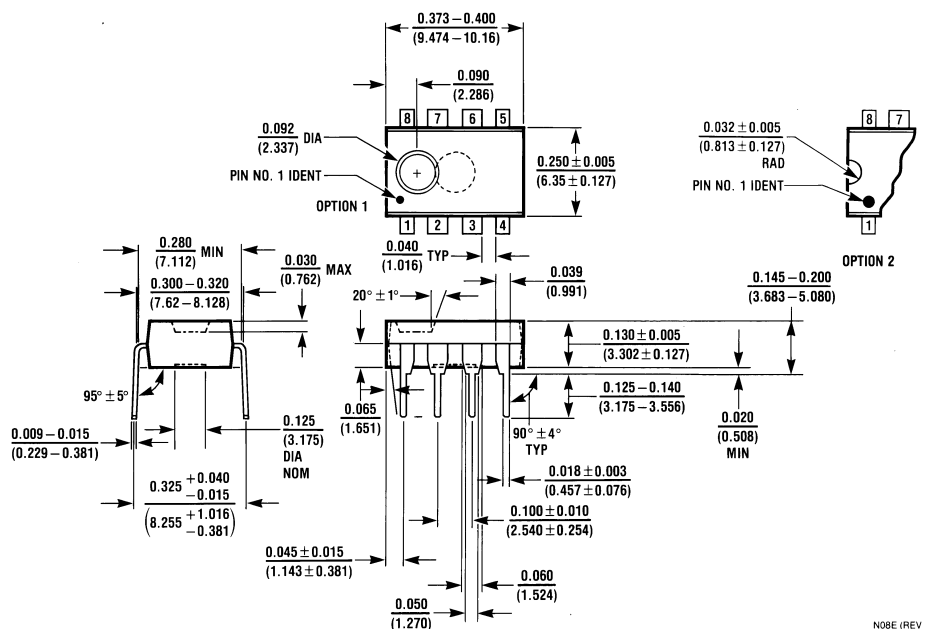
MA05A (REV D)

*Suffix indicates number of units. See Ordering Information on first page.

5-Pin SOT Package
Order Package Number LMC7101AIM5* or LMC7101BIM5*
NS Package Number MA05A

Physical Dimensions

inches (millimeters) unless otherwise noted (Continued)



8-Pin Molded DIP
8-Lead (0.300" Wide) Molded Dual-In-Line Package
Order Package Number LMC7101AIN or LMC7101BIN
NS Package Number N08E

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

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Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
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Fax: 65-2504466
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