MT92220

Carrier Class VoIP Processor

Advance Datasheet

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Introduction

The MT92220 is an assembly and disassembly engine that can convert up to 1023 full-duplex TDM voice channels to IP packets or AAL2 cells, according to the H.225 and I.363.2 standards. The device communicates via an H.1x0 TDM bus on the WAN Access side, carrying voice in plain PCM format, ADPCM or HDLC-encapsulated mini-packets.

On the Packet Switch Fabric side, the MT92220 can carry IP packets over Ethernet, ATM (using AAL5 or AAL2 cells) or Packet over SONET in a multitude of combinations. A 16 bit Intel/Motorola CPU interface is used to access and configure the device. Finally, up to 12 SRAMs and 2 SDRAMs can be used as external memory configuration and storage space.

The MT92220 offers significant savings in systems cost and system simplicity through reduced component count and simplified software. It also provides systems companies with the ability to provide a configurable solution (AAL2/AAL5/IP) for the convergence market space.

Features

General

- Up to 1023 full-duplex PCM or ADPCM voice channels over IP/UDP/RTP connections or AAL2 VC
- Up to 4096 HDLC channels carrying application data (UDP payload) converted to
- IP/UDP connections or AAL2 VC
- Simultaneous support of PCM, ADPCM and HDLC connections
- Simultaneous support of IP/UDP connections and AAL2 VC in any combination
- 16-bit Intel/Motorola CPU Interface
- Fully H.1x0 compliant TDM interface
- Network Interface A: UTOPIA Level 1/2, POS-PHY Level 2 or MII
- Network Interface B: UTOPIA Level 1
- Two to eight 18 bit data bus ZBT SSRAMs, each ranging in size from 128K to 1M bytes

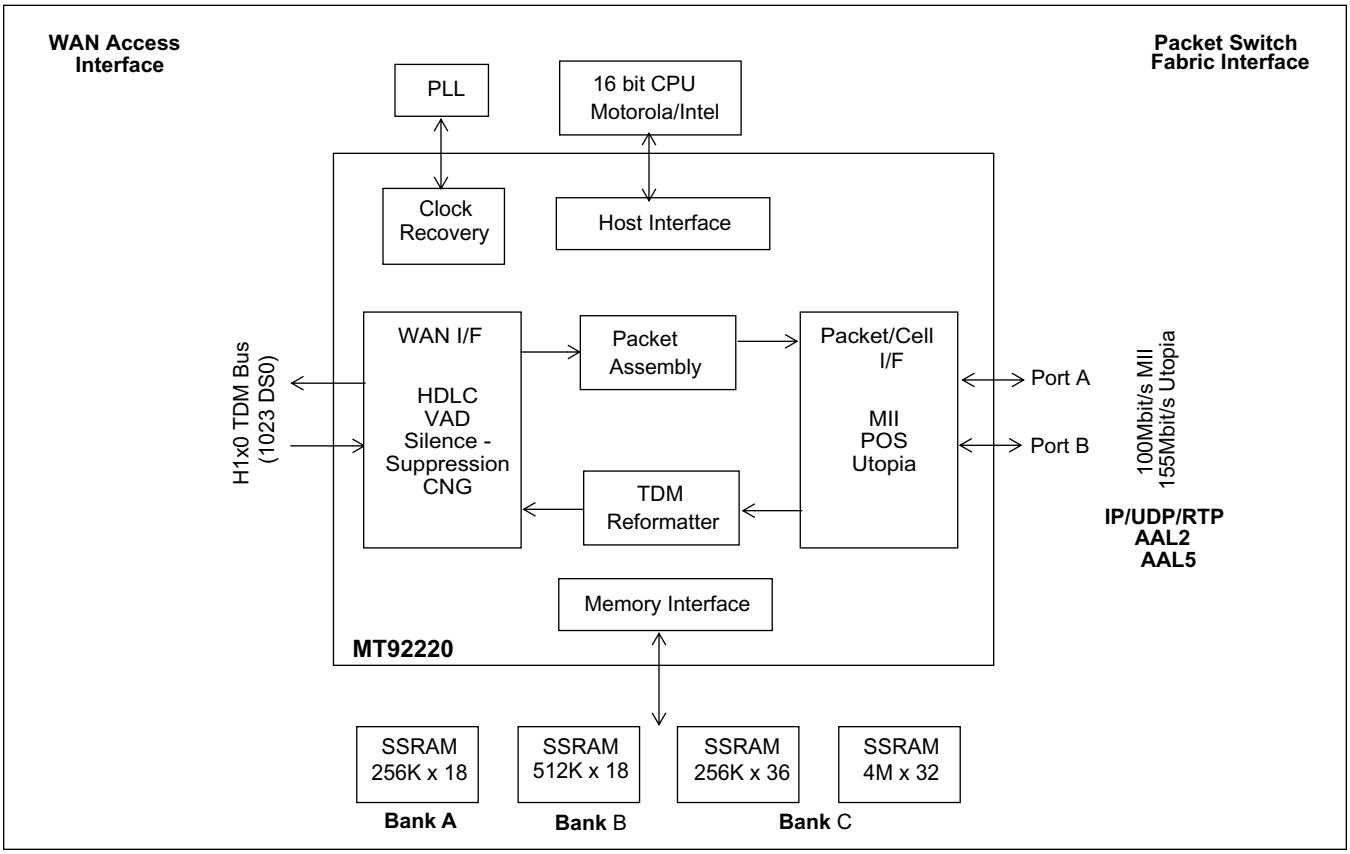

Figure 1 - MT92210 VOIP Processor

- One to four 36 bit data bus ZBT SSRAMs, each ranging in size from 128K to 1M bytes
- Two 16 bit data bus SDRAMs, each ranging in size from 8M to 16M bytes

Data Formats

- Simultaneous Support of IP version 4 and 6, and of AAL2
- Chip packages voice in RTP, UDP, and IP to support RFC791, RFC2460, RFC768, and RFC1889
- Chip packages voice in AAL2 to support I.363.2 and I.366.2
- IP packets can be sent over 3 different types of physical links (Ethernet, ATM, Packet over SONET)
- RTP packaging is optional per connection
- HDLC mini-packets are encapsulated in IP and UDP (RTP packaging performed by external processor); for AAL2 VC, AAL2 header is inserted by the MT92220 (but UUI can be inserted through HDLC control byte)
- IP/UDP layers are optional
- IP over AAL5 can be performed using Classical IP over ATM with SNAP/LLC headers or Ethernet LAN Emulation (LANE) v1 or v2
- Support of MPLS & MPOA. On reception, MPLS/MPOA labels can be used to establish data format
- Logical subnet number can be established using ATM header, MPLS flow header, MPOA tag or ELAN-ID in LANE v2 header
- Quality of service can de determined using ATM header, Ethernet user priority or IP Type Of Service (TOS)

Voice Treatment Functions

- Up to 4096 connections
- Up to 1023 PCM/ADPCM channels
- Support for up to 4096 HDLC channels distributed over 512 streams and 2046 time slots
- Up to 255 PCM/ADPCM channels per connection (using proprietary low delay encoding)
- Up to 248 voice CIDs per AAL2 VC
- One single AAL2 CID can interlace up to 64 PCM/ADPCM channels
- HDLC packets contain application data (UDP payload) converted to IP/UDP datagrams
- Packets sizes up to 1500 bytes for IP/UDP and 64 bytes for AAL2
- Support of up to 1500 TDM samples of data per packet
- Jitter Absorption Buffer size up to 8192 bytes allowing absorption of up to 512 ms of PDV
- Support for CPU-generated RTP or AAL2 packets
- Reception of CPU-destined RTP or AAL2 packets in buffers of up to 64K bytes
- Packet Delay Variation monitoring to diagnose and reduce delay
- Packet loss & misinsertion compensation for PCM and ADPCM packets
- Network jitter monitoring allows support of RTCP for PCM, ADPCM, HDLC and CPU connections
- Policing on HDLC channels and CPU channels protects against misbehaving connections
- PCM, ADPCM, HDLC and CPU mini-packets can all be transported on the same connection with chip's RTP engine to guarantee consistency among the packets

Network Functions

- IP packet identification can be performed using any combination of IP source address, IP destination address, UDP source port, UDP destination port and RTP Synchronization Source Identifier and are programmable on a per-connection basis
- Non-voice packets can be injected and received via the CPU Interface
- Non-voice packets can be injected and received via the secondary UTOPIA port
- The MT92220 can be daisy-chained to other UTOPIA devices to increase capacity
- Off-the-shelf AAL5 SAR can be used to terminate data connections on a PCI bus
- Complex priority Look-up can be performed based on IP, UDP or RTP headers
- IP, UDP and RTP header verification performed
- Full support for Silence Suppression and Padding

Silence Suppression and Padding

- Proprietary Adaptive Silence Suppression
- Supported in both PCM and ADPCM formats
- Padding with matched-energy comfort noise
- 64 tone buffers used to generate tones (1 byte to 64Kb each)
- 32 large comfort noise buffers (16Kb to 64Kb)
- Suppression indication can be generated by chip or used externally for synchronisation

H.100 Interface

- Fully H.1x0 compatible with Master and Slave capability
- Support of message channel
- Low Latency Loop-back (H.100 to H.100) of 128 channels (delay <= 375 us)
- Redundant Adaptive Clock Recovery Circuit
- Support of 2/4/8 MHz bus speed in groups of 4 streams (8 separate groups)
- Generation of H.1x0 compatibility signals

TDM data formats

- Support of plain PCM in u-law and A-law
- Translation between u-law and A-law on a per connection basis
- Support of ADPCM at 40, 32, 24 or 16 kbps
- Dual time-slot mode allows dynamic, error-free switching between PCM and ADPCM formats with silence suppression
- Support of HDLC encapsulated mini-packets with asynchronous timing
- Support of HDLC streams ranging from 1 to 2046 time slots
- Routing of HDLC streams according to HDLC address byte, with up to 512 channels per stream
- Support of HDLC packets up to 1500 bytes in length

Link Interface

- Ethernet support for MII interface
- Support for Ethernet MIB
- Packet over SONET support for 16-bit POS-PHY bus allowing interoperation with PHY at speeds up to 155 Mbps
- Support for packets of up to 1500 bytes (plus MAC header) in Ethernet and up to 65535 bytes in ATM and Packet Over SONET
- Secondary UTOPIA port can be used in all modes allowing the same data support architecture to be used independently of the link layer with minimal changes
- Pin-out allows designs that support Ethernet, ATM and Packet over SONET with only software configuration deciding on the link layer used

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