4Mb SYNCBURST™ SRAM

MT58L256L18D1, MT58L128L32D1, MT58L128L36D1

3.3V V_{DD}, 3.3V I/O, Pipelined, Double-Cycle Deselect

3.3V V_{DD}, 3.3V I/O, Pipelined, Double-Cycle Deselect

FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (V_{DD})
- Separate +3.3V isolated output buffer supply ($V_{DD}Q$)
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 165-pin FBGA package
- 100-pin TQFP package
- Low capacitive bus loading
- x18, x32, and x36 versions available

OPTIONS   MARKING

- Timing (Access/Cycle/MHz)

3.5ns/6ns/166 MHz	-6
4.0ns/7.5ns/133 MHz	-7.5
5ns/10ns/100 MHz	-10

- Configurations

256K x 18	MT58L256L18D1
128K x 32	MT58L128L32D1
128K x 36	MT58L128L36D1

- Packages

100-pin TQFP	T
165-pin FBGA	F*

- Operating Temperature Range

|	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)**	IT

Part Number Example:
MT58L256L18D1T-6

* A Part Marking Guide for the FBGA devices can be found on Micron's Web site—http://www.micron.com/support/index.html.

** Industrial temperature range offered in specific speed grades and configurations. Contact factory for more information.

100-Pin TQFP[1]

165-Pin FBGA

**NOTE:** 1. JEDEC-standard MS-026 BHA (LQFP).
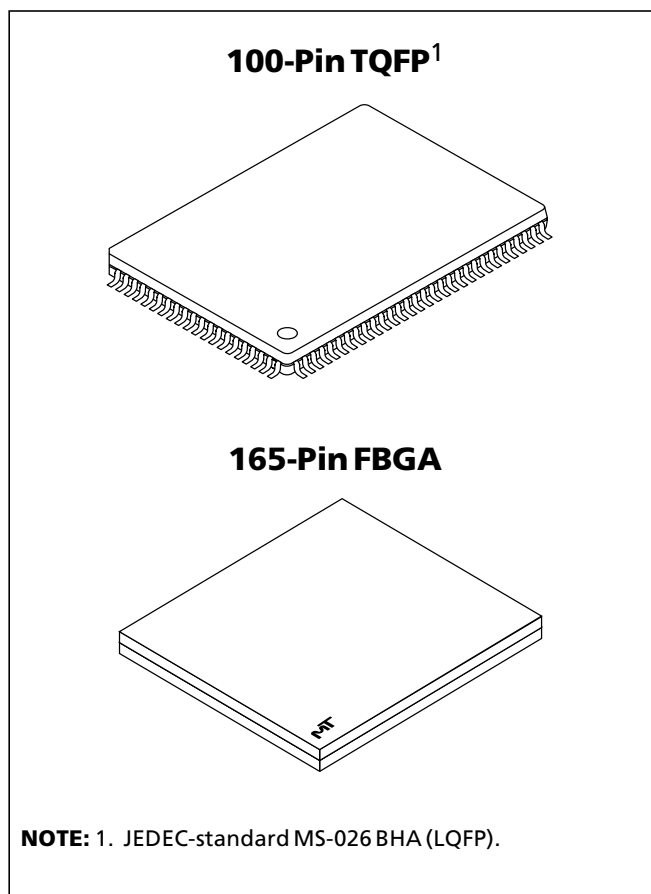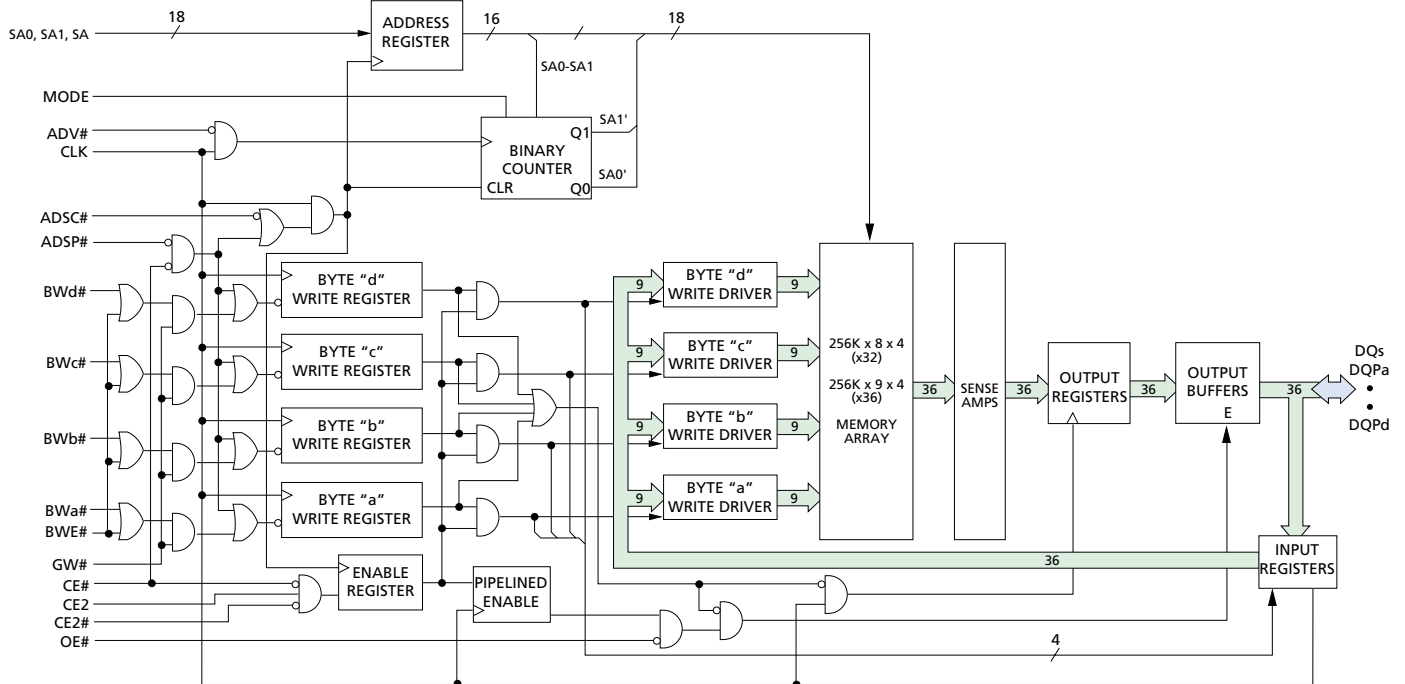
GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 4Mb SyncBurst SRAMs integrate a 256K x 18, 128K x 32, or 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

FUNCTIONAL BLOCK DIAGRAM
256K x 18
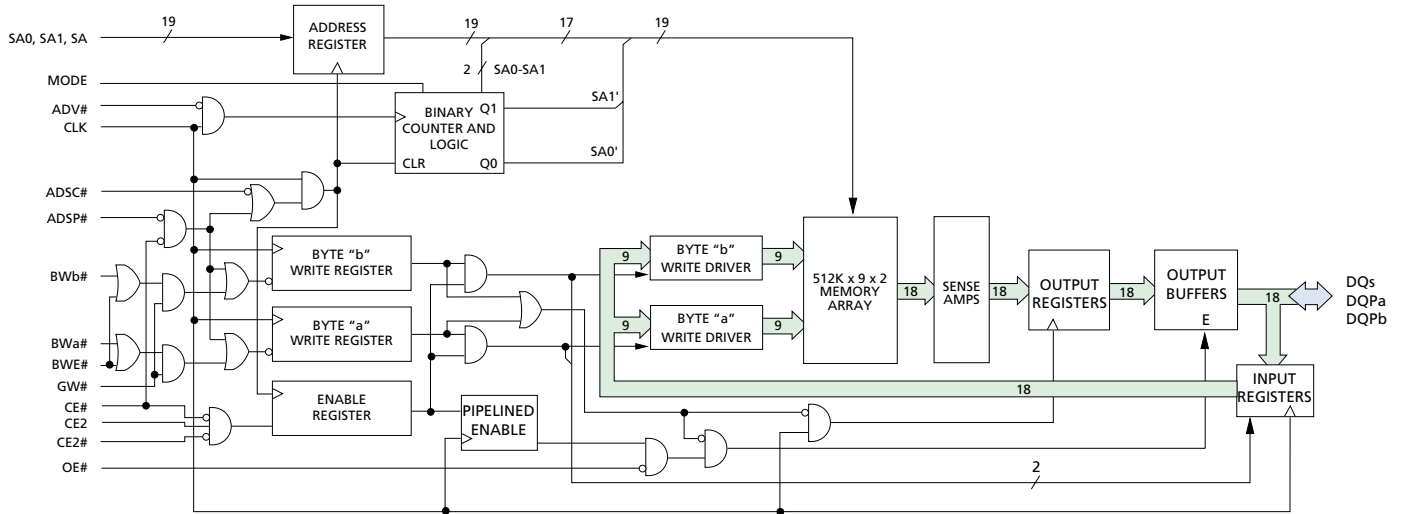
FUNCTIONAL BLOCK DIAGRAM
128K x 32/36

NOTE: Functional block diagrams illustrate simplified device operation. See truth tables, pin descriptions, and timing diagrams for detailed information.

GENERAL DESCRIPTION (continued)

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed write cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32

and x36 devices, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

This device incorporates an additional pipelined enable register which delays turning off the output buffer an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

Micron's 4Mb SyncBurst SRAMs operate from a +3.3V V_DD power supply, and all inputs and outputs are TTL-compatible. The device is ideally suited for Pentium® and PowerPC pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64-, and 72-bit-wide applications.

Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc*
2	NC	DQc
3	NC	DQc
4	VDDQ	VDDQ
5	Vss	Vss
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	Vss	Vss
11	VDDQ	VDDQ
12	DQb	DQc
13	DQb	DQc
14	VDD	VDD
15	VDD	VDD
16	NC	NC
17	Vss	Vss
18	DQb	DQd
19	DQb	DQd
20	VDDQ	VDDQ
21	Vss	Vss
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd

PIN #	x18	x32/x36
26	Vss	Vss
27	VDDQ	VDDQ
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	MODE
32	SA	SA
33	SA	SA
34	SA	SA
35	SA	SA
36	SA1	SA1
37	SA0	SA0
38	DNU	DNU
39	DNU	DNU
40	Vss	Vss
41	VDD	VDD
42	NF**	NF**
43	NF**	NF**
44	SA	SA
45	SA	SA
46	SA	SA
47	SA	SA
48	SA	SA
49	SA	SA
50	SA	SA

PIN #	x18	x32/x36
51	NC	NC/DQPa*
52	NC	DQa
53	NC	DQa
54	VDDQ	VDDQ
55	Vss	Vss
56	NC	DQa
57	NC	DQa
58	DQa	DQa
59	DQa	DQa
60	Vss	Vss
61	VDDQ	VDDQ
62	DQa	DQa
63	DQa	DQa
64	ZZ	ZZ
65	VDD	VDD
66	NC	NC
67	Vss	Vss
68	DQa	DQb
69	DQa	DQb
70	VDDQ	VDDQ
71	Vss	Vss
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb

PIN #	x18	x32/x36
76	Vss	Vss
77	VDDQ	VDDQ
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb*
81	SA	SA
82	SA	SA
83	ADV#	ADV#
84	ADSP#	ADSP#
85	ADSC#	ADSC#
86	OE#	OE#
87	BWE#	BWE#
88	GW#	GW#
89	CLK	CLK
90	Vss	Vss
91	VDD	VDD
92	CE2#	CE2#
93	BWa#	BWa#
94	BWb#	BWb#
95	NC	BWc#
96	NC	BWd#
97	CE2	CE2
98	CE#	CE#
99	SA	SA
100	SA	SA

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

**Pins 43 and 42 are reserved for address expansion, 8Mb and 16Mb respectively.

PIN ASSIGNMENT (TOP VIEW)
100-PIN TQFP

x18

Top row (pins 80–51): SA, NC, NC, VDDQ, Vss, NC, DQPa, DQa, DQa, Vss, VDDQ, DQa, DQa, Vss, NC, NC, VDD, ZZ, DQa, DQa, VDDQ, Vss, DQa, DQa, NC, NC, Vss, VDDQ, NC, NC

Left side:
- 81 SA
- 82 SA
- 83 ADV#
- 84 ADSP#
- 85 ADSC#
- 86 OE#
- 87 BWE#
- 88 GW#
- 89 CLK
- 90 Vss
- 91 VDD
- 92 CE2#
- 93 BWa#
- 94 BWb#
- 95 NC
- 96 NC
- 97 CE2
- 98 CE#
- 99 SA
- 100 SA

Right side:
- 50 SA
- 49 SA
- 48 SA
- 47 SA
- 46 SA
- 45 SA
- 44 SA
- 43 NF**
- 42 NF**
- 41 VDD
- 40 Vss
- 39 DNU
- 38 DNU
- 37 SA0
- 36 SA1
- 35 SA
- 34 SA
- 33 SA
- 32 SA
- 31 MODE

Bottom row (pins 1–30): NC, NC, NC, VDDQ, Vss, NC, NC, DQb, DQb, Vss, VDDQ, DQb, DQb, VDD, VDD, NC, Vss, DQb, DQb, VDDQ, Vss, DQb, DQb, DQPb, NC, NC, Vss, VDDQ, NC, NC

x32/x36

Top row (pins 80–51): NC/DQPb*, DQb, DQb, VDDQ, Vss, DQb, DQb, DQb, DQb, Vss, VDDQ, DQb, DQb, Vss, NC, VDD, ZZ, DQa, DQa, VDDQ, Vss, DQa, DQa, DQa, DQa, Vss, VDDQ, DQa, NC/DQPa*

Left side:
- 81 SA
- 82 SA
- 83 ADV#
- 84 ADSP#
- 85 ADSC#
- 86 OE#
- 87 BWE#
- 88 GW#
- 89 CLK
- 90 Vss
- 91 VDD
- 92 CE2#
- 93 BWa#
- 94 BWb#
- 95 BWc#
- 96 BWd#
- 97 CE2
- 98 CE#
- 99 SA
- 100 SA

Right side:
- 50 SA
- 49 SA
- 48 SA
- 47 SA
- 46 SA
- 45 SA
- 44 SA
- 43 NF**
- 42 NF**
- 41 VDD
- 40 Vss
- 39 DNU
- 38 DNU
- 37 SA0
- 36 SA1
- 35 SA
- 34 SA
- 33 SA
- 32 SA
- 31 MODE

Bottom row (pins 1–30): NC/DQPc*, DQc, DQc, VDDQ, Vss, DQc, DQc, DQc, DQc, Vss, VDDQ, DQc, DQc, VDD, NC, Vss, DQd, DQd, VDDQ, Vss, DQd, DQd, DQd, DQd, Vss, VDDQ, DQd, DQd, NC/DQPd*

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.
**Pins 43 and 42 are reserved for address expansion, 8Mb and 16Mb respectively.

TQFP PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-50, 80-82, 99, 100	37 36 32-35, 44-50, 81, 82, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93 94 – –	93 94 95 96	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. For the x32 and x36 versions, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; BWd# controls DQd pins and DQPd. Parity is only available on the x18 and x36 versions.
87	87	BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
88	88	GW#	Input	Global Write: This active LOW input allows a full 18-, 32- or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
86	86	OE#	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
83	83	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.

(continued on next page)

TQFP PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
84	84	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
85	85	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
31	31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating.
(a) 58, 59, 62, 63, 68, 69, 72, 73 (b) 8, 9, 12, 13, 18, 19, 22, 23	(a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/Output	SRAM Data I/Os: For the x18 version, Byte "a" is DQa pins; Byte "b" is DQb pins. For the x32 and x36 versions, Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
74 24 – –	51 80 1 30	NC/DQPa NC/DQPb NC/DQPc NC/DQPd	NC/I/O	No Connect/Parity Data I/Os: On the x32 version, these pins are No Connect (NC). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd.
14, 15, 41, 65, 91	14, 15, 41, 65, 91	VDD	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	VDDQ	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	VSS	Supply	Ground: GND.
38, 39	38, 39	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1-3, 6, 7, 16, 25, 28-30, 51-53, 56, 57, 66, 75, 78, 79, 95, 96	16, 66	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation.
42, 43	42, 43	NF	–	No Function: These pins are internally connected to the die and will have the capacitance of input pins. It is allowable to leave these pins unconnected or driven by signals. Reserved for address expansion, pin 43 becomes an SA at 8Mb density and pin 42 becomes an SA at 16Mb density.

PIN LAYOUT (TOP VIEW)
165-PIN FBGA

x18

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWb#	NC	CE2#	BWE#	ADSC#	ADV#	SA	SA
B	NC	SA	CE2	NC	BWa#	CLK	GW#	OE# (G#)	ADSP#	SA	NC
C	NC	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
H	VDD	Vss	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	Vss	NC	NC	Vss	Vss	VDDQ	NC	NC
P	NC	NC	SA	SA	DNU	SA1	DNU	SA	SA	SA	NC
R	MODE (LBO#)	NC	SA	SA	DNU	SA0	DNU	SA	SA	SA	SA

TOP VIEW

x32/x36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	SA	CE#	BWc#	BWb#	CE2#	BWE#	ADSC#	ADV#	SA	NC
B	NC	SA	CE2	BWd#	BWa#	CLK	GW#	OE# (G#)	ADSP#	SA	NC
C	NC/DQPc	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	NC/DQPb
D	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQb	DQb
H	VDD	Vss	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	DQa
N	NC/DQPd	NC	VDDQ	Vss	NC	NC	Vss	Vss	VDDQ	NC	NC/DQPa
P	NC	NC	SA	SA	DNU	SA1	DNU	SA	SA	SA	NC
R	MODE (LBO#)	NC	SA	SA	DNU	SA0	DNU	SA	SA	SA	SA

TOP VIEW

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.
NOTE: Pins 11P, and 6N reserved for address pin expansion; 8Mb, and 16Mb respectively.

FBGA PIN DESCRIPTIONS

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
6R 6P 2A, 2B, 3P, 3R, 4P, 4R, 8P, 8R, 9P, 9R, 10A, 10B, 10P, 10R, 11A, 11R	6R 6P 2A, 2B, 3P, 3R, 4P, 4R, 8P, 8R, 9P, 9R, 10A, 10B, 10P, 10R, 11R	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5B 4A – –	5B 5A 4A 4B	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQas and DQPa; BWb# controls DQbs and DQPb. For the x32 and x36 versions, BWa# controls DQas and DQPa; BWb# controls DQbs and DQPb; BWc# controls DQcs and DQPc; BWd# controls DQds and DQPd. Parity is only available on the x18 and x36 versions.
7A	7A	BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
7B	7B	GW#	Input	Global Write: This active LOW input allows a full 18-, 32-, or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
6B	6B	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
3A	3A	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
6A	6A	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
11H	11H	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
3B	3B	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
8B	8B	OE#(G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
9A	9A	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on ADV# effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.

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FBGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
9B	9B	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
8A	8A	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
1R	1R	MODE (LB0#)	Input	Mode: This input selects the burst sequence. A LOW on this input selects "linear burst." NC or HIGH on this input selects "interleaved burst." Do not alter input state while device is operating.
(a) 10J, 10K, 10L, 10M, 11D, 11E, 11F, 11G (b) 1J, 1K, 1L, 1M, 2D, 2E, 2F, 2G	(a) 10J, 10K, 10L, 10M, 11J, 11K, 11L, 11M (b) 10D, 10E, 10F, 10G, 11D, 11E, 11F, 11G (c) 1D, 1E, 1F, 1G, 2D, 2E, 2F, 2G (d) 1J, 1K, 1L, 1M, 2J, 2K, 2L, 2M	DQa DQb DQc DQd	Input/Output	SRAM Data I/Os: For the x18 version, Byte "a" is associated DQas; Byte "b" is associated with DQbs. For the x32 and x36 versions, Byte "a" is associated with DQas; Byte "b" is associated with DQbs; Byte "c" is associated with DQcs; Byte "d" is associated with DQds. Input data must meet setup and hold times around the rising edge of CLK.
11C 1N – –	11N 11C 1C 1N	NC/DQPa NC/DQPb NC/DQPc NC/DQPd	NC/I/O	No Connect/Parity Data I/Os: On the x32 version, these are No Connect (NC). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPc; Byte "d" parity is DQPd.
1H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	1H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	V$_{DD}$	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	V$_{DDQ}$	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.

(continued on next page)

FBGA PIN DESCRIPTIONS (continued)

x18	x32/x36	SYMBOL	TYPE	DESCRIPTION
2H, 4C, 4N, 5C, 5D, 5E 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 7N, 8C, 8N	2H, 4C, 4N, 5C, 5D, 5E 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 7N, 8C, 8N	V_{SS}	Supply	Ground: GND.
5P, 5R, 7P, 7R	5P, 5R, 7P, 7R	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1A, 1B, 1C, 1D, 1E, 1F, 1G, 1P, 2C, 2J, 2K, 2L, 2M, 2N, 2P, 2R, 3H, 4B, 5A, 5N, 6N, 9H, 10C, 10D, 10E, 10F, 10G, 10H, 10N, 11B, 11J, 11K, 11L, 11M, 11N, 11P	1A, 1B, 1P, 2C, 2N, 2P, 2R, 3H, 5N, 6N, 9H, 10C, 10H, 10N, 11A, 11B, 11P	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation. Pins 11P, and 6N reserved for address pin expansion; 8Mb, and 16Mb respectively.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x18)

FUNCTION	GW#	BWE#	BWa#	BWb#
READ	H	H	X	X
READ	H	L	H	H
WRITE Byte "a"	H	L	L	H
WRITE Byte "b"	H	L	H	L
WRITE All Bytes	H	L	L	L
WRITE All Bytes	L	X	X	X

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x32/x36)

FUNCTION	GW#	BWE#	BWa#	BWb#	BWc#	BWd#
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte "a"	H	L	L	H	H	H
WRITE All Bytes	H	L	L	L	L	L
WRITE All Bytes	L	X	X	X	X	X

NOTE: Using BWE# and BWa# through BWd#, any one or more bytes may be written.

TRUTH TABLE

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
DESELECTE Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
DESELECTE Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
DESELECTE Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
DESELECTE Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
DESELECTE Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:
1. X means "Don't Care." # means active LOW. H means logic HIGH. L means logic LOW.
2. For WRITE#, L means any one or more byte write enable signals (BWa#, BWb#, BWc# or BWd#) and BWE# are LOW or GW# is LOW. WRITE# = H for all BWx#, BWE#, GW# HIGH.
3. BWa# enables WRITEs to DQas and DQPa. BWb# enables WRITEs to DQbs and DQPb. BWc# enables WRITEs to DQcs and DQPc. BWd# enables WRITEs to DQds and DQPd. DQPa and DQPb are only available on the x18 and x36 versions. DQPc and DQPd are only available on the x36 version.
4. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, OE# must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP# LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GW# LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
    Relative to V_{SS} .... -0.5V to +4.6V
Voltage on $V_{DD}Q$ Supply
    Relative to V_{SS} .... -0.5V to +4.6V
V_{IN} .... -0.5V to $V_{DD}Q$ + 0.5V
Storage Temperature (plastic) .... -55°C to +150°C
Junction Temperature** .... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$; V_{DD}, $V_{DD}Q$ = +3.3V +0.3V/-0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{DD}$	IL_I	-1.0	1.0	µA	3
Output Leakage Current	Output(s) disabled, $0V \leq V_{IN} \leq V_{DD}$	IL_O	-1.0	1.0	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4	–	V	1, 4
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}	–	0.4	V	1, 4
Supply Voltage		V_{DD}	3.135	3.6	V	1
Isolated Output Buffer Supply		$V_{DD}Q$	3.135	3.6	V	1, 5

NOTE: 1. All voltages referenced to V_{SS} (GND).
      2. Overshoot: $V_{IH} \leq$ +4.6V for t $\leq$ $^tKC/2$ for I $\leq$ 20mA
         Undershoot: $V_{IL} \geq$ -0.7V for t $\leq$ $^tKC/2$ for I $\leq$ 20mA
         Power-up: $V_{IH} \leq$ +3.6V and $V_{DD} \leq$ 3.135V for t $\leq$ 200ms
      3. MODE pin has an internal pull-up, and input leakage = ±10µA.
      4. The load used for V_{OH}, V_{OL} testing is shown in Figure 2. AC load current is higher than the stated DC values. AC I/O curves are available upon request.
      5. $V_{DD}Q$ should never exceed V_{DD}. V_{DD} and $V_{DD}Q$ can be connected together.

TQFP CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T_A = 25°C; f = 1 MHz; V_{DD} = 3.3V	C_I	3	4	pF	1
Input/Output Capacitance (DQ)		C_O	4	5	pF	1
Address Capacitance		C_A	3	3.5	pF	1
Clock Capacitance		C_{CK}	3	3.5	pF	1

FBGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	2.5	3.5	pF	1, 2
Output Capacitance (Q)		C_O	4	5	pF	1, 2
Clock Capacitance		C_{CK}	2.5	3.5	pF	1, 2

NOTE: 1. This parameter is sampled.
2. Preliminary package data.

I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(0°C ≤ T_A ≤ +70°C; V_{DD}, $V_{DD}Q$ = +3.3V +0.3V/-0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYM	TYP	MAX -6	MAX -7.5	MAX -10	UNITS	NOTES
Power Supply Current: Operating	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKC (MIN); V_{DD} = MAX; Outputs open	I_{DD}	225	475	375	300	mA	1, 2, 3
Power Supply Current: Idle	Device selected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{DD1}	55	110	90	85	mA	1, 2, 3
CMOS Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; All inputs static; CLK frequency = 0	I_{SB2}	0.4	10	10	10	mA	2, 3
TTL Standby	Device deselected; V_{DD} = MAX; All inputs ≤ V_{IL} or ≥ V_{IH}; All inputs static; CLK frequency = 0	I_{SB3}	8	25	25	25	mA	2, 3
Clock Running	Device deselected; V_{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V_{IH}; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; Cycle time ≥ ^tKC (MIN)	I_{SB4}	55	110	90	85	mA	2, 3

NOTE: 1. I_{DD} is specified with no output current and increases with faster cycle times. $I_{DD}Q$ increases with faster cycle times and greater output loading.
2. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
3. Typical values are measured at 3.3V, 25°C and 10ns cycle time.

TQFP THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	46	°C/W	1
Thermal Resistance (Junction to Top of Case)		θ_{JC}	2.8	°C/W	1

FBGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	θ_{JA}	40	°C/W	1, 2
Junction to Case (Top)		θ_{JC}	9	°C/W	1, 2
Junction to Pins (Bottom)		θ_{JB}	17	°C/W	1, 2

NOTE: 1. This parameter is sampled.
2. Preliminary package data.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 1) (0°C ≤ T$_A$ ≤ +70°C; V$_{DD}$, V$_{DDQ}$ = +3.3V +0.3V/-0.165V unless otherwise noted)

DESCRIPTION	SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS	NOTES
Clock									
Clock cycle time	^{t}KC	6.0		7.5		10		ns	
Clock frequency	^{f}KF		166		133		100	MHz	
Clock HIGH time	^{t}KH	2.3		2.5		3.0		ns	2
Clock LOW time	^{t}KL	2.3		2.5		3.0		ns	2
Output Times									
Clock to output valid	^{t}KQ		3.5		4.0		5.0	ns	
Clock to output invalid	^{t}KQX	1.5		1.5		1.5		ns	3
Clock to output in Low-Z	^{t}KQLZ	0		0		1.5		ns	3, 4, 5, 6
Clock to output in High-Z	^{t}KQHZ		3.5		4.2		5.0	ns	3, 4, 5, 6
OE# to output valid	^{t}OEQ		3.5		4.2		5.0	ns	7
OE# to output in Low-Z	^{t}OELZ	0		0		0		ns	3, 4, 5, 6
OE# to output in High-Z	^{t}OEHZ		3.5		4.2		4.5	ns	3, 4, 5, 6
Setup Times									
Address	^{t}AS	1.5		1.5		2.0		ns	8, 9
Address status (ADSC#, ADSP#)	^{t}ADSS	1.5		1.5		2.0		ns	8, 9
Address advance (ADV#)	^{t}AAS	1.5		1.5		2.0		ns	8, 9
Write signals (BWa#-BWd#, BWE#, GW#)	^{t}WS	1.5		1.5		2.0		ns	8, 9
Data-in	^{t}DS	1.5		1.5		2.0		ns	8, 9
Chip enables (CE#, CE2#, CE2)	^{t}CES	1.5		1.5		2.0		ns	8, 9
Hold Times									
Address	^{t}AH	0.5		0.5		0.5		ns	8, 9
Address status (ADSC#, ADSP#)	^{t}ADSH	0.5		0.5		0.5		ns	8, 9
Address advance (ADV#)	^{t}AAH	0.5		0.5		0.5		ns	8, 9
Write signals (BWa#-BWd#, BWE#, GW#)	^{t}WH	0.5		0.5		0.5		ns	8, 9
Data-in	^{t}DH	0.5		0.5		0.5		ns	8, 9
Chip enables (CE#, CE2#, CE2)	^{t}CEH	0.5		0.5		0.5		ns	8, 9

NOTE: 1. Test conditions as specified with the output loading shown in Figure 1 unless otherwise noted.
2. Measured as HIGH above V$_{IH}$ and LOW below V$_{IL}$.
3. This parameter is measured with the output loading shown in Figure 2 unless otherwise noted.
4. This parameter is sampled.
5. Transition is measured ±500mV from steady state voltage.
6. Refer to Technical Note TN-58-09, "Synchronous SRAM Bus Contention Design Considerations," for a more thorough discussion on these parameters.
7. OE# is a "Don't Care" when a byte write enable is sampled LOW.
8. A WRITE cycle is defined by at least one byte write enable LOW and ADSP# HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ADSC# or ADV# LOW or ADSP# LOW for the required setup and hold times.
9. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP# or ADSC# is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP# or ADSC# is LOW to remain enabled.

AC TEST CONDITIONS

Input pulse levels .... V_{IH} = (V_{DD}/2.2) + 1.5V

.... V_{IL} = (V_{DD}/2.2) - 1.5V

Input rise and fall times 1ns

Input timing reference levels .... V_{DD}/2.2

Output reference levels .... $V_{DD}Q$/2.2

Output load .... See Figures 1 and 2
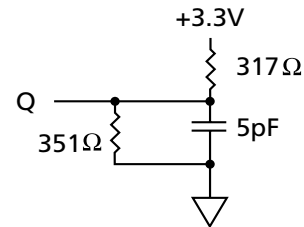
LOAD DERATING CURVES

Micron 256K x 18, 128K x 32, and 128K x 36 SyncBurst SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

Output Load Equivalents
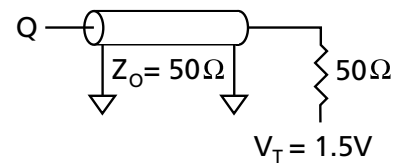
Figure 1

Figure 2

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time ZZ is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When ZZ becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time ^tZZ is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

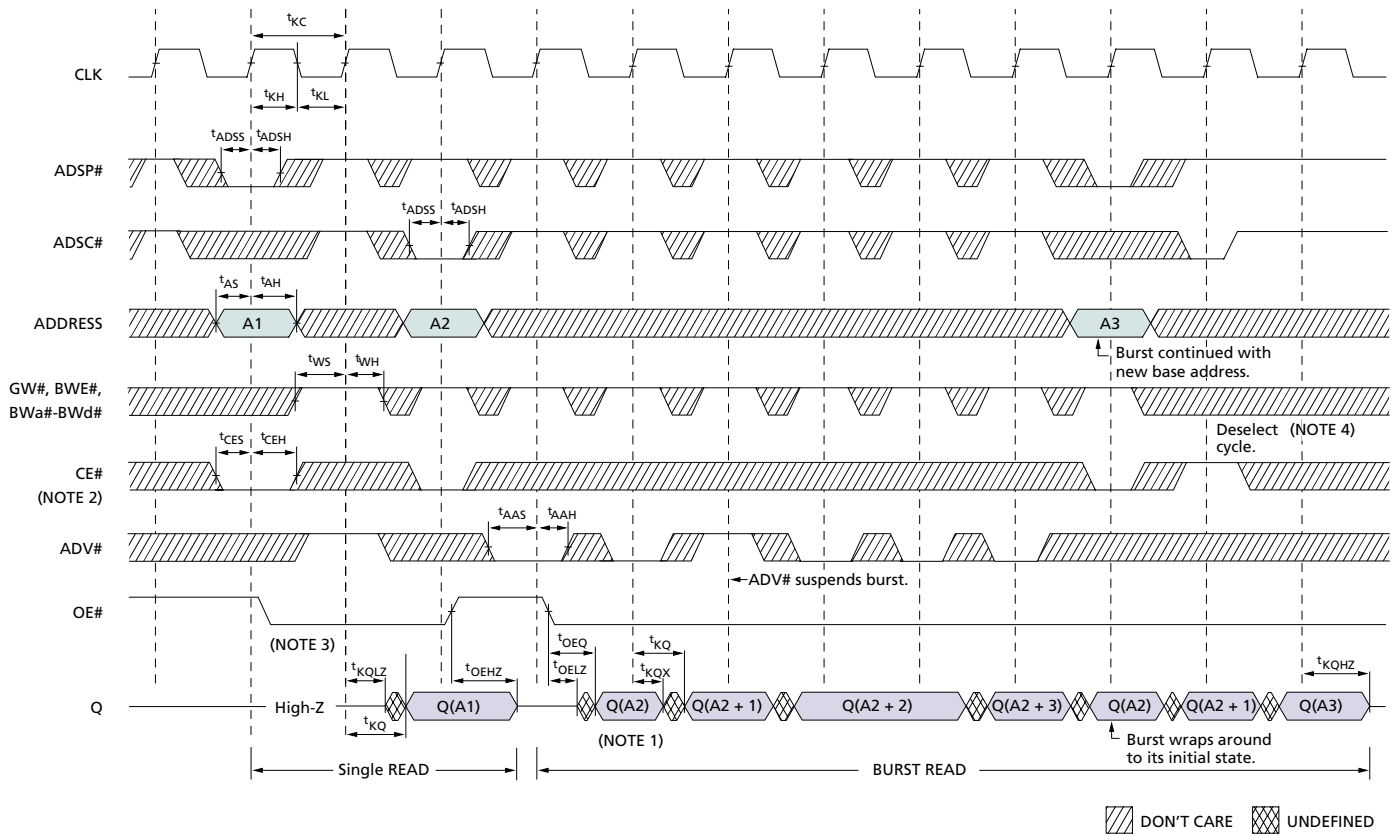| DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{SB2Z}		10	mA	
ZZ active to input ignored		^tZZ		$2(^tKC)$	ns	1
ZZ inactive to input sampled		^tRZZ	$2(^tKC)$		ns	1
ZZ active to snooze current		^tZZI		$2(^tKC)$	ns	1
ZZ inactive to exit snooze current		^tRZZI	0		ns	1

NOTE: 1. This parameter is sampled.

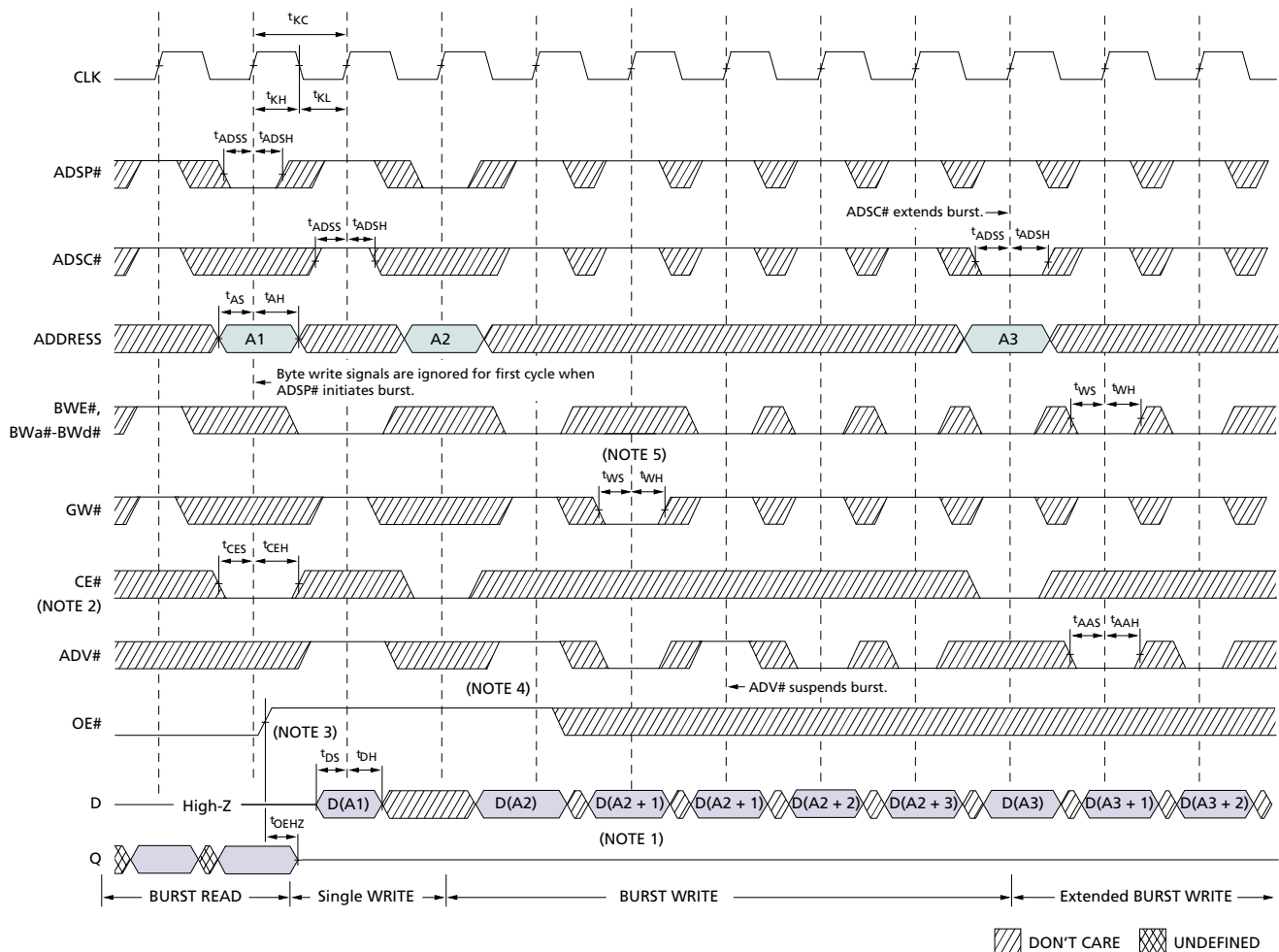## SNOOZE MODE WAVEFORM
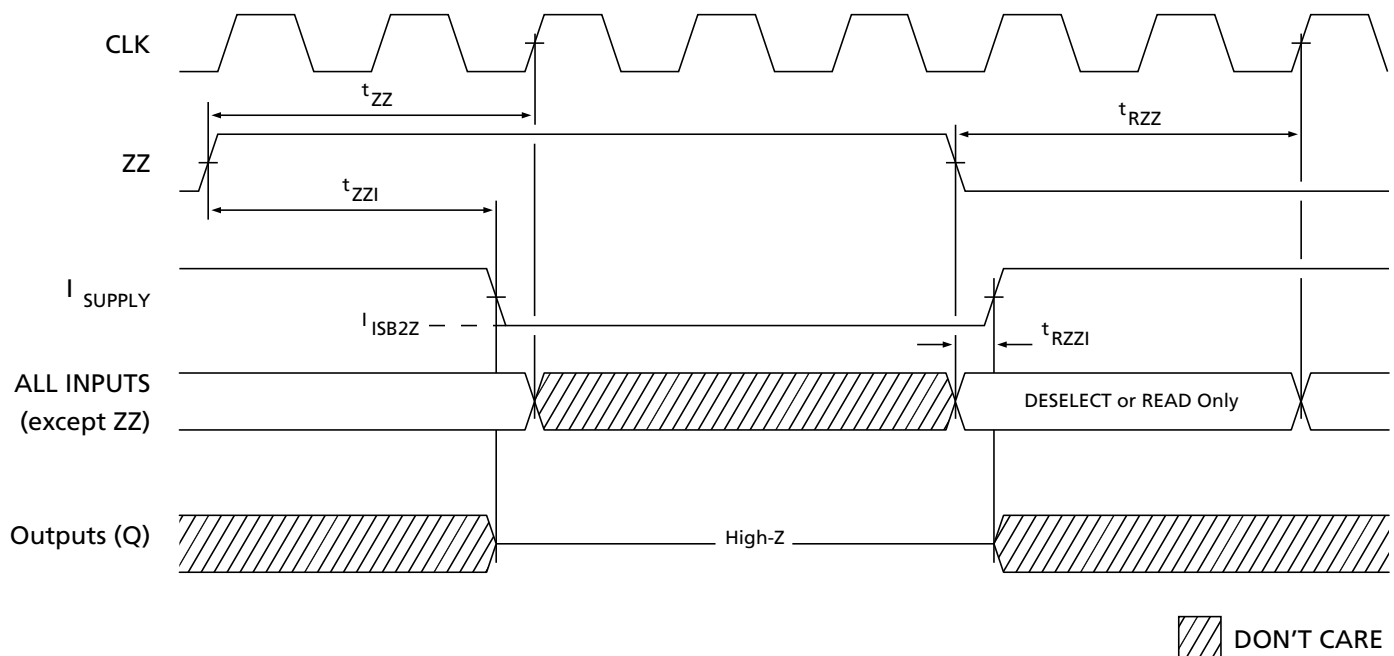
DON'T CARE

READ TIMING[3]

READ TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
t_{KC}	6.0		7.5		10		ns
f_{KF}		166		133		100	MHz
t_{KH}	2.3		2.5		3.0		ns
t_{KL}	2.3		2.5		3.0		ns
t_{KQ}		3.5		4.0		5.0	ns
t_{KQX}	1.5		1.5		1.5		ns
t_{KQLZ}	0		0		1.5		ns
t_{KQHZ}		3.5		4.2		5.0	ns
t_{OEQ}		3.5		4.2		5.0	ns
t_{OELZ}	0		0		0		ns
t_{OEHZ}		3.5		4.2		4.5	ns

SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
t_{AS}	1.5		1.5		2.0		ns
t_{ADSS}	1.5		1.5		2.0		ns
t_{AAS}	1.5		1.5		2.0		ns
t_{WS}	1.5		1.5		2.0		ns
t_{CES}	1.5		1.5		2.0		ns
t_{AH}	0.5		0.5		0.5		ns
t_{ADSH}	0.5		0.5		0.5		ns
t_{AAH}	0.5		0.5		0.5		ns
t_{WH}	0.5		0.5		0.5		ns
t_{CEH}	0.5		0.5		0.5		ns

NOTE:
1. Q(A2) refers to output from address A2. Q(A2 + 1) refers to output from the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. OE# does not cause Q to be driven until after the following clock rising edge.
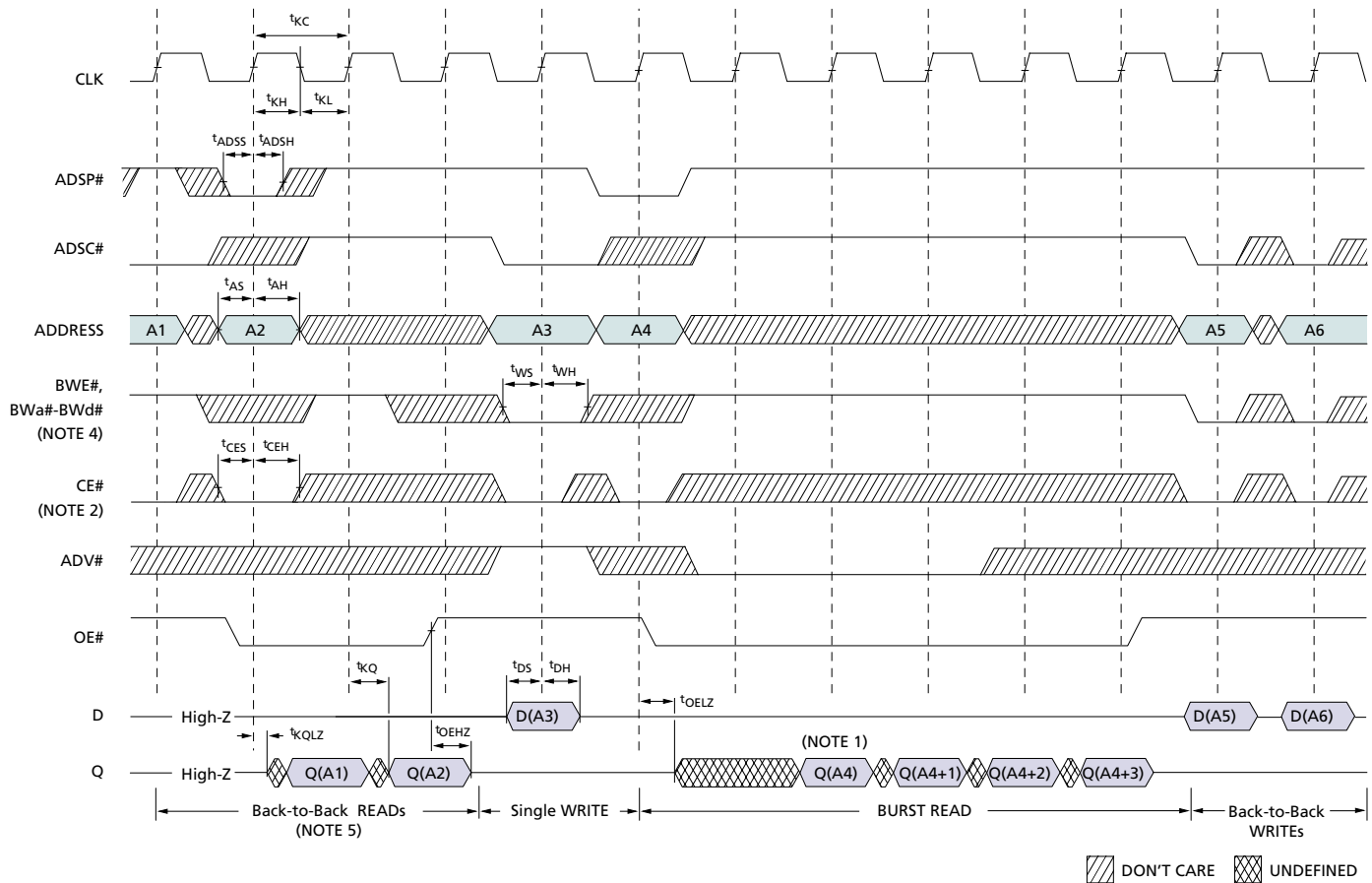4. Outputs are disabled within two clock cycles after deselect.

WRITE TIMING

WRITE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
^tKC	6.0		7.5		10		ns
^fKF		166		133		100	MHz
^tKH	2.3		2.5		3.0		ns
^tKL	2.3		2.5		3.0		ns
^tOEHZ		3.5		4.2		4.5	ns
^tAS	1.5		1.5		2.0		ns
^tADSS	1.5		1.5		2.0		ns
^tAAS	1.5		1.5		2.0		ns
^tWS	1.5		1.5		2.0		ns

SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
^tDS	1.5		1.5		2.0		ns
^tCES	1.5		1.5		2.0		ns
^tAH	0.5		0.5		0.5		ns
^tADSH	0.5		0.5		0.5		ns
^tAAH	0.5		0.5		0.5		ns
^tWH	0.5		0.5		0.5		ns
^tDH	0.5		0.5		0.5		ns
^tCEH	0.5		0.5		0.5		ns

NOTE:
1. D(A2) refers to input for address A2. D(A2 + 1) refers to input for the next internal burst address following A2.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. OE# must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. ADV# must be HIGH to permit a WRITE to the loaded address.
5. Full-width WRITE can be initiated by GW# LOW; or by GW# HIGH, BWE# LOW and BWa#-BWb# LOW for x18 device; or GW# HIGH, BWE# LOW and BWa#-BWd# LOW for x32 and x36 devices.
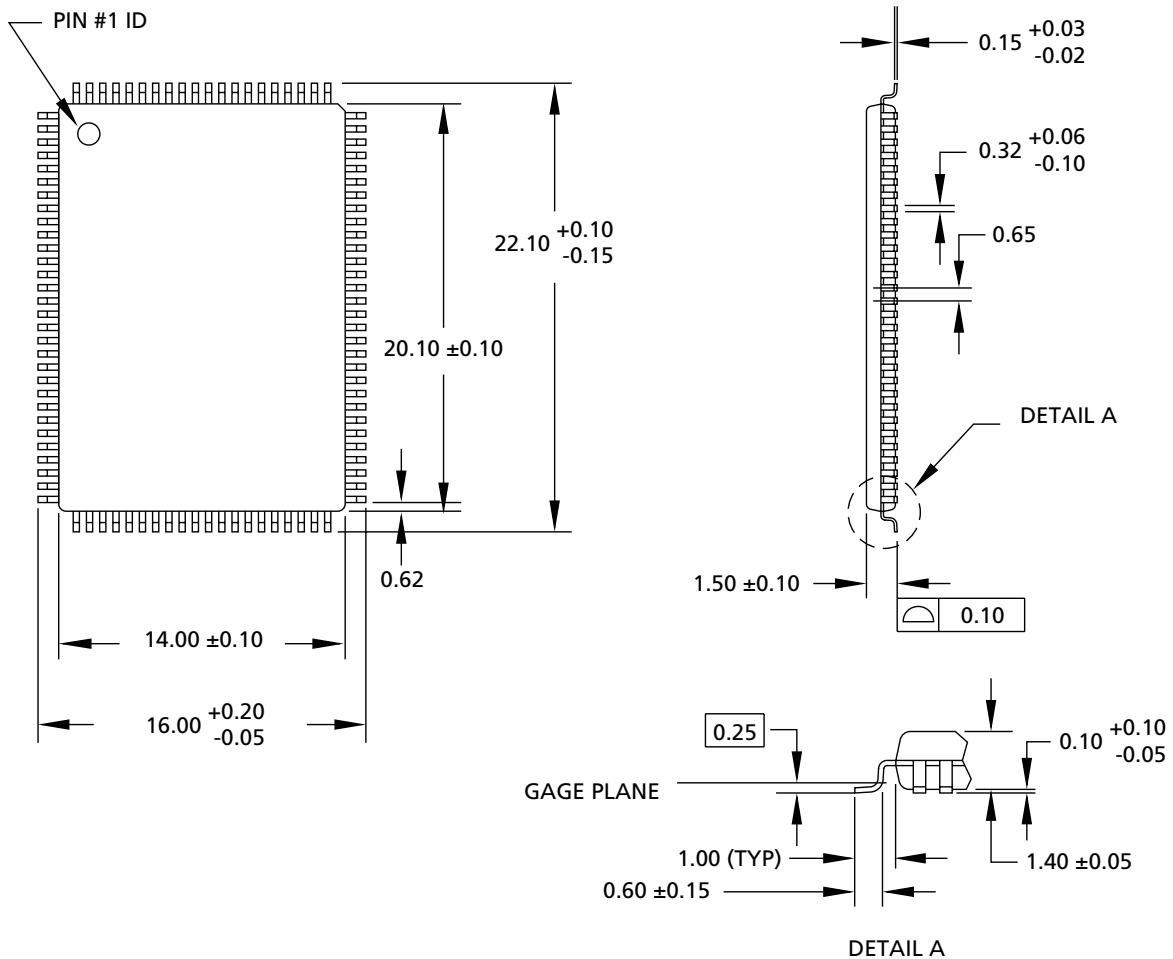
READ/WRITE TIMING[6]

WRITE TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
t_{KC}	6.0		7.5		10		ns
f_{KF}		166		133		100	MHz
t_{KH}	2.3		2.5		3.0		ns
t_{KL}	2.3		2.5		3.0		ns
t_{KQ}		3.5		4.0		5.0	ns
t_{KQLZ}	0		0		1.5		ns
t_{OELZ}	0		0		0		ns
t_{OEHZ}		3.5		4.2		4.5	ns
t_{AS}	1.5		1.5		2.0		ns

SYMBOL	-6 MIN	-6 MAX	-7.5 MIN	-7.5 MAX	-10 MIN	-10 MAX	UNITS
t_{ADSS}	1.5		1.5		2.0		ns
t_{WS}	1.5		1.5		2.0		ns
t_{DS}	1.5		1.5		2.0		ns
t_{CES}	1.5		1.5		2.0		ns
t_{AH}	0.5		0.5		0.5		ns
t_{ADSH}	0.5		0.5		0.5		ns
t_{WH}	0.5		0.5		0.5		ns
t_{DH}	0.5		0.5		0.5		ns
t_{CEH}	0.5		0.5		0.5		ns

NOTE: 1. Q(A4) refers to output from address A4. Q(A4 + 1) refers to output from the next internal burst address following A4.
2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP#, ADSC# or ADV# cycle is performed.
4. GW# is HIGH.
5. Back-to-back READs may be controlled by either ADSP# or ADSC#.
6. Timing is shown assuming that the device was not enabled before entering into this sequence.
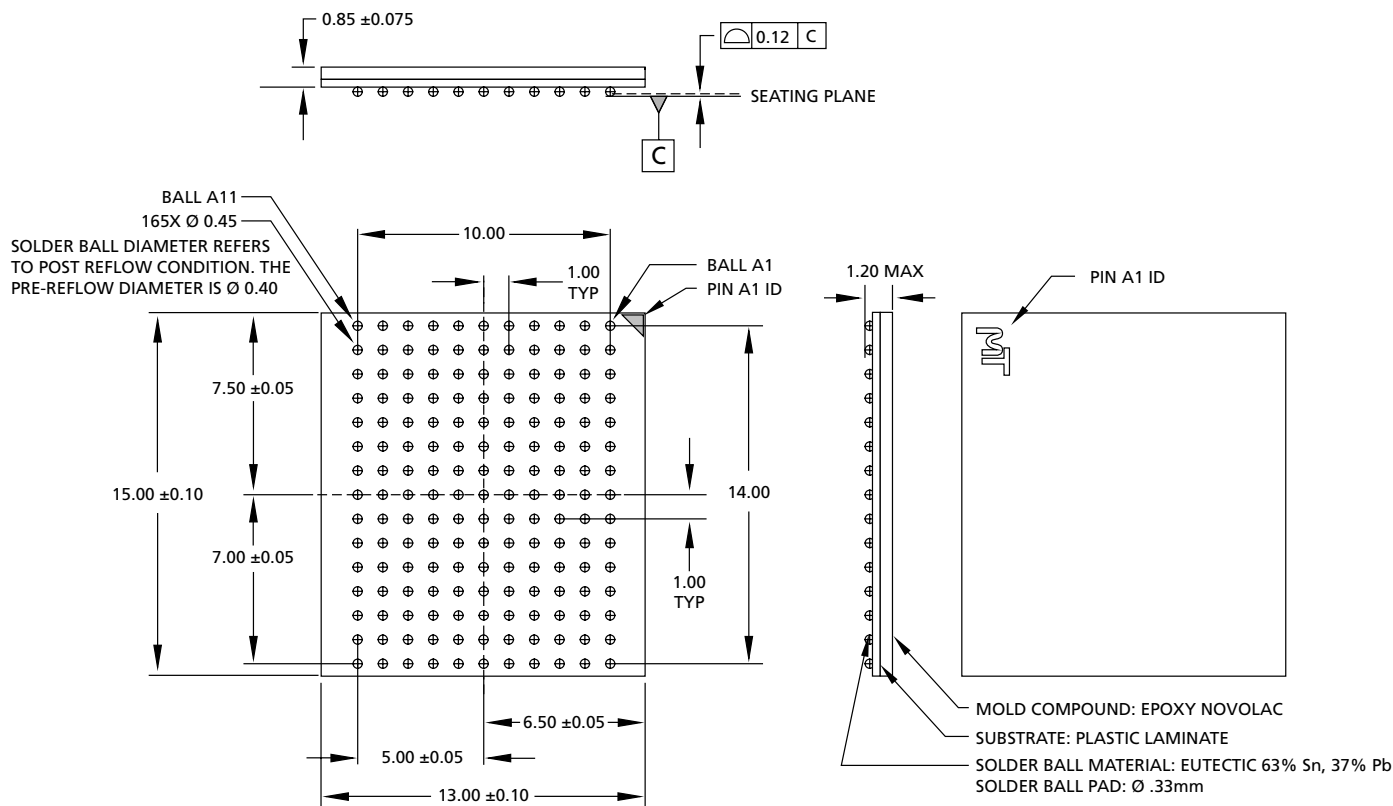
100-PIN PLASTIC TQFP (JEDEC LQFP)

PIN #1 ID

22.10 +0.10 / -0.15

20.10 ±0.10

0.62

14.00 ±0.10

16.00 +0.20 / -0.05

0.15 +0.03 / -0.02

0.32 +0.06 / -0.10

0.65

DETAIL A

1.50 ±0.10

0.10

0.25

GAGE PLANE

0.10 +0.10 / -0.05

1.00 (TYP)

0.60 ±0.15

1.40 ±0.05

DETAIL A

NOTE: 1. All dimensions in millimeters $\frac{MAX}{MIN}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

165-PIN FBGA

0.85 ±0.075

0.12 C

SEATING PLANE

C

BALL A11
165X Ø 0.45

SOLDER BALL DIAMETER REFERS
TO POST REFLOW CONDITION. THE
PRE-REFLOW DIAMETER IS Ø 0.40

10.00

1.00 TYP

BALL A1
PIN A1 ID

1.20 MAX

PIN A1 ID

7.50 ±0.05

15.00 ±0.10

14.00

7.00 ±0.05

1.00 TYP

6.50 ±0.05

5.00 ±0.05

13.00 ±0.10

MOLD COMPOUND: EPOXY NOVOLAC
SUBSTRATE: PLASTIC LAMINATE
SOLDER BALL MATERIAL: EUTECTIC 63% Sn, 37% Pb
SOLDER BALL PAD: Ø .33mm

NOTE: 1. All dimensions in millimeters $\frac{MAX}{MIN}$ or typical where noted.

REVISION HISTORY

Removed "Preliminary Package Data" from front page .... February 22/02

Removed 119-pin PBGA package and references .... February 14/02

Removed note "Not Recommended for New Designs," Rev. 6/01 .... June 7/01

Added Industrial Temperature note and reference, Rev. 3/01, FINAL .... March 6/01

Added 119-pin PBGA package, Rev. 1/01, FINAL .... January 10/01

Removed FBGA Part Marking Guide, REV 8/00-A, FINAL .... August 22/00

Changed FBGA capacitance values, REV 8/00, FINAL .... August 7/00
C_I; TYP 2.5pF from 4pF; MAX. 3.5pF from 5pF
C_O; TYP 4pF from 6pF; MAX. 5pF from 7pF
C_{CK}; TYP 2.5pF from 5pF; MAX. 3.5pF from 6pF

Added FBGA Part Marking Guide, Rev. 7/00, Preliminary .... July 18/00
Added revision history
Added FBGA Part Marking References
Removed 119-Pin PBGA package and references
Removed industrial temperature references

Added 165-pin FBGA package, Rev. 6/00, Preliminary .... May 23/00