Preliminary

OKI Semiconductor

Version E2: Sep. 1998

MSM66573 Family

Oki's Original High-Performance, 16-Bit CMOS Single-Chip Microcontrollers

Microcontrollers for Controlling Compact Devices

GENERAL DESCRIPTION

The MSM66573 family consists of high-performance, 16-bit CMOS single-chip microcontrollers based on Oki's own architecture.

Internal peripherals include a selection of multifunction timers configurable for compare output, input capture, event counting, auto reloading, and PWM output for such uses as measuring frequencies and time intervals. In addition to the main clock, the family supports a low-speed (32.768 kHz) clock for use in applications requiring energy conservation modes. Interfaces to external devices include a high-speed bus interface using separate address and data buses to eliminate the need for an external address latch and a three-channel serial interface.

The 16-bit core supports high-speed 16-bit arithmetic and a wide variety of bit manipulations, making the microcontrollers ideal for such system control applications as high-speed CD-ROM drives and other PC peripherals.

The family includes the flash ROM version MSM66Q573, rewritable with a single power supply (V_{DD} = 2.7 to 3.3/4.5 to 5.5 V) and thus rapidly adaptable for changing specifications and applying field upgrades.

APPLICATIONS

High-speed CD-ROM drives, PC peripherals, audiovisual equipment control sysems, office electronics control systems

FEATURES

Family device	MSM66572	MSM66573
Operating temperature	–30˚C to +70˚C	
Power supply voltage and maximum clock frequency	V_{DD} = 4.5 V to 5.5 V/f = 30 MHz V_{DD} = 2.4 V to 3.6 V/f = 14 MHz	
Minimum instruction execution time	67 ns @30 MHz (4.5 to 5.5 V) 143 ns @14 MHz (2.4 to 3.6 V) 61 µs @32.768 kHz (2.4 to 3.6/4.5 to 5.5 V)	
Internal ROM	48K Byte	64K Byte
(Maximum external ROM)	(1M Byte)	
Internal RAM	4K Byte	
(Maximum external RAM)	(1M Byte)	
I/O ports	75 I/O pins (with programmable pull-up resistors) Eight pins are for inputs only.	
Timers	One 16-bit free-running counter Two compare output/capture input channels	
	One 16-bit timer (auto reload/timer output) One 8-bit auto reload timer	
	Three 8-bit auto reload timers (These double as serial interface baud rate generators.)	
	One watchdog timer (This doubles as an 8-bit auto reload timer.)	
	One clock timer channel	
	Four 8-bit PWM channels (These are configurable as two 16-bit PWM channels.)	
Serial ports	One UART channel One synchronous channel One channel switchable between UART and synchronous operation	
Analog-to-digital converter	Eight 10-bit channels	
External interrupts	One non-maskable; six maskable	
Interrupt priorities	Three levels	
Miscellaneous	Separate address and data busses	
	Bus release function	
	Dual clock operation	
Flash ROM/One-time PROM versions	MSM66Q573/MSM66P573	

BLOCK DIAGRAM

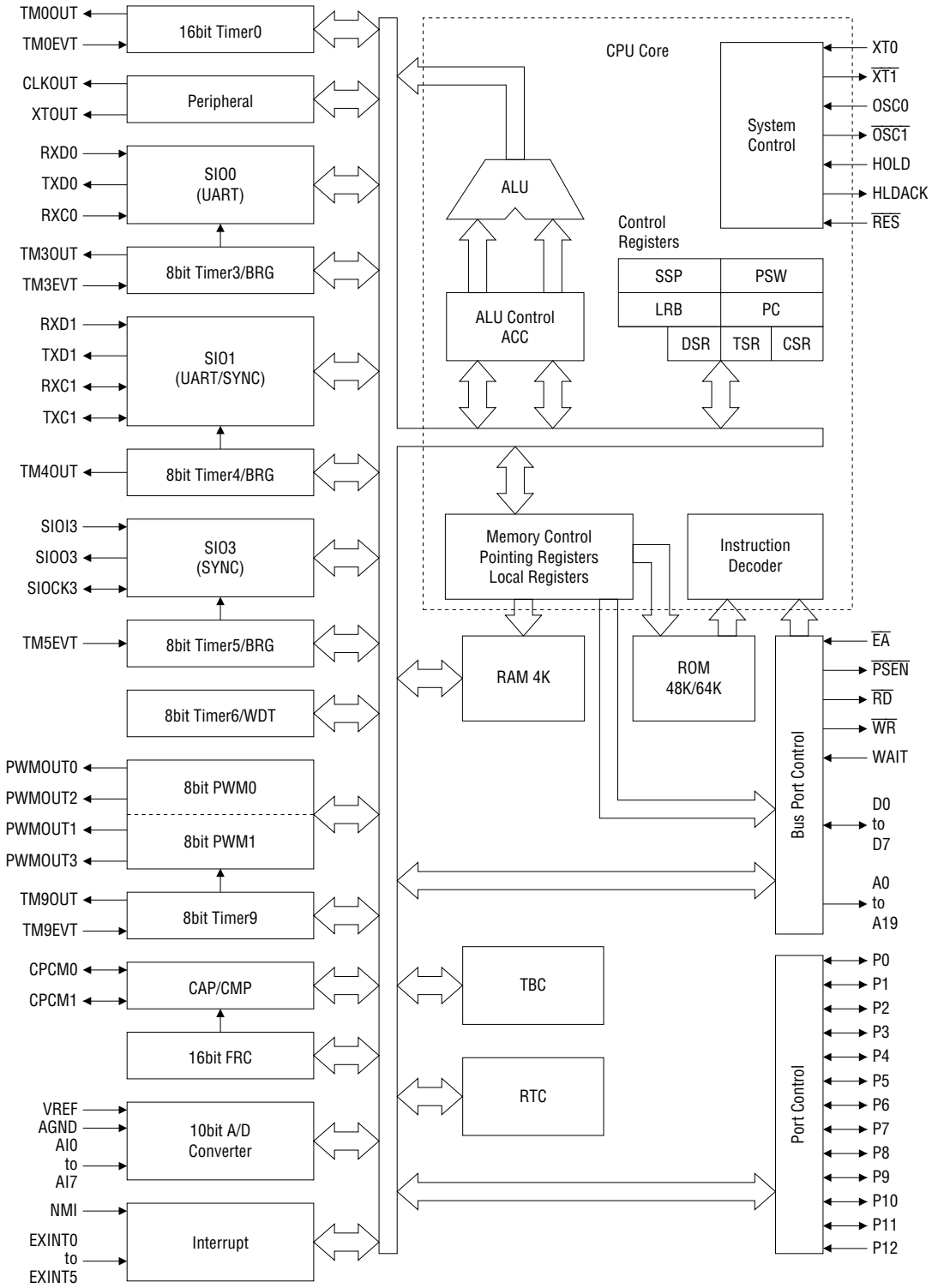


Figure 1 MSM66573 Family Block Diagram

PIN CONFIGURATION (TOP VIEW)

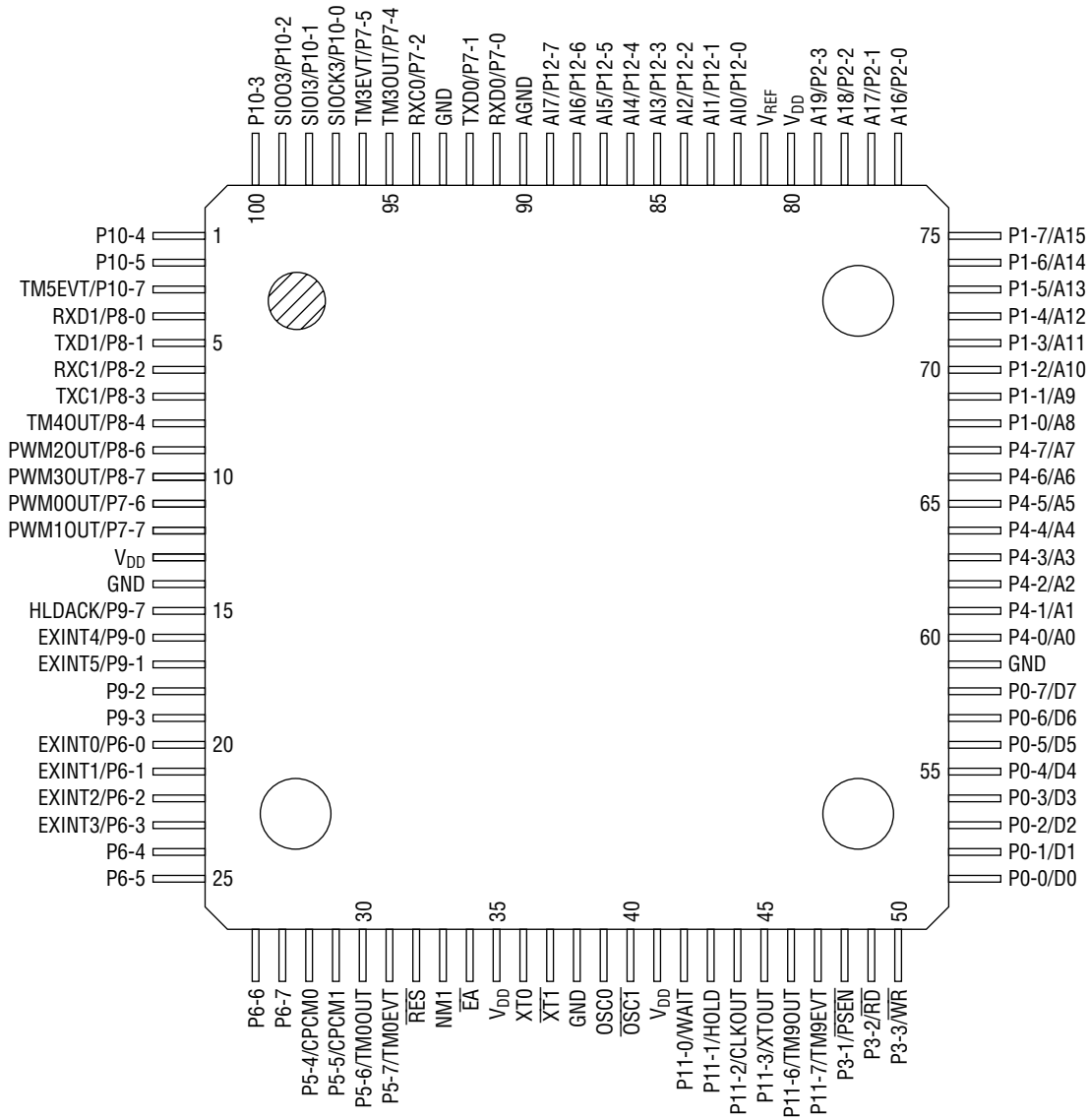


Figure 2 MSM66573 Family Pin Configuration (100-Pin Plastic TQFP)

PIN CONFIGURATION (TOP VIEW) (continued)

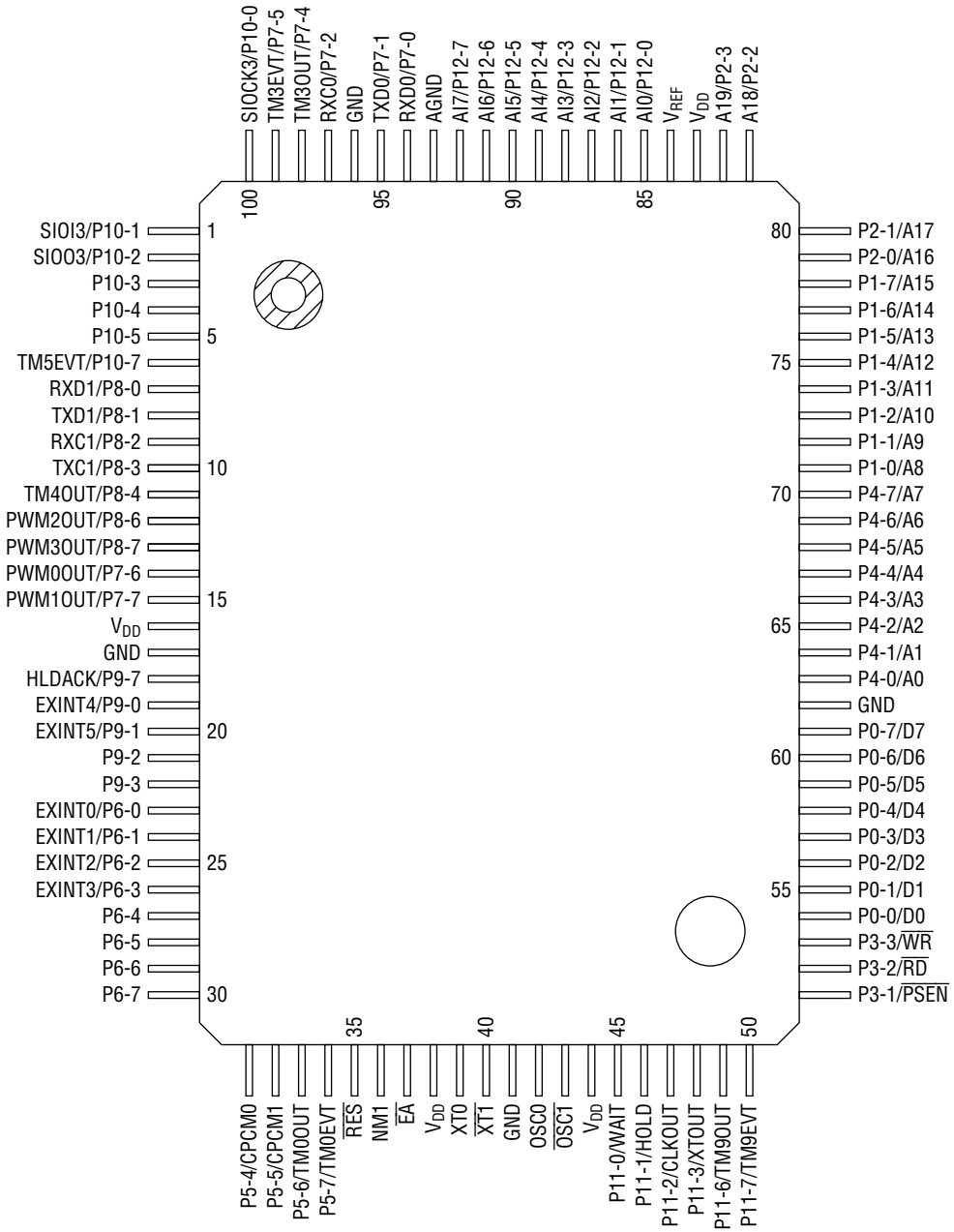


Figure 3 MSM66573 Family Pin Configuration (100-Pin Plastic QFP)

PIN DESCRIPTIONS

Table 1 lists the function of each pin in the MSM66573 family.
In the Type column, "I" indicates an input pin, "O" indicates an output pin, and "I/O" indicates an I/O pin.

Table 1 Pin Descriptions

Classification	Symbol	Function			
		Type	Primary function	Type	Secondary function
Port	P0_0/D0 to P0_7/D7	I/O	8-bit I/O port LED direct drive port Pull-up resistors can be specified for each individual bit	I/O	External memory access Data I/O port
	P1_0/A8 to P1_7/A15	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P2_0/A16 to P2_3/A19	I/O	4-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P3_1/$\overline{\text{PSEN}}$	I/O	3-bit I/O port LED direct drive port Pull-up resistors can be specified for each individual bit	O	External program memory access Read strobe output pin
	P3_2/$\overline{\text{RD}}$			O	External memory access Read strobe output pin
	P3_3/$\overline{\text{WR}}$			O	External memory access Write strobe output pin
	P4_0/A0 to P4_7/A7	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P5_4/CPCM0	I/O	4-bit I/O port Pull-up resistors can be specified for each individual bit	I/O	Capture 0 input/ Compare 0 output pin
	P5_5/CPCM1			I/O	Capture 1 input/ Compare 1 output pin
	P5_6/TM0OUT			O	Timer 0 timer output pin
	P5_7/TM0EVT			I	Timer 0 external event input pin
	P6_0/EXINT0	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	I	External interrupt 0 input pin
	P6_1/EXINT1			I	External interrupt 1 input pin
	P6_2/EXINT2			I	External interrupt 2 input pin
	P6_3/EXINT3			I	External interrupt 3 input pin
	P6_4 to P6_7			—	None

Table 1 Pin Descriptions (continued)

Classification	Symbol	Function			
		Type	Primary function	Type	Secondary function
Port	P7_0/RXD0	I/O	7-bit I/O port	I	SIO0 receive data input pin
	P7_1/TXD0		Pull-up resistors can be specified	O	SIO0 transmit data output pin
	P7_2/RXC0		for each individual bit	I	SIO0 external clock input pin
	P7_4/TM3OUT			O	Timer 3 timer output pin
	P7_5/TM3EVT			I	Timer 3 external event input pin
	P7_6/PWM0OUT			O	PWM0 output pin
	P7_7/PWM1OUT			O	PWM1 output pin
	P8_0/RXD1	I/O	7-bit I/O port	I	SIO1 receive data input pin
	P8_1/TXD1		Pull-up resistors can be specified	O	SIO1 transmit data output pin
	P8_2/RXC1		for each individual bit	I/O	SIO1 receive clock I/O pin
	P8_3/TXC1			I/O	SIO1 transmit clock I/O pin
	P8_4/TM4OUT			O	Timer 4 timer output pin
	P8_6/PWM2OUT			O	PWM2 output pin
	P8_7/PWM3OUT			O	PWM3 output pin
	P9_0/EXINT4	I/O	5-bit I/O port	I	External interrupt 4 input pin
	P9_1/EXINT5		Pull-up resistors can be specified	I	External interrupt 5 input pin
	P9_2, P9_3		for each individual bit	—	None
	P9_7/HLDACK			O	HOLD mode output pin
	P10_0/SIOCK3	I/O	7-bit I/O port	I/O	SIO3 transmit-receive clock I/O pin
	P10_1/SIOI3		Pull-up resistors can be specified	I	SIO3 receive data input pin
	P10_2/SIOO3		for each individual bit	O	SIO3 transmit data output pin
	P10_3 to P10_5			—	None
	P10_7/TM5EVT			I	Timer 5 external event input pin
	P11_0/WAIT	I/O	6-bit I/O port LED direct drive port	I	External data memory access wait input pin
	P11_1/HOLD		Pull-up resistors can be specified	I	HOLD mode request input pin
	P11_2/CLKOUT		for each individual bit	O	Main clock pulse output pin
	P11_3/XTOUT			O	Sub clock pulse output pin
	P11_6/TM9OUT			O	Timer 9 timer output pin
	P11_7/TM9EVT			I	Timer 9 external event input pin
	P12_0/AI0 to P12_7/AI7	I	8-bit input port	I	A/D converter analog input port

Table 1 Pin Descriptions (continued)

Classification	Symbol	Type	Function
Power supply	V_{DD}	I	Power supply pin Connect all V_{DD} pins to the power supply.
	GND	I	GND pin Connect all GND pins to GND.
	V_{REF}	I	Analog reference voltage pin
	AGND	I	Analog GND pin
Oscillation	XT0	I	Sub clock oscillation input pin Connect to a crystal oscillator of f = 32.768 kHz.
	$\overline{XT1}$	O	Sub clock oscillation output pin Connect to a crystal oscillator of f = 32.768 kHz. The clock output is opposite in phase to XT0.
	OSC0	I	Main clock oscillation input pin Connect to a crystal or ceramic oscillator. Or, input an external clock.
	$\overline{OSC1}$	O	Main clock oscillation output pin Connect to a crystal or ceramic oscillator. The clock output is opposite in phase to OSC0. Leave this pin unconnected when an external clock is used.
Reset	$\overline{RES}$	I	Reset input pin
Other	NMI	I	Non-maskable interrupt input pin
	$\overline{EA}$	I	External program memory access input pin If the $\overline{EA}$ pin goes to a low level, all program addresses of external program memory are accessed.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Digital power supply voltage	V_{DD}	GND = AGND = 0 V Ta = 25°C		–0.3 to +7.0	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog reference voltage	V_{REF}			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AI}			–0.3 to V_{REF}	V
Power Dissipation	PD	Ta = 70°C	1 per package	650	mW
			1 per output	8	mW
Storage temperature	T_{STG}	—		–50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Range	Unit
Digital power supply voltage	V_{DD}	MSM66572	$f_{OSC} \leq 30$ MHz	4.5 to 5.5	V
		MSM66573	$f_{OSC} \leq 14$ MHz	2.4 to 3.6 *1	
		MSM66Q573	$f_{OSC} \leq 30$ MHz	4.5 to 5.5	
			$f_{OSC} \leq 14$ MHz	2.7 to 3.3	
		MSM66P573	$f_{OSC} \leq 24$ MHz	4.5 to 5.5	
			$f_{OSC} \leq 12$ MHz	2.7 to 3.6 *1	
Analog reference voltage	V_{REF}	—		V_{DD} – 0.3 to V_{DD}	V
Analog input voltage	V_{AI}	—		AGND to V_{REF}	V
Memory hold voltage	V_{DDH}	f_{OSC} = 0 Hz		2.0 to 5.5	V
Operating frequency	f_{OSC}	MSM66572	V_{DD} = 4.5 to 5.5 V	2 to 30	MHz
		MSM66573	V_{DD} = 2.4 to 3.6 V	2 to 14	
		MSM66Q573	V_{DD} = 4.5 to 5.5 V	2 to 30	
			V_{DD} = 2.7 to 3.3 V	2 to 14	
		MSM66P573	V_{DD} = 4.5 to 5.5 V	2 to 24	
			V_{DD} = 2.7 to 3.6 V	2 to 12	
Ambient temperature	Ta	—		–30 to +70	°C
Fan out	N	MOS load		20	—
		TTL load	P0, P3, P11	6	—
			P1, P2, P4, P5 P6, P7, P8, P9, P10	1	—

*1 In this data sheet, electrical characteristics are shown up to 3.3 V for low-voltage operation. Please contact Oki sales office to refer to the 3.6 V operation electrical characteristics.

ALLOWABLE OUTPUT CURRENT VALUES

Parameter	Pin	Symbol	Min.	Typ.	Max.	Unit
"H" output pin (1 pin)	All output pins	I_{OH}	—	—	–2	mA
"H" output pins (sum total)	Sum total of all output pins	ΣI_{OH}	—	—	–40	
"L" output pin (1 pin)	P0, P3, P11	I_{OL}	—	—	10	
	Other ports				5	
"L" output pins (sum total)	Sum total of P0, P3, P11	ΣI_{OL}	—	—	80	
	Sum total of P1, P2, P4				50	
	Sum total of P5, P6, P9					
	Sum total of P7, P8, P10					
	Sum total of all output pins				140	

Note: Connect the power supply voltage to all V_{DD} pins and the ground voltage to all GND pins.

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD} = 4.5 to 5.5 V)

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage *1	V_{IH}	—	0.44V_{DD}	—	V_{DD} + 0.3	V
"H" input voltage *2, *3, *4, *5, *6, *7			0.80V_{DD}	—	V_{DD} + 0.3	
"L" input voltage *1	V_{IL}	—	–0.3	—	0.16V_{DD}	
"L" input voltage *2, *3, *4, *5, *6, *7			–0.3	—	0.2V_{DD}	
"H" output voltage *1, *4	V_{OH}	I_O = –400 µA	V_{DD} – 0.4	—	—	
		I_O = –2.0 mA	V_{DD} – 0.6	—	—	
"H" output voltage *2		I_O = –200 µA	V_{DD} – 0.4	—	—	
		I_O = –2.0 mA	V_{DD} – 0.6	—	—	
"L" output voltage *1, *4	V_{OL}	I_O = 3.2 mA	—	—	0.4	
		I_O = 10.0 mA	—	—	0.8	
"L" output voltage *2		I_O = 1.6 mA	—	—	0.4	
		I_O = 5.0 mA	—	—	0.8	
Input leakage current *3, *6	I_{IH}/I_{IL}	V_I = V_{DD}/0 V	—	—	1/–1	µA
Input current *5			—	—	1/–250	
Input current *7			—	—	15/–15	
Output leakage current *1, *2, *4	I_{LO}	V_O = V_{DD}/0 V	—	—	±10	µA
Pull-up resistance	R_{pull}	V_I = 0 V	25	50	100	kΩ
Input capacitance	C_I	f = 1 MHz, Ta = 25°C	—	5	—	pF
Output capacitance	C_O		—	7	—	
Analog reference supply current	I_{REF}	During A/D operation	—	—	4	mA
		When A/D is stopped	—	—	10	µA
Supply current (during STOP mode)	I_{DDS}	V_{DD} = 2 V, Ta = 25°C*	—	0.2	10	µA
		*8	—	1	100	
Supply current (during HALT mode)	I_{DDH}	f_{OSC} = 30 MHz, No Load	—	—	TBD	mA
Supply current	I_{DD}		—	—	TBD	
		During XTCLK (32.768 kHz) operation	—	—	TBD	

*1. Applicable to P0
*2. Applicable to P1, P2, P4, P5, P6, P7, P8, P9, P10
*3. Applicable to P12
*4. Applicable to P3, P11
*5. Applicable to $\overline{RES}$
*6. Applicable to $\overline{EA}$, NMI
*7. Applicable to OSC0
*8. Ports used as inputs are at V_{DD} or 0 V Other ports are unloaded

DC Characteristics (V_{DD} = 2.4 to 3.3 V)

MSM66572/573 (V_{DD} = 2.4 to 3.3 V, Ta = –30 to +70°C)
MSM66P573/Q573 (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage *1	V_{IH}	—	0.44V_{DD}	—	V_{DD} + 0.3	V
"H" input voltage *2, *3, *4, *5, *6, *7			0.80V_{DD}	—	V_{DD} + 0.3	
"L" input voltage *1	V_{IL}	—	–0.3	—	0.16V_{DD}	
"L" input voltage *2, *3, *4, *5, *6, *7			–0.3	—	0.2V_{DD}	
"H" output voltage *1, *4	V_{OH}	I_O = –400 µA	V_{DD} – 0.4	—	—	
		I_O = –2.0 mA	V_{DD} – 0.8	—	—	
"H" output voltage *2		I_O = –200 µA	V_{DD} – 0.4	—	—	
		I_O = –1.0 mA	V_{DD} – 0.8	—	—	
"L" output voltage *1, *4	V_{OL}	I_O = 3.2 mA	—	—	0.5	
		I_O = 5.0 mA	—	—	0.9	
"L" output voltage *2		I_O = 1.6 mA	—	—	0.5	
		I_O = 2.5 mA	—	—	0.9	
Input leakage current *3, *6	I_{IH}/I_{IL}	V_I = V_{DD}/0 V	—	—	1/–1	µA
Input current *5			—	—	1/–250	
Input current *7			—	—	15/–15	
Output leakage current *1, *2, *4	I_{LO}	V_O = V_{DD}/0 V	—	—	±10	µA
Pull-up resistance	R_{pull}	V_I = 0 V	40	100	200	kΩ
Input capacitance	C_I	f = 1 MHz, Ta = 25°C	—	5	—	pF
Output capacitance	C_O		—	7	—	
Analog reference supply current	I_{REF}	During A/D operation	—	—	2	mA
		When A/D is stopped	—	—	5	µA
Supply current (during STOP mode)	I_{DDS}	V_{DD} = 2 V, Ta = 25°C*	—	0.2	10	µA
		*8	—	1	100	
Supply current (during HALT mode)	I_{DDH}	f_{OSC} = 14 MHz, No Load	—	—	TBD	mA
Supply current	I_{DD}		—	—	TBD	
		During XTCLK (32.768 kHz) operation	—	—	TBD	

*1. Applicable to P0
*2. Applicable to P1, P2, P4, P5, P6, P7, P8, P9, P10
*3. Applicable to P12
*4. Applicable to P3, P11
*5. Applicable to $\overline{RES}$
*6. Applicable to $\overline{EA}$, NMI
*7. Applicable to OSC0
*8. Ports used as inputs are at V_{DD} or 0 V Other ports are unloaded

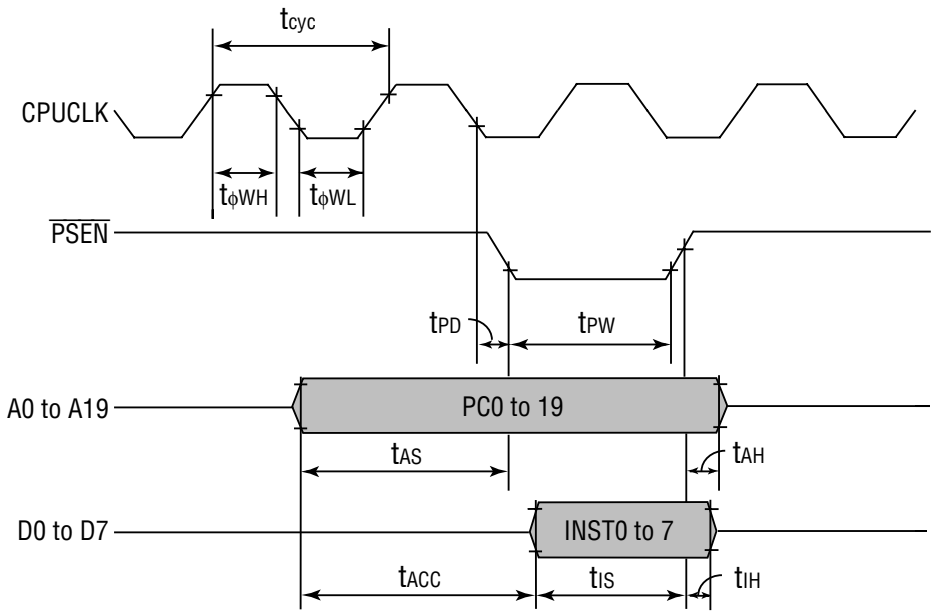
AC Characteristics (V_{DD} = 4.5 to 5.5 V)

[1] External program memory control

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
$\overline{PSEN}$ pulse width	t_{PW}		2 tϕ – 15	—	
$\overline{PSEN}$ pulse delay time	t_{PD}		—	45	
Address setup time	t_{AS}		tϕ – 25	—	
Address hold time	t_{AH}		0	9	
Instruction setup time	t_{IS}		30	—	
Instruction hold time	t_{IH}		0	—	
Read data access time	t_{ACC}		—	3 tϕ – 70*1	

Note: tϕ = t_{cyc}/2



Bus timing during no wait cycle time

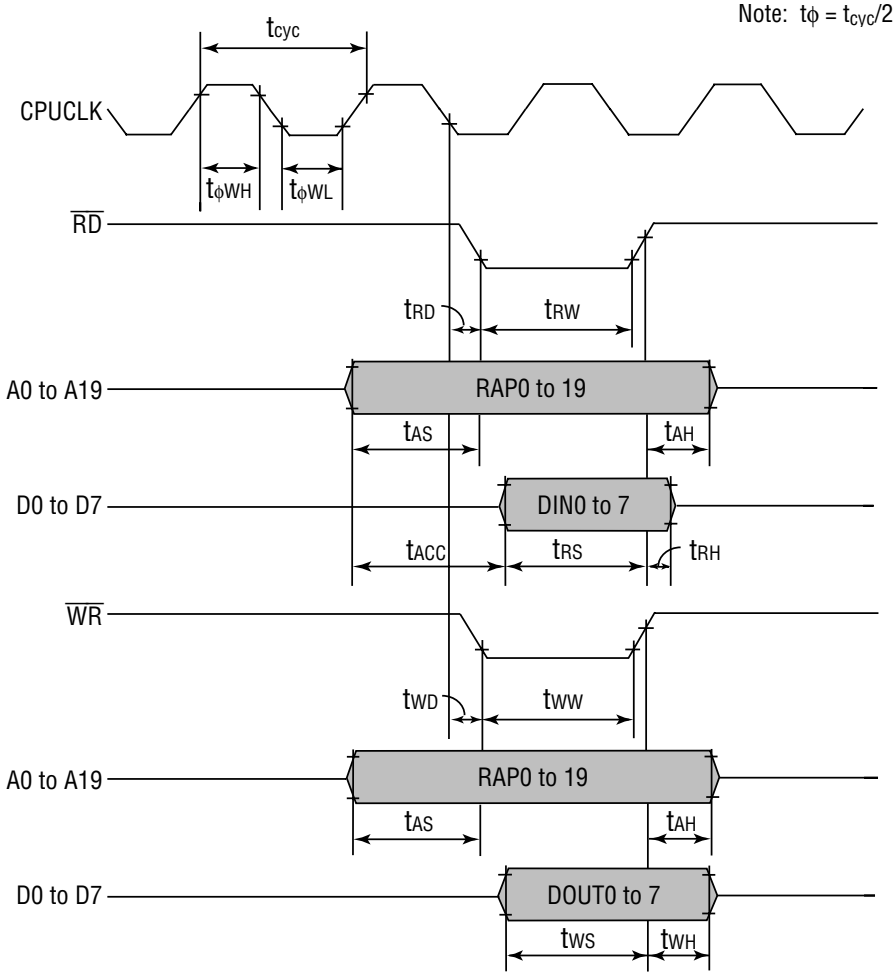
*1: The read data access time (t_{ACC}) is (3 + 2n) tϕ – 70 when n wait cycles are inserted.

[2] External data memory control

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
$\overline{RD}$ pulse width	t_{RW}		2 tϕ – 15	—	
$\overline{WR}$ pulse width	t_{WW}		2 tϕ –15	—	
$\overline{RD}$ pulse delay time	t_{RD}		—	45	
$\overline{WR}$ pulse delay time	t_{WD}		—	45	
Address setup time	t_{AS}		tϕ – 25	—	
Address hold time	t_{AH}		tϕ – 3	tϕ + 3	
Read data setup time	t_{RS}		30	—	
Read data hold time	t_{RH}		0	—	
Read data access time	t_{ACC}		—	3 tϕ – 70*1	
Write data setup time	t_{WS}		2 tϕ – 30	—	
Write data hold time	t_{WH}		tϕ – 3	tϕ + 3	

Note: $t\phi = t_{cyc}/2$



Bus timing during no wait cycle time

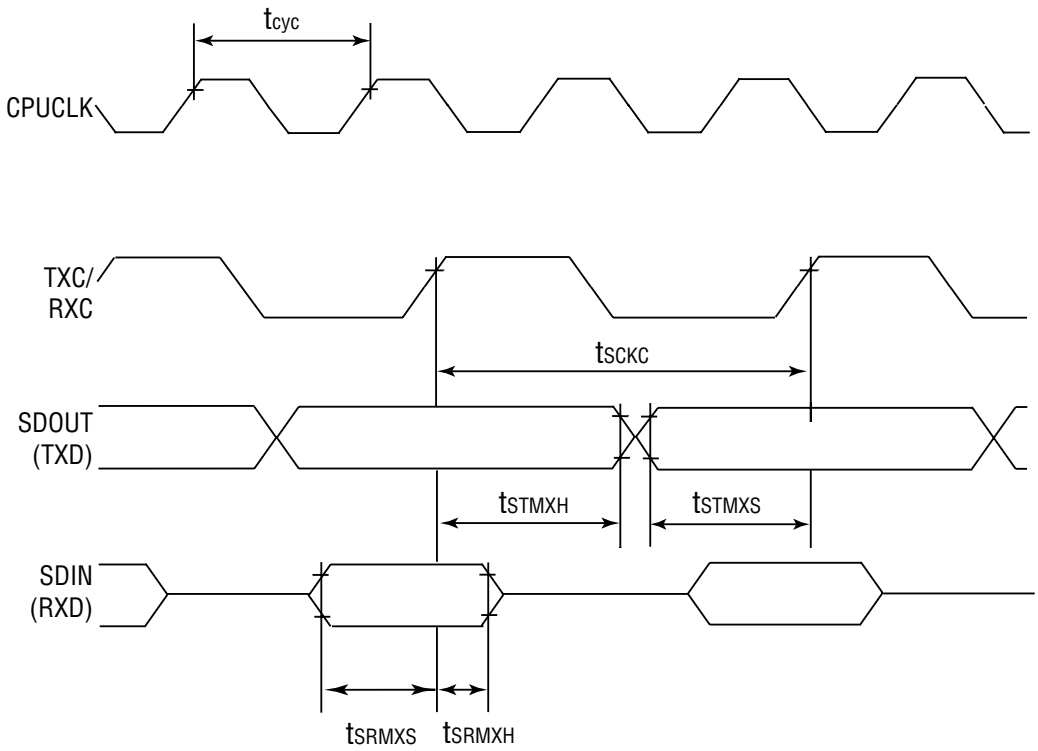
[3] Serial port control

Master mode

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2 tϕ – 5	—	
Output data hold time	t_{STMXH}		5 tϕ – 10	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		0	—	

Note: tϕ = t_{cyc}/2

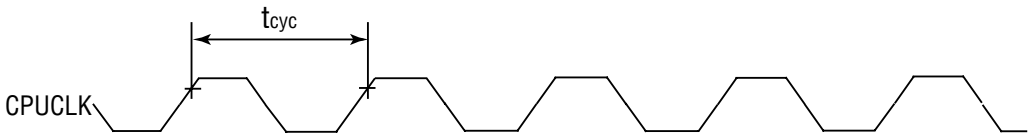


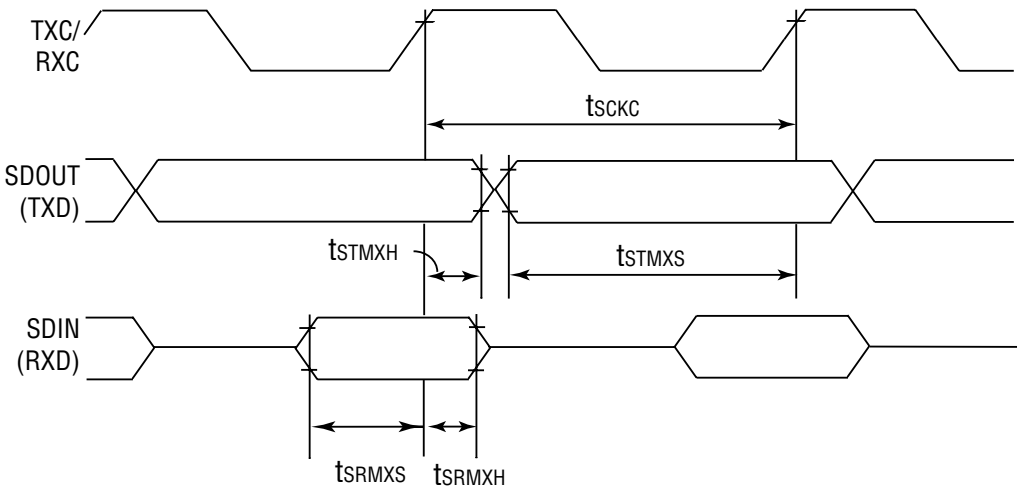
Slave mode

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

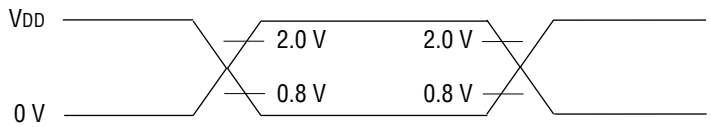
Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2 tϕ – 15	—	
Output data hold time	t_{STMXH}		4 tϕ – 10	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		3	—	

Note: $t\phi = t_{cyc}/2$

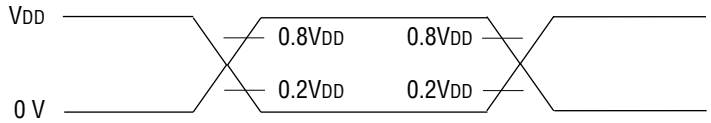




Measurement points for AC timing (except the serial port)



Measurement points for AC timing (the serial port)



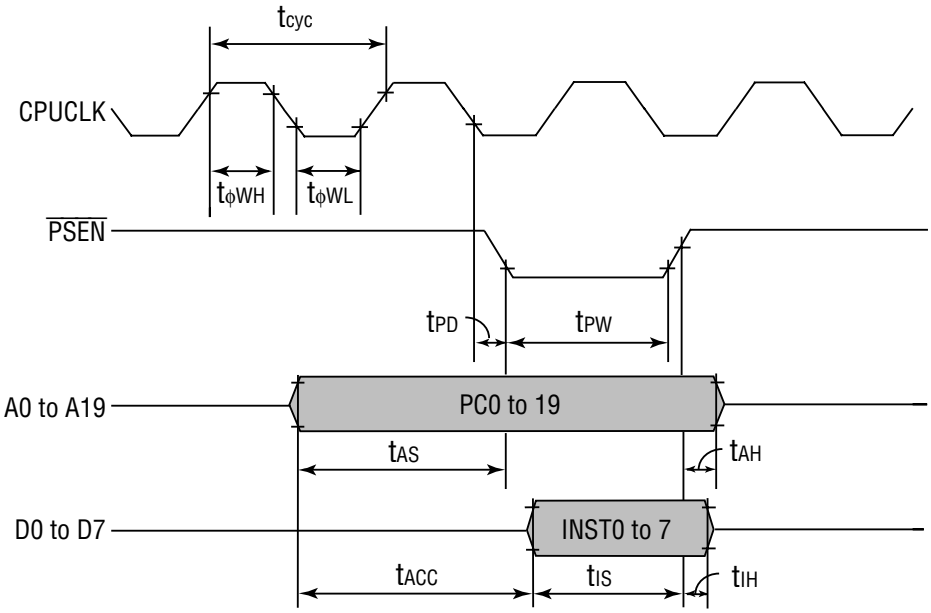
AC Characteristics (V_{DD} = 2.4 to 3.3 V)

[1] External program memory control

MSM66572/573 (V_{DD} = 2.4 to 3.3 V, Ta = –30 to +70°C)
MSM66P573/Q573 (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
$\overline{PSEN}$ pulse width	t_{PW}		2 tϕ – 20	—	
$\overline{PSEN}$ pulse delay time	t_{PD}		—	75	
Address setup time	t_{AS}		tϕ – 40	—	
Address hold time	t_{AH}		0	18	
Instruction setup time	t_{IS}		60	—	
Instruction hold time	t_{IH}		0	—	
Read data access time	t_{ACC}		—	3 tϕ – 120*2	

Note: tϕ = t_{cyc}/2



Bus timing during no wait cycle time

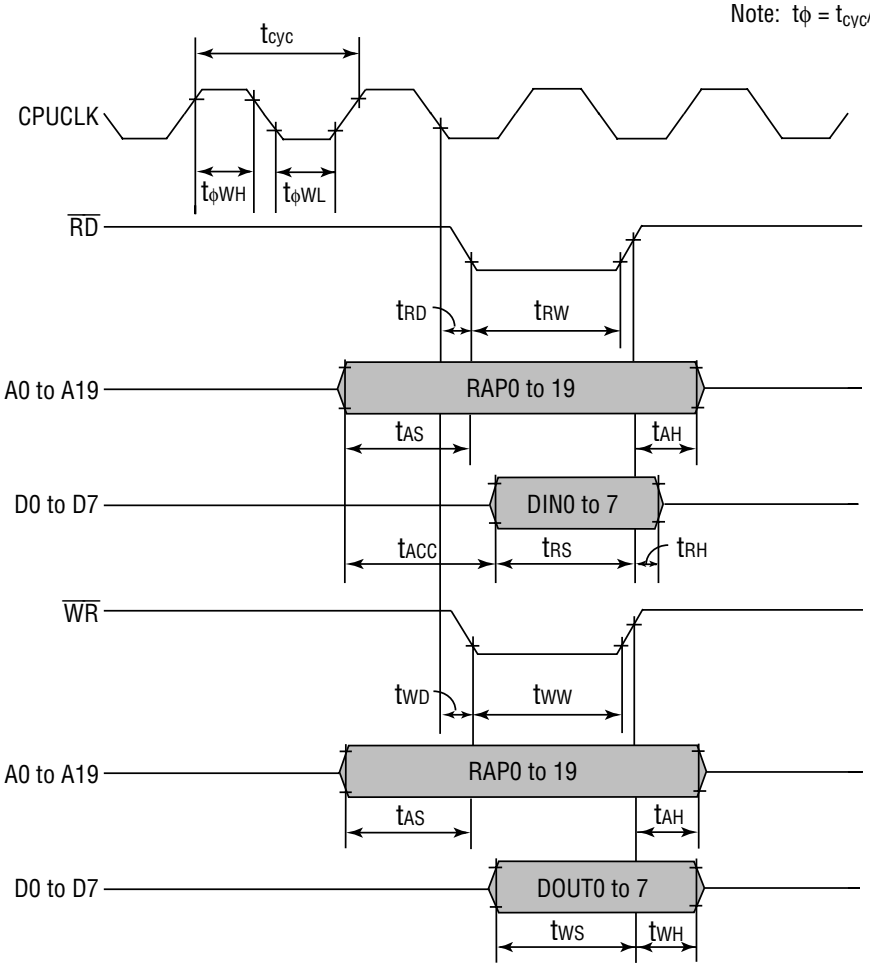
*2: The read data access time (t_{ACC}) is (3 + 2n) tϕ – 120 when n wait cycles are inserted.

[2] External data memory control

MSM66572/573 (V_{DD} = 2.4 to 3.3 V, Ta = –30 to +70°C)
MSM66P573/Q573 (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
$\overline{RD}$ pulse width	t_{RW}		2 tϕ – 20	—	
$\overline{WR}$ pulse width	t_{WW}		2 tϕ – 20	—	
$\overline{RD}$ pulse delay time	t_{RD}		—	75	
$\overline{WR}$ pulse delay time	t_{WD}		—	75	
Address setup time	t_{AS}		tϕ – 40	—	
Address hold time	t_{AH}		tϕ – 6	tϕ + 6	
Read data setup time	t_{RS}		60	—	
Read data hold time	t_{RH}		0	—	
Read data access time	t_{ACC}		—	3 tϕ – 120*2	
Write data setup time	t_{WS}		2 tϕ – 40	—	
Write data hold time	t_{WH}		tϕ – 6	tϕ + 6	

Note: $t\phi = t_{cyc}/2$



Bus timing during no wait cycle time

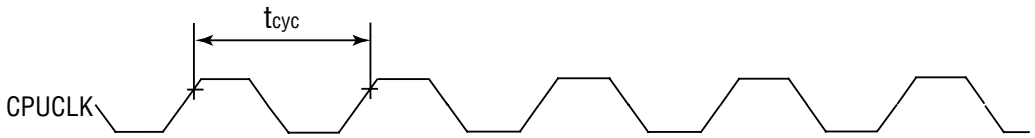
[3] Serial port control

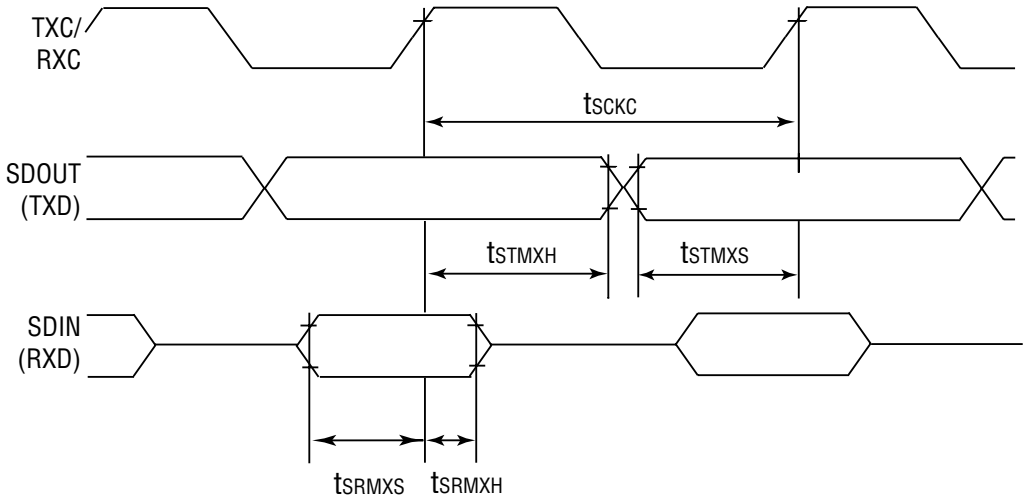
Master mode

MSM66572/573 (V_{DD} = 2.4 to 3.3 V, Ta = –30 to +70°C)
MSM66P573/Q573 (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2 $t\phi$ – 10	—	
Output data hold time	t_{STMXH}		5 $t\phi$ – 20	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		0	—	

Note: $t\phi = t_{cyc}/2$



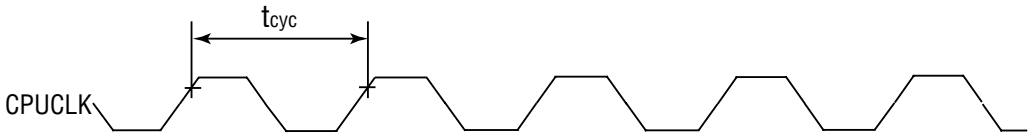


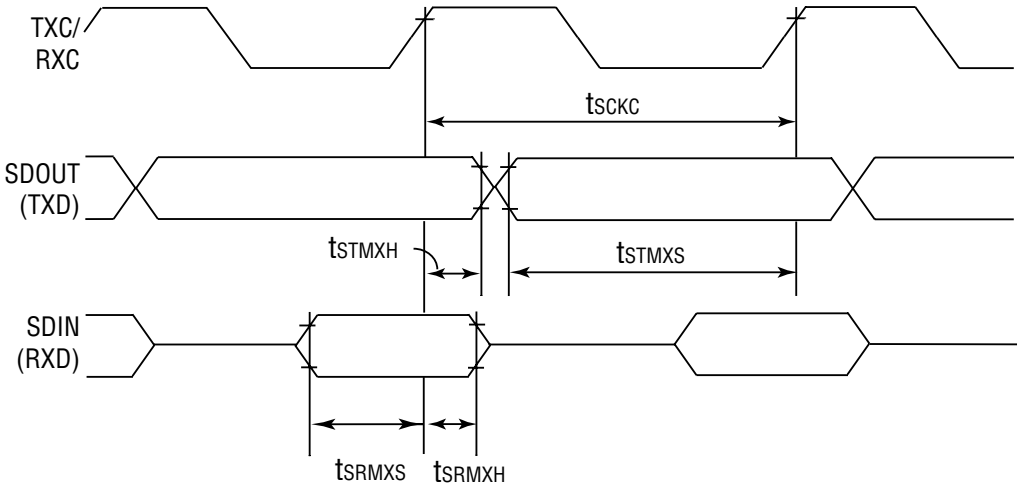
Slave mode

MSM66572/573 (V_{DD} = 2.4 to 3.3 V, Ta = –30 to +70°C)
MSM66P573/Q573 (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

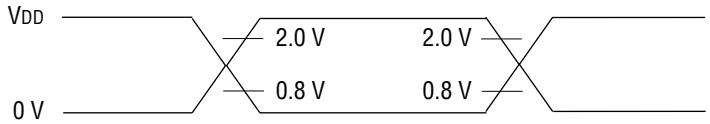
Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2 $t\phi$ – 30	—	
Output data hold time	t_{STMXH}		4 $t\phi$ – 20	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		7	—	

Note: $t\phi = t_{cyc}/2$

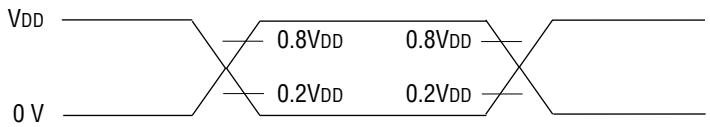




Measurement points for AC timing (except the serial port)



Measurement points for AC timing (the serial port)



A/D Converter Characteristics (V_{DD} = 4.5 to 5.5 V)

(Ta = –30 to +70°C, V_{DD} = V_{REF} = 4.5 V to 5.5 V, AGND = GND = 0 V)

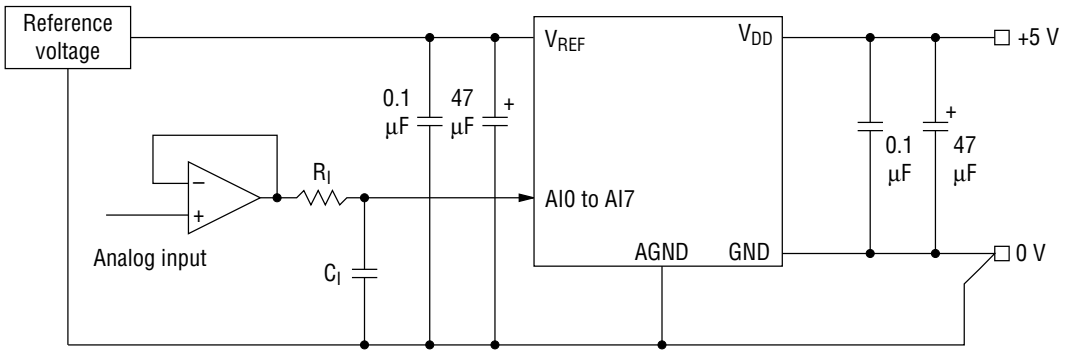
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit of Fig.4 Analog input source impedance Ri ≤ 5 kΩ t_{conv} = 10.7 µs	—	10	—	Bit
Linearity error	E_L		—	—	±3	LSB
Differential linearity error	E_D		—	—	±2	
Zero scale error	E_{ZS}		—	—	+3	
Full-scale error	E_{FS}		—	—	–3	
Cross talk	E_{CT}	Refer to measurement circuit of Fig.5	—	—	±1	
Conversion time	t_{CONV}	Set according to ADTM set data	10.7	—	—	µs/ch

A/D Converter Characteristics (V_{DD} = 2.4 to 3.3 V)

(Ta = –30 to +70°C, V_{DD} = V_{REF} = 2.4 to 3.3 V, AGND = GND = 0 V)

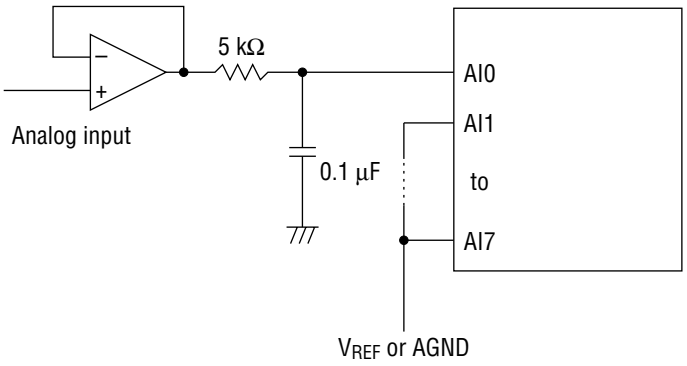
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit of Fig.4 Analog input source impedance Ri ≤ 5 kΩ t_{conv} = 13.7 µs	—	10	—	Bit
Linearity error	E_L		—	—	±3	LSB
Differential linearity error	E_D		—	—	±2	
Zero scale error	E_{ZS}		—	—	+3	
Full-scale error	E_{FS}		—	—	–3	
Cross talk	E_{CT}	Refer to measurement circuit of Fig.5	—	—	±1	
Conversion time	t_{CONV}	Set according to ADTM set data	27.4	—	—	µs/ch

For the MSM66P573, the A/D conversion time should be 32 µs or more.



R_I (impedance of analog input source) ≤ 5 kΩ
C_I ≒ 0.1 µF

Figure 4 Measurement Circuit



Cross talk is the difference between the A/D conversion results when the same analog input is applied to AI0 through AI7 and the A/D conversion results of the circuit to the left.

Figure 5 Cross Talk Measurement Circuit

Definition of Terminology

1. Resolution
   Resolution is the value of minimum discernable analog input.
   With 10 bits, since $2^{10} = 1024$, resolution of (VREF – AGND) ÷ 1024 is possible.

2. Linearity error
   Linearity error is the difference between ideal conversion characteristics and actual conversion characteristics of a 10-bit A/D converter (not including quantization error). Ideal conversion characteristics can be obtained by dividing the voltage between VREF and AGND into 1024 equal steps.

3. Differential linearity error
   Differential linearity error indicates the smoothness of conversion characteristics. Ideally, the range of analog input voltage that corresponds to 1converted bit of digital output is 1LSB = (VREF – AGND) ÷ 1024. Differential error is the difference between this ideal bit size and bit size of an arbitrary point in the conversion range.

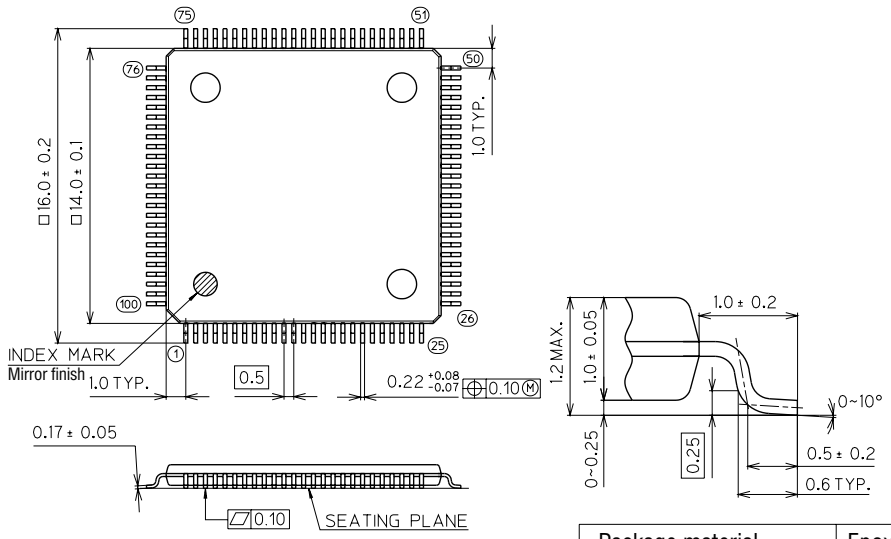
4. Zero scale error
   Zero scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 000H to 001H.

5. Full-scale error
   Full-scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 3FEH to 3FFH.

PACKAGE DIMENSIONS

(Unit : mm)

TQFP100-P-1414-0.50-K



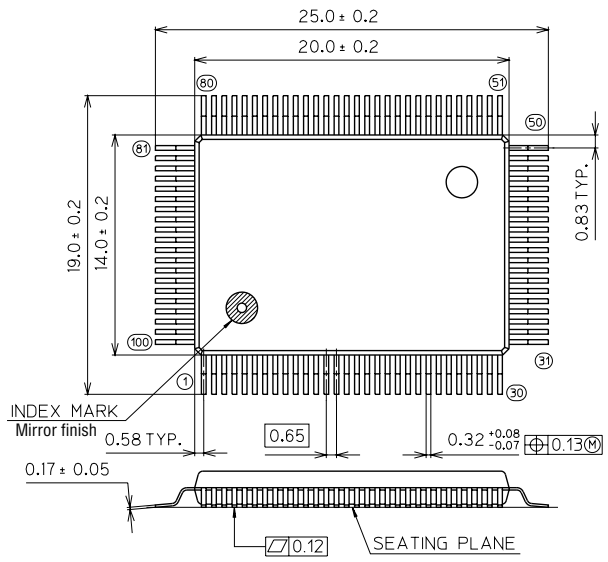
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.55 TYP.

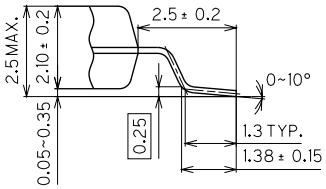
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP100-P-1420-0.65-BK





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).