# □ MN102L360C

Туре	MN102L360C				
ROM (x8-bit / x16-bit)	External				
RAM (×8-bit / ×16-bit)	5 K				
Package	LQFP128-P-1818C *Lead-free				
Minimum Instruction Execution Time	<ul> <li>• RESET • Watchdog • Timer counter 0 to 5 • Fixed-length serial ch.0,1 transmission</li> <li>• Fixed-length serial ch.0,1 reception • Timer counter 6 to 7 • Timer counter 6 to 7 compare capture A</li> <li>• Timer counter 6 to 7 compare capture B • ATC transfer finish • External 0 to 7 • Serial ch.0,1 transmission</li> <li>• Serial ch.0,1 reception • NMI pin • A/D conversion finish</li> </ul>				
Interrupts					
Timer Counter	Timer counter 0: 8-bit × 1 (timer output, event count) Clock source				
	Timer counter 1: 8-bit × 1 (timer output, even count, A/D conversion start) Clock source system clock; 1/4 of low speed clock frequency; external clock; timer counter 0 ou Interrupt source timer counter 1 underflow				
	Timer counter 2 to 3: 8-bit × 1 (timer output, event count, UART baud rate generation) Clock source system clock; external clock; timer counter 0 output; timer counter 1, 2 outp Interrupt source timer counter 2, 3 underflow				
	Timer counter 4,5: 8-bit × 1 (timer output, event count) Clock source				
	Timer counter 6, 7: 16-bit × 1 (timer output, event count, input capture, output compare, PWM output, 2-phase encoder input) Clock source system clock; external clock; timer counter 4, 5 output Interrupt source coincidence with compare capture A or at capture; coincidence with compare capture B or at capture; underflow of timer counter 6, 7				
	Connectable timer counter 0 to 5				
Serial Interface	Serial 0: 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source				
	Serial 1: 7, 8-bit × 1 (common use with UART, transfer direction of MSB/LSB selectable) Clock source				
	Fixed-length serial 0: 8-bit × 1 Clock sourceexternal clock Sending direction LSB				
	Fixed-length serial 1: 8-bit × 1 Clock source external clock				
	Sending direction LSB				

### MN102L360C

# D/A Outputs 8-bit × 2-ch. PWM 16-bit × 2-ch.

Notes

Burst ROM interface support, ATC ( between serial 0 ch and built-in RAM) support

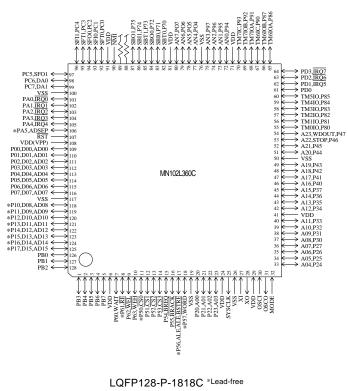
#### Electric Characteriatics

Supply current

Parameter	Symbol	Condition	Limit			Unit	
Falameter		Condition		typ	max	Unit	
Operating supply current	IDDopr	VI = VDD or VSS, output open			75	mA	
		$f=20\ MHz$ , VDD = 5.0 V			15		
Supply current at STOP	IDDS	Pin with pull-up resistor is open			50	50	
	IDDS	all other input pins and Hi-Z state input/output		50		μΑ	
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level			30	mA	
		f = 20  MHz, VDD = 5.0 V, output open					

Pin Assignment

 $(Ta = -40^{\circ}C \text{ to } +85^{\circ}C \text{ , } VDD = \text{ } 5.0 \text{ V} \text{ , } VSS = 0 \text{ V})$ 



\* Port unusable

# Support Tool

In-circuit Emulator	PX-ICE102L00 + PX-PRB102L36-LQFP128-P-1818C		
EPROM Built-in Type	Туре	MN102LP36Z	
	ROM (× 8-bit / × 16-bit)	128 K	
	RAM (× 8-bit / × 16-bit)	10 K	-
	Minimum instruction execution time	100 ns (at 4.5 V to 5.5 V, 20 MHz)	
	Package	LQFP128-P-1818C *Lead-free	

## MN102L360C

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