❑ MN102H60G , MN102H60K , MN102H60M , MN102H60R

Type	MN102H60G	MN102H60K	MN102H60M [ES (Engineering Sample) available]	MN102H60R (under development)
ROM (×8-bit)	128 K	256 K	384 K	1024 K
RAM (×8-bit)	4 K	10 K	10 K	4 K
Package	LQFP100-P-1414 *Lead-free			
Minimum Instruction Execution Time	With main clock operated	58 ns (at 3.0 V to 3.6 V, 34 MHz)		
Interrupts	• $\overline{\text{RST}}$ pin • Watchdog • $\overline{\text{NMI}}$ pin • Timer counter 0 to 7 underflow • Timer counter 8 to 12 underflow • Timer counter 8 to 12 compare capture A • Timer counter 8 to 12 compare capture B • ATC ch.0 to 3 transfer finish • ETC ch.0 to 1 transfer finish • External 0 to 4 • Serial ch.0 to 4 transmission • Serial ch.0 to 4 reception • $\overline{\text{KI}}$ pin (OR) • A/D conversion finish			
Timer Counter	Timer counter 0 : 8-bit × 1 (prescaler, timer output, event count, clock supply for 16-bit timer, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; 1/4 of system clock (XI) frequency; system clock (BOSC); TM0IO pin Interrupt source ····· underflow of timer counter 0 Timer counter 1 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source ····· underflow of timer counter 1 Timer counter 2 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source ····· underflow of timer counter 2 Timer counter 3 : 8-bit × 1 (A/D conversion start up, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0, 4 Interrupt source ····· underflow of timer counter 3 Timer counter 4 : 8-bit × 1 (prescaler, serial clock generator, timer output, event count, clock supply for 16-bit timer, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; TM4IO pin Interrupt source ····· underflow of timer counter 4 Timer counter 5 : 8-bit × 1 (serial clock generator, timer interrupts) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; system clock (BOSC) Interrupt source ····· underflow of timer counter 5 Timer counter 6 : 8-bit × 1 (timer interrupts) Clock source ····· 1/4 of system clock (XI) frequency; underflow of timer counter 0, 4 Interrupt source ····· underflow of timer counter 6 Timer counter 7 : 8-bit × 1 (timer output, event count, timer interrupts) Clock source ····· 1/4 of system clock (XI) frequency; underflow of timer counter 0; TM7IO pin Interrupt source ····· underflow of timer counter 7 (Connectable) timer counter 0 to 7 Timer counter 8 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; TM8IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM8IOA pin/TM8IOB pin (1 ×, 4 ×); TM8IC pin Interrupt source ····· underflow of timer counter 8; timer counter 8 compare capture A; timer counter 8 compare capture B			

Timer Counter (Continue)	Timer counter 9 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; TM9IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM9IOA pin/TM9IOB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 9; timer counter 9 compare capture A; timer counter 9 compare capture B Timer counter 10 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; TM10IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM10IOA pin/TM10IOB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B Timer counter 11 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; TM11IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM11IOA pin/TM11IOB pin (1 ×, 4 ×) Interrupt source ····· underflow of timer counter 11; timer counter 11 compare capture A; timer counter 11 compare capture B Timer counter 12 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source ····· underflow of timer counter 0, 4; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM12IOA pin/TM12IOB pin (1 ×, 4 ×), TM12IOB pin Interrupt source ····· underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B Timer counter 13, 14 : 8-bit × 1 (simple PWM output) Clock source ····· 1/2 of system clock (BOSC) frequency; underflow of timer counter 0 Timer counter 15 : 16-bit × 1 (pulse width measurement) Clock source ····· system clock (BOSC); 1/2 of system clock (BOSC) frequency; underflow of timer counter 0; TM15IB pin (Connectable) timer counter 13, 14
Serial Interface	Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source ····· 1/8 of timer counter 1 underflow frequency; 1/8, 1/2 of timer counter 2 underflow frequency; external pin Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source ····· 1/8 of timer counter 4 underflow frequency; 1/8, 1/2 of timer counter 5 underflow frequency; external pin Serial 4 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source ····· 1/8 of timer counter 1 underflow frequency; 1/8, 1/2 of timer counter 5 underflow frequency; external pin UART × 2 (common use with serial 3, 4) I^2C × 2 (common use with serial 3,4; single master)
I/O Pins — **I/O**	82 — • Common use : 46 (address data separate 8-bit mode) • Common use : 53 (address data multiplex 8-bit mode)
A/D Inputs	10-bit × 8-ch. (with S/H)
PWM	16-bit × 5-ch. (timer counter 8 to 12)
ICR	16-bit × 5-ch. (timer counter 8 to 12)
OCR	16-bit × 5-ch. (timer counter 8 to 12)
Notes	Address / data multiplex bus interface, address / data separate bus interface, 8-bit / 16-bit bus width selectable

See the next page for electrical characteristics, pin assignment and support tool.

Electrical Characteristics

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDDopr	VI = VDD or VSS, output open f = 34 MHz , VDD = 3.3 V			60+10α*	mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open All other input pins and Hi-Z state input/output pins are simultaneously applied VDD or VSS level f = 34 MHz , VDD = 3.3 V, output open			70	µA
Supply current at HALT	IDDH				30+10α*	mA

(Ta = –40°C to +85°C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V)

* "α" depends on products.

MN102H60G, MN102H60K, MN102H60M, MN102H60R : α = 0

MN102HF60G : α = 1

MN102HF60K : α = 2

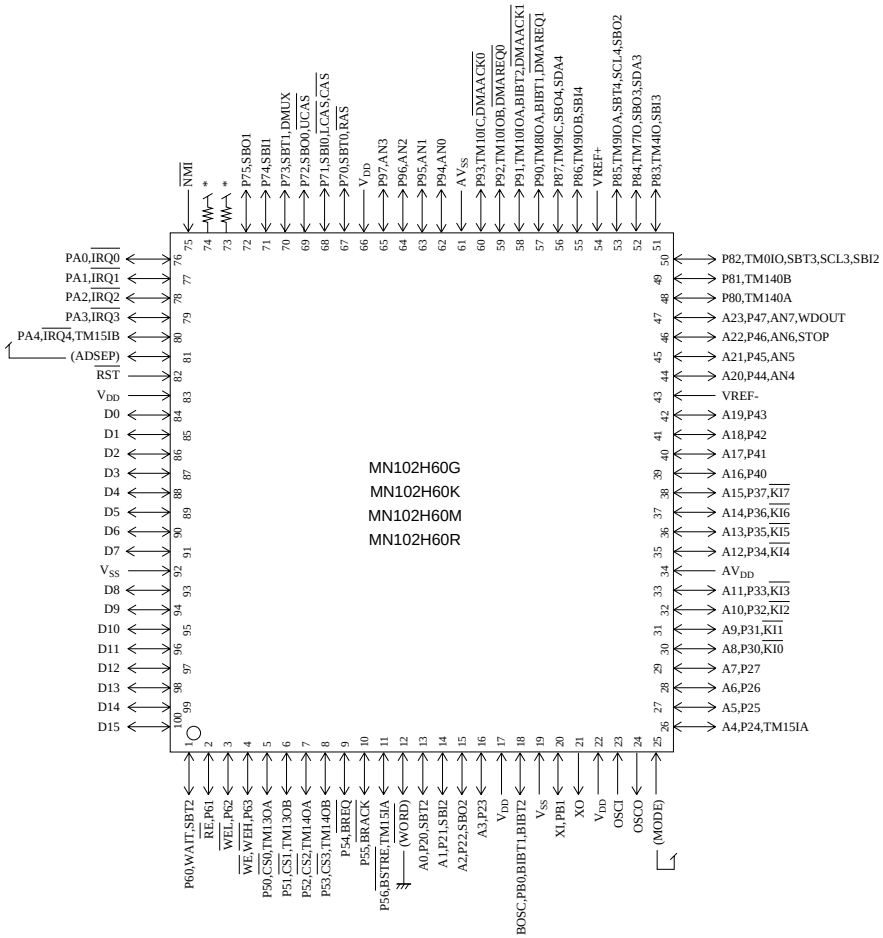
MN102HF60M : α = 3

A/D characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Non-linear error		10-bit			± 4	LSB
A/D conversion time		at 34 MHz	3.29			µs
Analog input voltage	VIA		VSS		VDD	V

(Ta = 25°C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V)

Pin Assignment



LQFP100-P-1414 *Lead-free

* Use 33 kΩ to 50 kΩ.

* Pin position in 16-bit bus width address data split memory extension mode.

Support Tool

In-circuit Emulator	PX-ICE102H60-LQFP100-P-1414	Not applicable to MN102H60R. Use in the same way as mentioned in Note) of a flash memory built-in version.
Flash Memory Built-in Type	Type	MN102HF60G, MN102HF60K, MN102HF60M (under development)
	ROM (× 8-bit)	128 K / 256 K / 384 K
	RAM (× 8-bit)	4 K / 10 K / 10 K
	Minimum instruction execution time	58 ns (at 3.0 V to 3.6 V, 34 MHz)
	Package	LQFP100-P-1414 *Lead-free

Note: This system does not support the MN102H60R flash memory built-in type; instead, use the MN102HF60G + external flash.

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