I²C BUS Control 5-Input 2-Output AV Switch
Monolithic IC MM1313

Outline

This IC is a 5-input 2-output AV switch with I²C control, developed for use in televisions. Two outputs enable it to support two screens or "picture-in-picture".

Features

1. Serial control by I²C bus.
2. 5-inputs, 2-outputs.
3. Video and audio system switches can be controlled independently.
4. 6dB amplifier built in to video system.
5. Built-in Y/C MIX circuit.
6. Slave address can be changed : 90H or 92H.
7. Audio muting possible by external pin.
8. Maintains high impedance even when I²C BUS line (SDA, SCL) power supply is off.
9. Built-in 3 value discrimination function.
10. On-chip power ON reset function.
11. Two types of audio input impedance : 60kΩ and 30kΩ.
    MM1313AD : 60kΩ MM1313BD : 30kΩ
12. Supports 2-screen or P-IN-P TV.

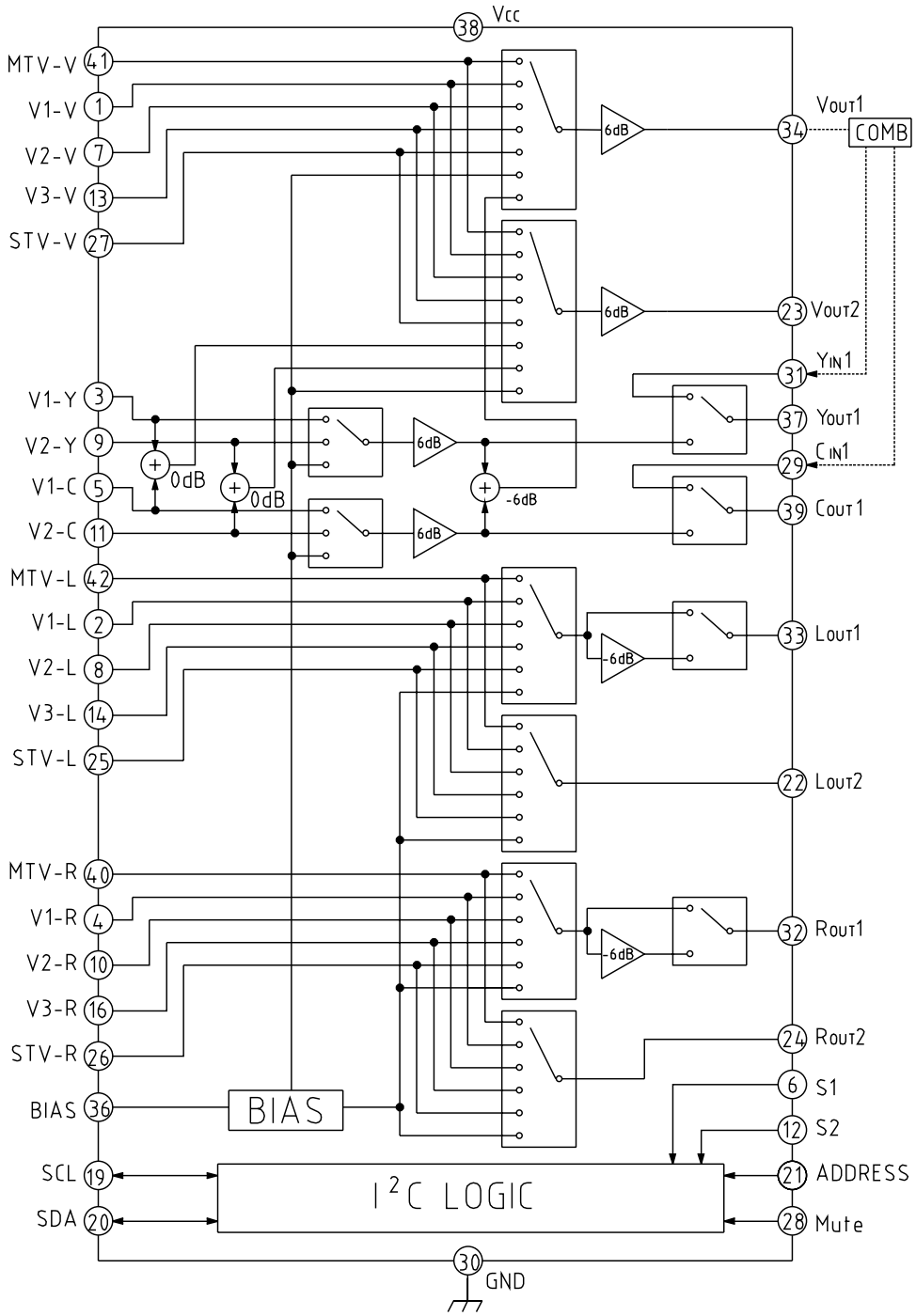
Package

SDIP-42A (MM1313AD, MM1313BD)

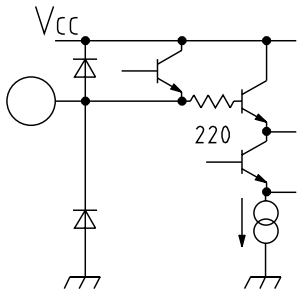
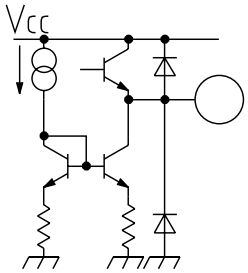
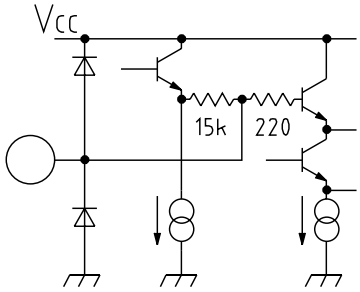
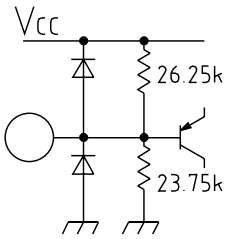
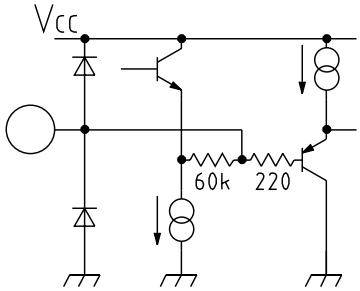
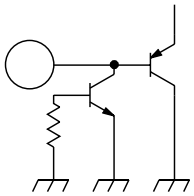
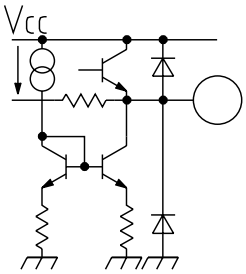
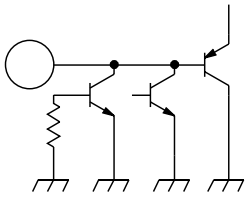
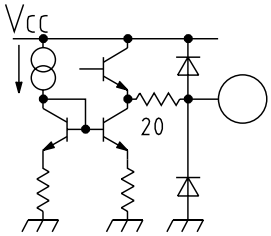
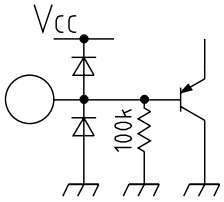
Applications

1. Televisions
2. Other video equipment

Equivalent Block Diagram



Pin Function

Pin No.	Name	Internal equivalent circuit diagram	Pin No.	Name	Internal equivalent circuit diagram
41 1 7 13 27 3 9 31	MTV–V V1–V V2–V V3–V STV–V V1–Y V2–Y YIN1		33 22 32 24	LOUT1 LOUT2 ROUT1 ROUT2	
5 11 29	V1–C V2–C CIN1		36	BIAS	
42 2 8 14 25 40 4 10 16 26	MTV–L V1–L V2–L V3–L STV–L MTV–R V1–R V2–R V3–R STV–R		19	SCL	
34 23	VOUT1 VOUT2		20	SDA	
37 39	YOUT1 COUT1		6 12 21 28	S1 S2 ADR Mute	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	−40~+125	°C
Operating temperature	T_{OPR}	−20~+75	°C
Power supply voltage	V_{CC}	12	V
Allowable power dissipation	Pd	850	mW

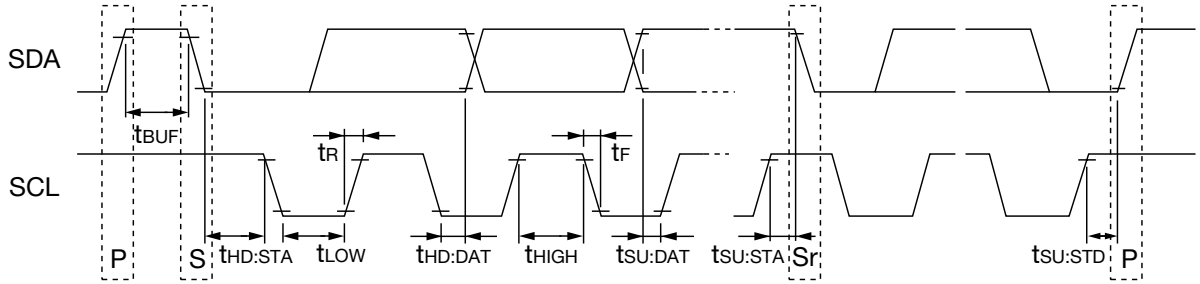
Electrical Characteristics (Ta=25°C, V_{CC}=9V)

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Operating power supply voltage	V_{CC}			8	9	10	V
Current consumption	I_{CC}	38	V_{CC}=9V, no signal, no load		40	52	mA
V_{OUT}1 output							
Voltage gain	G_{V}1	TP1	Sine wave 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F_{V}1	TP1	Sine wave 1.0V_{P-P}, 10MHz/100kHz	−1.0	0	1.0	dB
Differential gain	DG_{V}1	TP1	Vn-V : Staircase 1V_{P-P} APL=10~90% Vn-Y : Staircase (luminance signal) 1V_{P-P} Vn-C : Chroma signal 0.3V_{P-P} APL=10~90%	−3	0	3	%
Differential phase	DP_{V}1	TP1	Vn-V : Staircase 1V_{P-P} APL=10~90% Vn-Y : Staircase (luminance signal) 1V_{P-P} Vn-C : Chroma signal 0.3V_{P-P} APL=10~90%	−3	0	3	deg
Input dynamic range	D_{V}1	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V_{P-P}
V_{OUT}2 output							
Voltage gain	G_{V}2	TP6	Sine wave 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F_{V}2	TP6	Sine wave 1.0V_{P-P} 10MHz/100kHz	−1.0	0	1.0	dB
Differential gain	DG_{V}2	TP6	Vn-V : Staircase 1V_{P-P} APL=10~90% Vn-Y : Staircase (luminance signal) 1V_{P-P} Vn-C : Chroma signal 0.3V_{P-P} APL=10~90%	−3	0	3	%
Differential phase	DP_{V}2	TP6	Vn-V : Staircase 1V_{P-P} APL=10~90% Vn-Y : Staircase (luminance signal) 1V_{P-P} Vn-C : Chroma signal 0.3V_{P-P} APL=10~90%	−3	0	3	deg
Input dynamic range	D_{V}2	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V_{P-P}
Y_{OUT}1 output							
Voltage gain	G_{Y}1	TP2	Vn-Y : Sine wave 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
	G_{Y}2	TP2	Y_{IN}1 : Sine wave 2.0V_{P-P}, 100kHz	−0.5	0	0.5	
Frequency characteristics	F_{Y}1	TP2	Vn−Y : Sine wave 1.0V_{P-P} 10MHz/100kHz	−1.0	0	1.0	dB
	F_{Y}2	TP2	Y_{IN}1 : Staircase 2.0V_{P-P} 10MHz/100kHz	−1.0	0	1.0	
Differential gain	DG_{Y}	TP2	Vn-Y : Staircase 1V_{P-P} APL=10~90% Y_{IN}1: Staircase 2V_{P-P} APL=10~90%	−3	0	3	%
Differential phase	DP_{Y}	TP2	Vn-Y : Staircase 1V_{P-P} APL=10~90% Y_{IN}1 : Staircase 2V_{P-P} APL=10~90%	−3	0	3	deg

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Input dynamic range	D_{Y1}	SG2	Vn-Y : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V_{P-P}
	D_{Y2}	SG4	V_{IN1} : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	3.2	3.8		
Output impedance	Z_{OYC1}				50		Ω
C_{OUT1} output							
Voltage gain	G_{C1}	TP3	Vn-C : Sine wave 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
	G_{C2}	TP3	C_{IN1} : Sine wave 2.0V_{P-P}, 100kHz	–0.5	0	0.5	
Frequency characteristics	F_{C1}	TP3	Vn–C : Sine wave 1.0V_{P-P} 10MHz/100kHz	–1.0	0	1.0	dB
	F_{C2}	TP3	C_{IN1} : Sine wave 2.0V_{P-P} 10MHz/100kHz	–1.0	0	1.0	
Differential gain	DG_C	TP3	C_{IN1} : Staircase 2V_{P-P} APL=10~90%	–3	0	3	%
Differential phase	DP_C	TP3	C_{IN1} : Staircase 2V_{P-P} APL=10~90%	–3	0	3	deg
Input dynamic range	D_{C1}	SG3	Vn-C : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	2.75	3.25		V_{P-P}
	D_{C2}	SG5	C_{IN1}: Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	5.5	6.5		
Input impedance	Z_{IC}		Vn–C, C_{IN1}	10	15	20	kΩ
Output impedance	Z_{OC1}				50		Ω
L_{OUT1} output							
Voltage gain	G_{L11}	TP4	b7=0, Sine wave 2.5V_{P-P}, 1kHz	–6.5	–6.0	–5.5	dB
	G_{L12}	TP4	b7=1, Sine wave 2.5V_{P-P}, 1kHz	–0.5	0.0	0.5	
Frequency characteristics	F_{L1}	TP4	Sine wave 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THD_{L1}	TP4	Sine wave 2.5V_{P-P}, 1kHz		0.03	0.1	%
Input dynamic range	D_{L1}	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	V_{OFFL1}	33	L_{OUT1} pin DC difference during SW switching		0	±15	mV
Input impedance	Z_{IL1}			42	60	78	kΩ
Output impedance	Z_{OL1}				120		Ω
L_{OUT2} output							
Voltage gain	G_{L2}	TP7	Sine wave 2.5V_{P-P}, 1kHz	–0.5	0.0	0.5	dB
Frequency characteristics	F_{L2}	TP7	Sine wave 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THD_{L2}	TP7	Sine wave 2.5V_{P-P}, 1kHz		0.03	0.1	%
Input dynamic range	D_{L2}	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	V_{OFFL2}	22	L_{OUT2} pin DC difference during SW switching		0	±15	mV
Output impedance	Z_{OL2}				120		Ω
R_{OUT1} output							
Voltage gain	G_{R11}	TP5	b7=0, Sine wave 2.5V_{P-P}, 1kHz	–6.5	–6.0	–5.5	dB
	G_{R12}	TP5	b7=1, Sine wave 2.5V_{P-P}, 1kHz	–0.5	0.0	0.5	
Frequency characteristics	F_{R1}	TP5	Sine wave 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THD_{R1}	TP5	Sine wave 2.5V_{P-P}, 1kHz		0.03	0.1	%
Input dynamic range	D_{R1}	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	V_{OFFR1}	32	R_{OUT1} pin DC difference during SW switching		0	±15	mV
Input impedance	Z_{IR1}			42	60	78	kΩ
Output impedance	Z_{OR1}				120		Ω

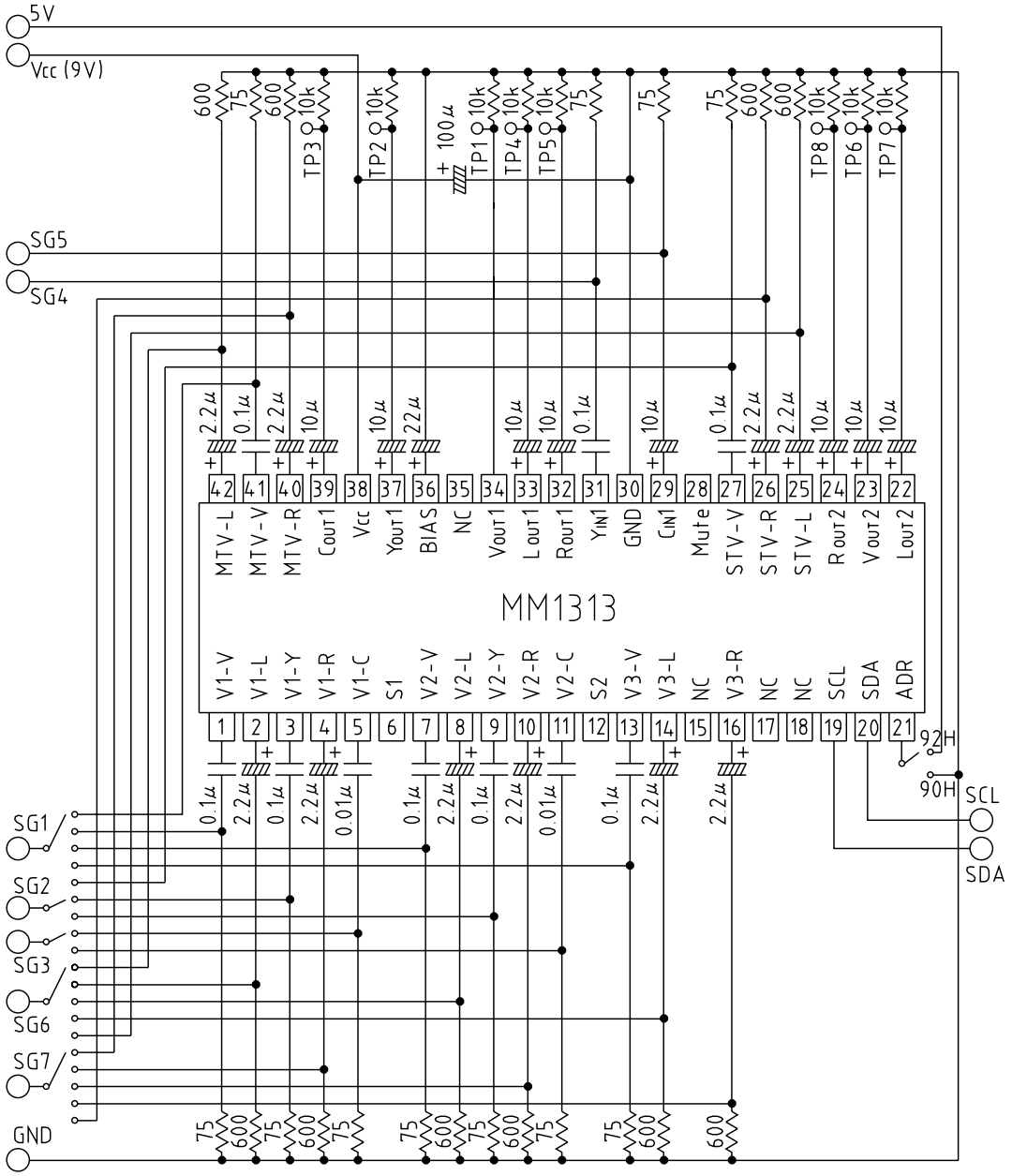
Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
ROUT2 output							
Voltage gain	GR2	TP8	Sine wave 2.5VP-P, 1kHz	–0.5	0.0	0.5	dB
Frequency characteristics	FR2	TP8	Sine wave 2.5VP-P, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THDR2	TP8	Sine wave 2.5VP-P, 1kHz		0.03	0.1	%
Input dynamic range	DR2	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	VOFFR2	24	ROUT2 pin DC difference during switching		0	±15	mV
Output impedance	ZOR2				120		Ω
Crosswalk							
VOUT 1	CTV1	TP1	Measurement Circuit Figure 2 for SG1 input : 4.43MHz, 1VP-P for SG2 input : 4.43MHz, 0.5VP-P		–60	–53	dB
VOUT 2	CTV2	TP2			–60	–53	dB
YOUT 1	CTY1	TP3			–60	–53	dB
COUT 1	CTC1	TP6			–60	–53	dB
LOUT 1	CTL1	TP4	Measurement Circuit Figure 2 1kHz, 2.5VP-P		–90	–80	dB
LOUT 2	CTL2	TP5			–90	–80	dB
ROUT 1	CTR1	TP7			–90	–80	dB
ROUT 2	CTR2	TP8			–90	–80	dB
Video I/O Pin Voltage							
Input pin voltage	VVIP		No signal, no load	4.6	4.9	5.2	V
Output pin voltage	VVOP		VOUT1 pin, VOUT2 pin No signal, no load	4.1	4.4	4.7	V
	VSOP		YOUT1 pin, COUT1 pin No signal, no load	3.3	3.6	3.9	V
Audio I/O Pin Voltage							
Input pin voltage	VAIP		No signal, no load	4.0	4.3	4.6	V
Output pin voltage	VAOP		No signal, no load	3.9	4.2	4.5	V
Logic section (Refer to figure below)							
Input voltage L	VIL		I²C logic low level discrimination value	0.0		1.5	V
Input voltage H	VIH		I²Clogic high level discrimination value	3.0		5.0	V
Low level output voltage (SDA)	VOL		SDA for 3mA inflow	0.0		0.4	V
High level input current	IIH		when SDA, SCL=4.5V impressed	–10		+10	µA
Low level input current	IIL		when SDA, SCL=0.4V impressed	–10		+10	µA
Clock frequency	fSCL					100	kHz
Data transmission waiting time	tBUF			4.7			µS
SCL start hold time	tHD;STA			4.0			µS
SCL low level hold time	tLOW			4.7			µS
SCL high level hold time	tHIGH			4.0			µS
SCL start set-up time	tSU;STA			4.7			µS
SDA data hold time	tHD;DAT			200			nS
SDA data set-up time	tSD;DAT			250			nS
SCL rise time	tR					1000	nS
SCL fall time	tF					300	nS
SCL stop set-up time	tSU;STO			4.0			µS

I²C BUS BUS Control Signal

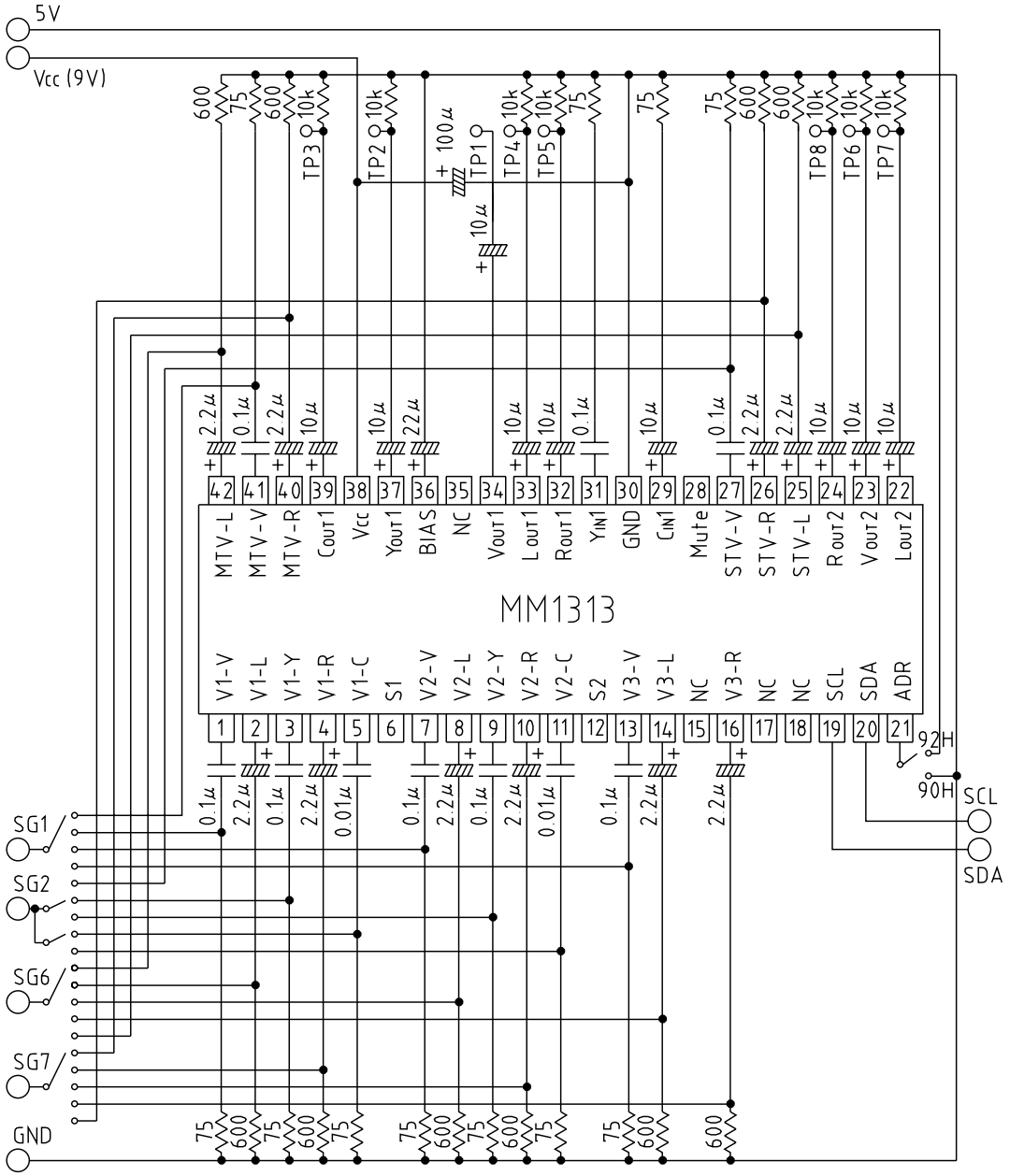


Measurement Circuit

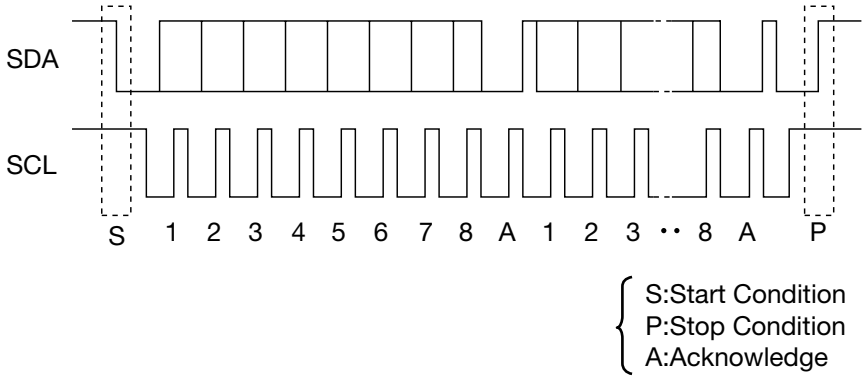
Measurement Circuit 1



Measurement Circuit 2 (Crosstalk measurement)



I²C BUS



The I²C BUS is a BUS system developed by Philips for internal use in equipment. Data transmission is carried out by the two SDA and SCL lines, in byte units, with the MSB first from start condition.

[Control Register]

The control register contains data sent from the master in order to determine the status of each switch.

S	Slave address							R/W	A	Control register 1								A	Control register 2								A	P
	1	0	0	1	0	0	0/1	0		b7	b6	b5	b4	b3	b2	b1	b0		b7	b6	b5	b4	b3	b2	b1	b0		
	Address byte									Control data																		

The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 0 when using as a control register.

The MM1313 slave address can be selected as 90H/92H depending on the status of the ADR pin. When ADR pin is low it is 90H.

The relationship between the control register bits and switch control is as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
Audio Gain	S/Comp Select	Video–Select			Audio–Select		

The control register bits are reset to 0 when power is applied.

MM1313 control is carried out by the 3-byte structure of the 1 address byte and 2 control data bytes. The first byte in the control data is control data for output 1, and the remaining 1 byte is control data for output 2.

All of the remaining data (fourth byte and after) are ignored.

Refer to the separate tables for details on switch control.

[Status Register]

The status register contains data for sending device status to the master.

S	Slave address							R/W	A	Status register								NA	P
	1	0	0	1	0	0	0/1	1		b7	b6	b5	b4	b3	b2	b1	b0		
	Address byte									Status data									

The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 1 when using as a status register.

The MM1313 slave address can be selected as 91H/93H depending on the status of the ADR pin. When the ADR pin is low it is 91H. However, the confirmation response after completion of the status register should be non-acknowledge.

The status register output data as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
P-ON RESET	×	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL	×	×

P-ON RESET : Returns 1 for power on reset. However once data read begins, 0 is returned next.
S1/S2 OPEN : Returns 0 when the S1/S2 pin is not open, and returns 1 when the S1/S2 pin is open
S1/S2 SEL : Returns 0 when the S1/S2 pin is not grounded, and returns 1 when the S1/S2 pin is grounded.

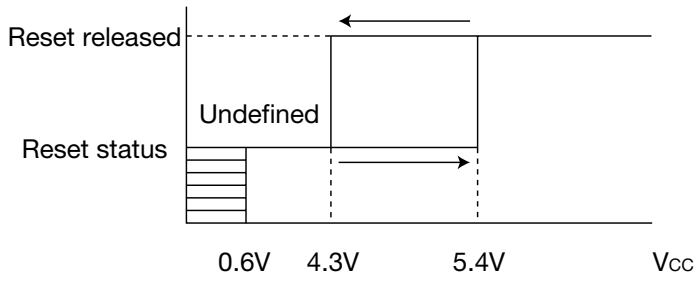
S1/S2 OPEN, SEL have 3-value discrimination, and the combinations are as shown below.

S1/S2 pin DC voltage	S1/S2 OPEN	S1/S2 SEL
0.8V or less	0	1
1.3V or more, 3.5V or less	0	0
4.5V or more	1	0

[Power On Reset]

Power on reset is built in to reset each control register to 0 when power is turned on.

Power on reset threshold has hysteresis as shown in the figure below. The IC power on reset status can be discriminated by reading the status register P-ON RESET.



Switch Control Table

1. Video Output 1

b6	b5	b4	b3	VOUT1	YOUT1	COUT1
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV–V	YIN1	CIN1
0	0	1	0	V1–V	YIN1	CIN1
0	0	1	1	V2–V	YIN1	CIN1
0	1	0	0	V3–V	YIN1	CIN1
0	1	0	1	STV–V	YIN1	CIN1
0	1	1	0	Mute	Mute	Mute
		1	1			
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV–V	YIN1	CIN1
1	0	1	0	V1–Y+C	V1–Y	V1–C
1	0	1	1	V2–Y+C	V2–Y	V2–C
1	1	0	0	V3–V	YIN1	CIN1
1	1	0	1	STV–V	YIN1	CIN1
1	1	1	0	Mute	Mute	Mute
		1	1			

2. Video Output 2

b6	b5	b4	b3	VOUT2
0	0	0	0	Mute
0	0	0	1	MTV–V
0	0	1	0	V1–V
0	0	1	1	V2–V
0	1	0	0	V3–V
0	1	0	1	STV–V
0	1	1	0	Mute
		1	1	
1	0	0	0	Mute
1	0	0	1	MTV–V
1	0	1	0	V1–Y+C
1	0	1	1	V2–Y+C
1	1	0	0	V3–V
1	1	0	1	STV–V
1	1	1	0	Mute
		1	1	

3. Audio Output 1

Mute pin	b2	b1	b0	LOUT1	ROUT1
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV–L	MTV–R
	0	1	0	V1–L	V1–R
	0	1	1	V2–L	V2–R
	1	0	0	V3–L	V3–R
	1	0	1	STV–L	STV–R
	1	1	0	Mute	Mute
		1	1		
3.0V or more	–	–	–	Mute	Mute

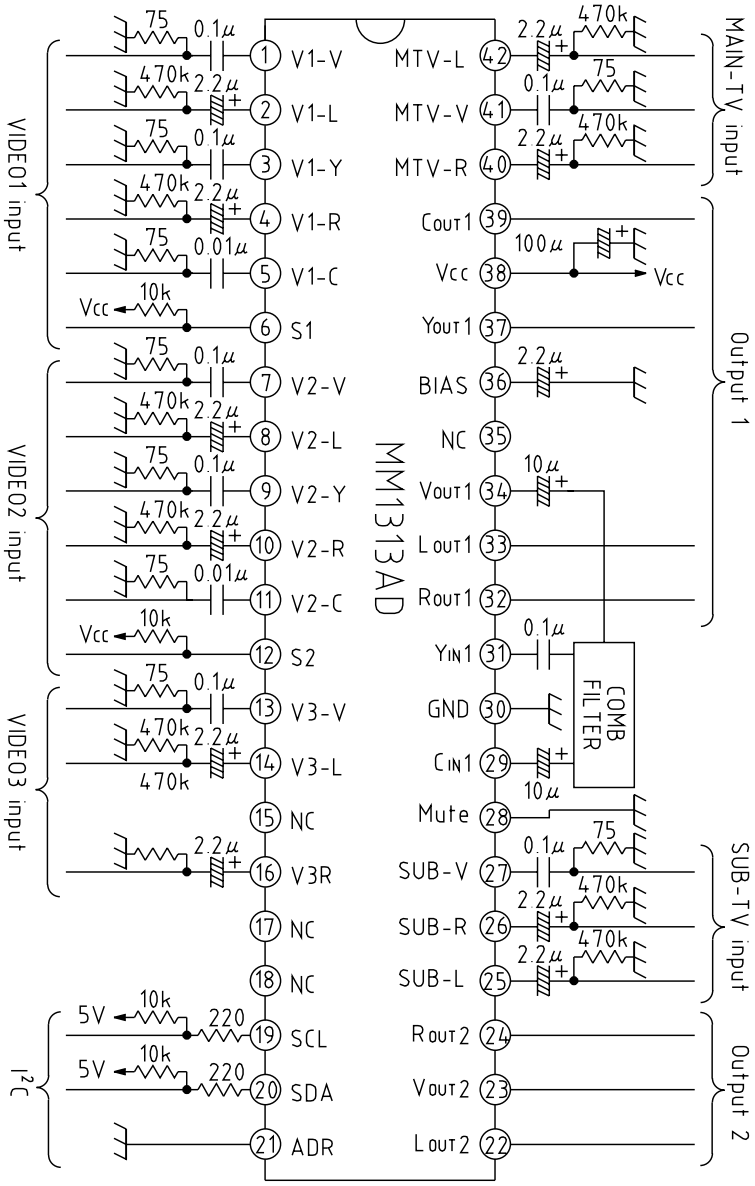
4. Audio Output 1 Gain Switching

b7	Output gain
0	–6dB output
1	0dB output

5. Audio Output 2

Mute pin	b2	b1	b0	LOUT2	ROUT2
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV–L	MTV–R
	0	1	0	V1–L	V1–R
	0	1	1	V2–L	V2–R
	1	0	0	V3–L	V3–R
	1	0	1	STV–L	STV–R
	1	1	0	Mute	Mute
		1	1		
3.0V or more	–	–	–	Mute	Mute

Application Circuit



Notes

1. VOUT is set at 4.4V and CIN at 4.9V
   Please note that capacitance polarity may vary depending on comb filter bias.
2. Each audio output can be muted by making pin 19 high. Mute is off when it is open or low.