MK3727

LOW COST 24 TO 36 MHZ 3.3 VOLT VCXO

Description

The MK3727 series of devices include the original MK3727S, and the new MK3727C and MK3727D. The MK3727D and MK3727C are drop-in replacements for the MK3727S device. Compared to these earlier devices, the MK3727D and MK3727C offer a wider operating frequency range and improved power supply noise rejection. The MK3727D is recommended for new designs.

The MK3727 series combines the functions of a VCXO (Voltage Controlled Crystal Oscillator) and PLL (Phase Locked Loop) frequency doubler onto a single chip. Used in conjunction with an external pullable quartz crystal, this monolithic integrated circuit replaces more costly hybrid (canned) VCXO devices. The MK3727 is designed primarily for data and clock recovery applications within end products such as ADSL modems, set-top box receivers, and telecom systems.

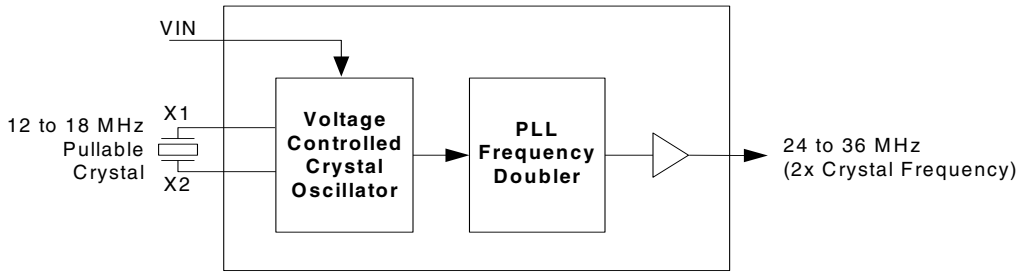
The MK3727D is recommended for new designs. The MK3727D exhibits a moderate VCXO gain of 120ppm/V typical, when used with a high quality external pullable quartz crystal. The MK3727C offers a higher VCXO gain of 150ppm/V. The higher intrinsic VCXO gain of the MK3727C may help compensate for the reduced pullability of a low quality crystal used in some applications. However, higher VCXO gain may also increase clock output phase noise.

The frequency of the on-chip VCXO is adjusted by an external control voltage input into pin VIN. Because VIN is a high impedance input, it can be driven directly from an PWM RC integrator circuit. Frequency output increases with VIN voltage input. The usable range of VIN is 0 to 3 V.

Features

- MK3727D and MK3727C are drop-in upgrades to the earlier MK3727S device
- MK3727D and MK3727C offer 24 to 36 MHz output frequency range (output frequency = 2x crystal frequency) and improved power supply noise rejection
- Uses an inexpensive 12 to 18 MHz external crystal
- Ideal for ADSL applications using 17.664 MHz external pullable crystal to generate locked 35.328 MHz clock physical layer clock
- Ideal for set-top box applications using 13.5 MHz external pullable crystal to generate lock 27 MHz clock transport video clock
- On-chip VCXO with guaranteed pull range of ±115 ppm minimum (MK3727D)
- VCXO input tuning voltage 0 to 3.3 V
- Packaged in 8-pin SOIC (150 mil wide)
- MK3727D available in Pb-free packaging
- **MK3727D is recommended for new designs.**

Block Diagram



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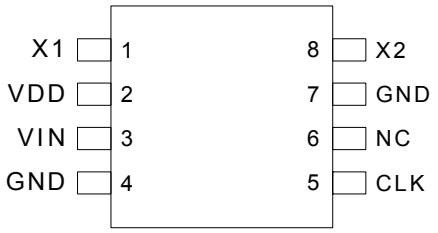
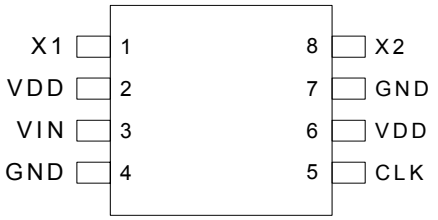
Pin Assignment



MK3727C
MK3727D

8-Pin (150 mil) SOIC



MK3727S

8-Pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	XI	Input	Crystal connection — Connect to the external pullable crystal.
2	VDD	Power	Connect to +3.3 V (0.01uf decoupling capacitor recommended)
3	VIN	Input	Voltage input to VCXO — 0 to 3.3 V analog input which controls the oscillation frequency of the VCXO.
4	GND	Power	Connect to ground
5	CLK	Output	Clock output
6 (3727C/D)	NC	—	No internal connection (may connect to ground or VDD)
6 (3727S)	VDD	Power	Connect to VDD
7	GND	Power	Connect to ground
8	X2	Input	Crystal connection — Connect to the external pullable crystal.

External Component Selection

The MK3727 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD (pin 2) and GND (pin 4 & 7), as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output (CLK, pin 5) and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Quartz Crystal

The MK3727 VCXO function consists of the external crystal and the integrated VCXO oscillator circuit. To assure the best system performance (frequency pull range) and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the following section shown must be followed.

The frequency of oscillation of a quartz crystal is determined by its "cut" and by the load capacitors connected to it. The MK3727 incorporates on-chip variable load capacitors that "pull" (change) the frequency of the crystal. The crystal specified for use with the MK3727 is designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF.

Recommended Crystal Parameters:

Initial Accuracy at 25°C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm
Load Capacitance	14 pf
Shunt Capacitance, C0	7 pF Max
C0/C1 Ratio	250 Max
Equivalent Series Resistance	35Ω Max

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the MK3727. There should be no vias between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

Crystal Tuning Load Capacitors

The crystal traces should include pads for small fixed capacitors, one between X1 and ground, and another between X2 and ground. The need for these capacitors is determined at system prototype evaluation, and is influenced by the particular crystal used (manufacture and frequency) and by PCB layout. The typical required capacitor value is 1 to 4 pF.

The procedure for determining the value of these capacitors can be found in application note MAN05.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK3727. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

VDD=3.3 V ±5% , Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	Output = 27 MHz, no load		10		mA
Short Circuit Current	I_{OS}			±50		mA
VIN, VCXO Control Voltage	V_{IA}		0		3.3	V

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency							
	MK3727D and MK3727C	F_O	VCXO Crystal frequency = 1/2 Output	24		36	MHz
	MK3727S	F_O	VCXO Crystal frequency = 13.5 MHz		27		MHz
Crystal Pullability							
	MK3727D and MK3727C	F_P	0V≤ VIN ≤ 3.3 V, Note 1	± 115			ppm
	MK3727S	F_P	0V≤ VIN ≤ 3.3 V, Note 1	± 100			ppm
VCXO Gain							
	MK3727D		VIN = VDD/2 ± 1 V, Note 1		120		ppm/V
	MK3727C		VIN = VDD/2 ± 1 V, Note 1		150		ppm/V
	MK3727S		VIN = VDD/2 ± 1 V, Note 1		100		ppm/V
Output Rise Time		t_{OR}	0.8 to 2.0 V, C_L=15 pF			1.5	ns
Output Fall Time		t_{OF}	2.0 to 0.8 V, C_L=15 pF			1.5	ns
Output Clock Duty Cycle		t_D	Measured at 1.4 V, C_L=15 pF	45	50	55	%
Maximum Output Jitter, short term		t_J	C_L=15 pF		100		ps

Note 1: External crystal device must conform with Pullable Crystal Specifications listed on page 3.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

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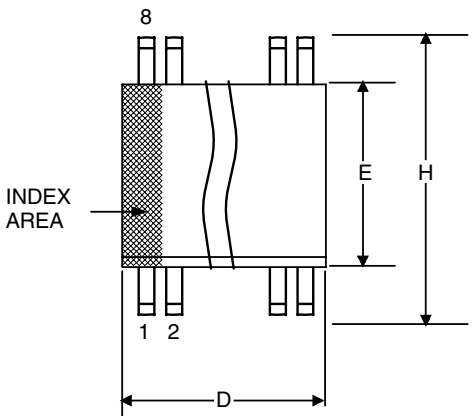
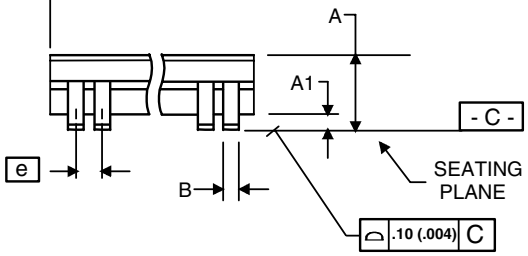
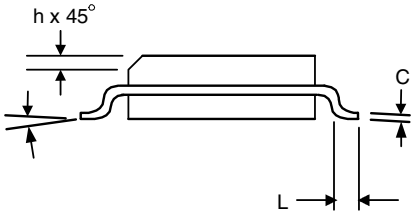
Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°





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Ordering Information

Part / Order Number (Note 1)	Marking	Shipping Packaging	Package	Temperature
MK3727D	MK3727D	Tubes	8-pin SOIC	0 to +70° C
MK3727DTR	MK3727D	Tape and Reel	8-pin SOIC	0 to +70° C
MK3727DLF	3727DLF	Tubes	8-pin SOIC	0 to +70° C
MK3727DLFTR	3727DLF	Tape and Reel	8-pin SOIC	0 to +70° C
MK3727C	MK3727C	Tubes	8-pin SOIC	0 to +70° C
MK3727CTR	MK3727C	Tape and Reel	8-pin SOIC	0 to +70° C
MK3727S	MK3727S	Tubes	8-pin SOIC	0 to +70° C
MK3727STR	MK3727S	Tape and Reel	8-pin SOIC	0 to +70° C
MK3727SLF	3727SLF	Tubes	8-pin SOIC	0 to +70° C
MK3727SLFTR	3727SLF	Tape and Reel	8-pin SOIC	0 to +70° C
MK3727D-DPK	—	Tested die in waffle pack		0 to +70° C

“LF” denotes Pb (lead) free package.

Note 1: MK3727D is recommended for new designs.