Features

- **High Speed - 180 ps Gate Delay - 2 Input NAND, FO = 2 (nominal)**
- **Up to 1.198M Used Gates and 512 Pads with 3.3V, 3V and 2.5V Libraries when Tested to Space Quality Grades**
- **Up to 1.6M Used Gates and 596 Pads with 3.3V, 3V and 2.5V Libraries when Tested to Military Quality Grades**
- **System Level Integration Technology Cores on Request:**
  - **Memory: SRAMs and TPRAMs; Gate Level or Embedded, with EDACS**
- **I/O Interfaces:**
  - **5V Tolerant/Compliant (S) or 3V (R) Matrix Options**
  - **CMOS, LVTTL, LVDS, PCI, USB, etc.**
  - **Output Currents Programmable from 2 to 24 mA, by Step of 2 mA**
  - **Cold Sparing Buffers (2 µA Max. Leakage Current at 3.6V Worst Case Mil Temp.)**
- **250 MHz PLL (on request), 220 MHz LVDS and 800 MHz Max. Toggle Frequency at 3.3V**
- **Deep Submicron CAD Flow**
- **Latch-up Immune, 200K rads Total Dose Capability, SEU Free Cells and 4000V ESD Protection**
- **QML Q and V with SMD 5962-01B01**

Description

The MH1RT Series Gate Array and Embedded Array families from Atmel are fabricated on a radiation tolerant 0.35 micron CMOS process, with up to 4 levels of metal for interconnect. This family features arrays with up to 1.6 million routable gates and 596 pads. The high density and high pin count capabilities of the MH1RT family, coupled with the ability to embed cores or memory on the same silicon, makes the MH1RT series of arrays an ideal choice for System Level Integration.

The MH1RT series is supported by an advanced software environment based on industry standards linking proprietary and commercial tools. Verilog®, DFT®, Synopsys® and Vital are the reference front end tools. The Cadence® 'Logic Design Planner' floor planning associated with timing driven layout provides an efficient back end cycle.

The MH1RT series comes as a dual use of the MH1 series, adding:

- through process changes, the 100 MeV latch-up immunity and the 200K rads+ total dose capability as required by most space programs

- through cells relayout, an SEU immunity allowing to SEU harden only where it is necessary with respect to function requirements

With a background of 15 years experience, the MH1RT series comes as the Atmel 7th generation of ASIC series designed for radiation hardened applications.

Rad Hard 1.6M Used Gates 0.35 µm CMOS Sea of Gates/ Embedded Array

MH1RT

Rev. 4110F–AERO–06/02

Table 1. MH1RT Array Organization

Device Number	Max. Sites Count	4 LM Routable Gates (Typ)	Max. Pad Count	Max. I/O Count	Gate Speed[1]
MH1099E	921,000	519,000	332	324	180 ps
MH1156E	1,452,000	764,000	412	404	180 ps
MH1242E	2,275,000	1,198,000	512	504	180 ps
MH1332E[2]	3,105,000	1,634,000	596	588	180 ps

Notes: 1. Nominal 2 Input NAND Gate FO = 2 at 3.3V.
2. Available only when tested to mil quality grades.

Design

Design Systems Supported

Atmel supports several major software systems for design with complete macro cell libraries, as well as utilities for checking the netlist and estimated pre-route delay simulations.

The following design systems are supported:

Table 2. Supported design systems

System	Available/Planned Tools
Cadence	Pearl® - Static Path Verilog-XL® - Verilog Simulator Logic Design Planner™ - Floorplanner BuildGates® - Synthesis (Ambit)
Mentor/Model Tech	Modelsim Verilog and VHDL (VITAL) Simulator Leonardo Spectrum™ - Synthesis Velocity - Static Path DFT- Scan insertion and ATPG, BIST
Synopsys®	Design Compiler™ - Synthesis Test Compiler™ - Scan Insertion and ATPG TestGen™ - Scan Insertion and ATPG Primetime® - Static Path

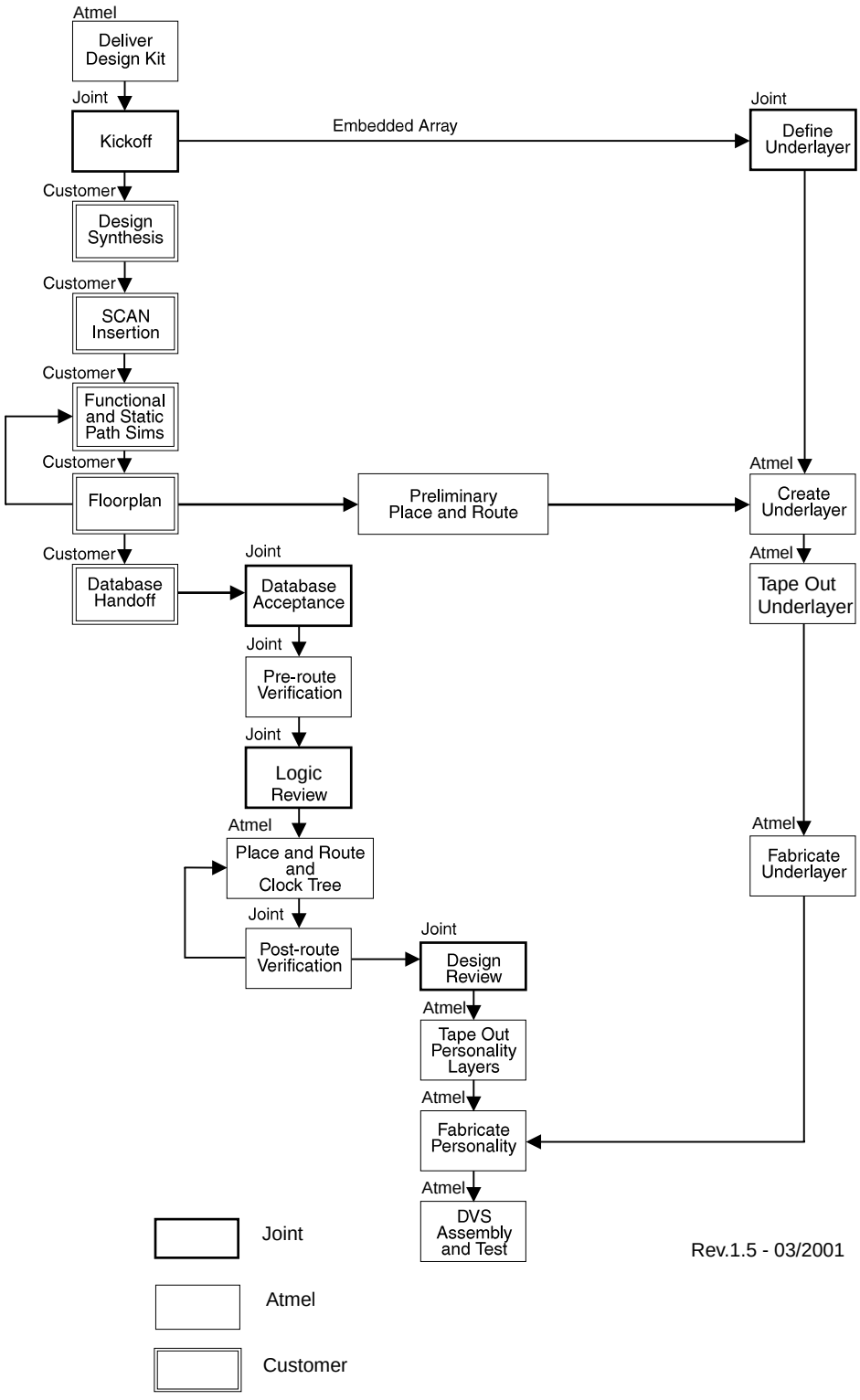
Design Flow and Tools

Atmel's design flow for Gate Arrays/Embedded Arrays is structured to allow the designer to consolidate the greatest number of system components possible onto the same silicon chip, using available third party design tools. Atmel's cell library reflects silicon performance over extremes of temperature, voltage, and process, and includes the effects of metal loading, inter-level capacitance, and edge rise and fall times. The Design Flow includes clock tree synthesis to customer specified skew and latency goals. RC extraction is performed on final design database and incorporated into the timing analysis.

The Typical Gate Array/Embedded Array Design Flow, shown on page 4, provides a pictorial description of the typical interaction between Atmel's Gate Array/Embedded Array design staff and the customer. Atmel will deliver design kits to support the customer's synthesis, verification, floorplanning, and SCAN insertion activities. Tools such as Synopsys, Cadence, Verilog-HDL and CTgen™ are used, and many others are available. Should a design include embedded memory or an embedded core, Atmel will support a design review with the customer. The purpose of the design review is to permit Atmel to understand the partition of the Gate Array/Embedded Array, and define the location of the memory blocks and/or cores so that an underlayer layout model can be created.

Following a Preliminary Design Review, the design is routed, and post-route RC data is extracted. Following post-route verification and a Final Design Review, the design is taped out for fabrication.

Figure 1. Typical Gate Array/Embedded Array Design Flow



Pin Definition Requirements

The corner pads are reserved for Power and Ground only. All other pads are fully programmable as Input, Output, Bidirectional, Power or Ground. When implementing a design with 5V tolerant buffers, one buffer site must be reserved for the V_{DD5} pin, which is used to distribute power to the buffers.

Figure 2. Gate Array

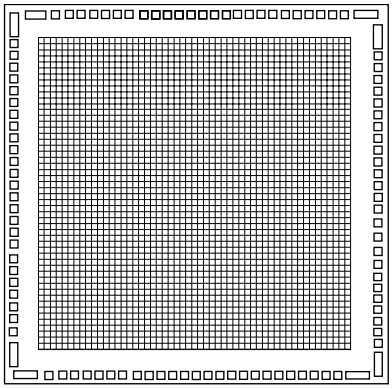
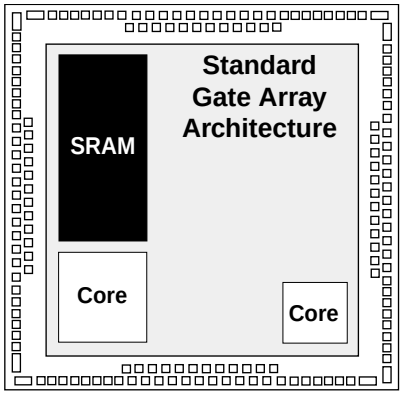


Figure 3. Embedded Array



I/O Site: Pad and Sub-Sections

The I/O sites are configurable as input, output, 3-state output and bidirectional buffers, each with pullup or pulldown capability, if required, by utilizing their corresponding sub-section. Bidirectionnal buffers are the result of an input and output buffers placed in adjacent sub-sections in the same I/O site. Special buffers may require multiple I/O sites. Oscillators require 2 I/O sites, each power and ground pin utilizes one I/O site.

PCI Buffers

PCI compatible input and output buffers are available for each bias voltage, 3 and 5V.

LVDS Buffers

Each LVDS buffer uses 2 I/O sites.

LVDS drivers are specific for each bias voltage and require one external current bias resistor per chip; LVDS receiver is the same for all bias voltages and requires 1 external line matching 100 kΩ resistor per receiver.

Cold Sparring

It is the use of twice the same chip, A1 and A2, A1 ON and A2 OFF, with all signal pins/pads connected by pairs, A1I1 with A2I1, A101 with A201,...

During this mode operation:

- the chip OFF must survive and operate when turned ON without functional, AC, DC or reliability impact,
- the current pulled by the OFF chip must be limited to a low value: Atmel specification for their dedicated cold sparring buffers is 2 µA worst case by signal pins/pads.

For any other operation mode, refer to maximum ratings.

Memory Blocks

Memory blocks can be either synthesized on gates (when smaller than 8 bits) or compiled and embedded in the array itself; various combinations of Through Flow or Bus Watch EDACs, 4, 8, 16 and 32 wide, can be used to alleviate the effect of SEU induced errors.

Design Options

ASIC Design Translation

Atmel has successfully translated existing designs from most major ASIC vendors (LSI Logic®, Motorola®, SMOS®, Oki®, NEC®, Fujitsu®, AMI® and others) into the gate arrays. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated for a pin-for-pin compatible, drop-in replacement.

Design Entry

Design entry is performed by the customer using an Atmel provided macro cell library. A complete netlist and vector set must then be provided to Atmel. Upon acceptance of this data set, Atmel continues with the standard design flow.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx®, Actel®, Altera®, AMD® and Atmel) into the gate arrays. There are four primary reasons to convert from an FPGA/PLD to a gate array. Conversion of high volume devices for a single or combined design is cost effective. Performance can often be optimized for speed or low power consumption. Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements. Finally, in situations where an FPGA/PLD was used for fast cycle time prototyping, a gate array may provide a lower cost answer for long-term volume production.

Cell Library

Atmel's MH1RT Series gate arrays make use of an extensive library of macro cell structures, including logic cells, buffers and inverters, multiplexers, decoders, and I/O options. Soft macros are also available.

The MH1RT Series PLL operates at frequencies of up to 250 MHz with minimal phase error and jitter, making it ideal for frequency synthesis of high speed on-chip clocks and chip to chip synchronization.

These cells are well characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test arrays. Characterization is performed over the rated temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product.

Table 3. Cell Index

Cell Name	Description	Gate Count
ADD3X	1 bit full adder with buffered outputs	10
AND2	2 input AND	2
AND2H	2 input AND - high drive	3
AND3	3 input AND	3
AND3H	3 input AND - high drive	4
AND4	4 input AND	3
AND4H	4 input AND - high drive	4
AND5	5 input AND	5
AOI22	2 input AND into 2 input NOR	2
AOI22H	2 input AND into 2 input NOR - high drive	4
AOI222	Two, 2 input ANDs into 2 input NOR	2
AOI222H	Two, 2 input ANDs into 2 input NOR - high drive	4
AOI2223	Three, 2 input ANDs into 3 input NOR	4
AOI2223H	Three, 2 input ANDs into 3 input NOR - high drive	8
AOI23	2 input AND into 3 input NOR	3
BUF1	1x buffer	2
BUF2	2x buffer	2
BUF2T	2x Tri State bus driver with active high enable	4
BUF2Z	2x Tri State bus driver with active low enable	4
BUF3	3x buffer	3
BUF4	4x buffer	3
BUF4T	4x Tri-State bus driver with active high enable	6
CLA7X	7 input carry lookahead	5
DEC4	2:4 decoder	8

Table 3. Cell Index (Continued)

Cell Name	Description	Gate Count
DEC4N	2:4 decoder with active low enable	10
DEC8N	3:8 decoder with active low enable	22
DFF	D flip-flop	8
DFFBCPX	D flip-flop with asynchronous clear and preset with complementary outputs	16
DFFBSRX	D flip-flop with asynchronous set and reset with complementary outputs	16
DFFC	D flip flop with asynchronous clear	9
DFFR	D flip-flop with asynchronous reset	10
DFFS	D flip-flop with asynchronous set	9
DFFSR	D flip-flop with asynchronous set and reset	11
DLY1	Delay buffer 1.0 ns	6
DLY2	Delay buffer 1.5 ns	9
DLY3	Delay buffer 2.0 ns	11
DPLG	Dual Port cell (for Genesys)	–
DSS	Set scan flip-flop	12
DSSBCPY	Set scan flip-flop with clear and preset	16
DSSBR	Set scan flip-flop with reset	14
DSSBS	Set scan flip-flop with set	14
DSSR	Set scan D flip-flop with reset	12
DSSS	Set scan D flip-flop with set	14
DSSSR	Set scan D flip-flop with set and reset	16
INV1	1x inverter	1
INV2	2x inverter	1
INV2T	2x Tri State inverter with active high enable	3
INV3	3x inverter	2
INV4	4x inverter	2
JKF	JK flip-flop	10
JKFBCPX	Clear preset JK flip-flop with asynchronous clear and preset and complementary outputs	16
JKFC	JK flip-flop with asynchronous clear	12
LAT	Latch	6
LATB	Latch with complementary outputs	6

Table 3. Cell Index (Continued)

Cell Name	Description	Gate Count
LATBG	Latch with complementary outputs and inverted gate signal	6
LATBH	Latch with high drive complementary outputs	7
LATIQ	Quad Latch	20
LATR	Latch with reset	5
LATS	Latch with set	6
LATSR	Latch with set and reset	8
MUX2	2:1 MUX	4
MUX2H	2:1 MUX - high drive	5
MUX2N	2:1 MUX with active low enable	5
MUX4	4:1 MUX	10
MUX5H	5:1 MUX - high drive	14
MUX8	8:1 MUX	20
MUX8N	8:1 MUX with active low enable	20
NAN2	2 input NAND	2
NAN2H	2 input NAND - high drive	2
NAN3	3 input NAND	2
NAN3H	3 input NAND - high drive	3
NAN4	4 input NAND	3
NAN4H	4 input NAND - high drive	4
NAN5	5 input NAND	5
NAN5H	5 input NAND - high drive	6
NAN6	6 input NAND	6
NAN6H	6 input NAND - high drive	7
NAN8	8 input NAND	7
NAN8H	8 input NAND - high drive	8
NOR2	2 input NOR	2
NOR2H	2 input NOR - high drive	2
NOR3	3 input NOR	2
NOR3H	3 input NOR - high drive	3
NOR4	4 input NOR	3
NOR4H	4 input NOR - high drive	5
NOR5	5 input NOR	5

Table 3. Cell Index (Continued)

Cell Name	Description	Gate Count
NOR8	8 input NOR	7
OAI22	2 input OR into 2 input NAND	2
OAI22H	2 input OR into 2 input NAND - high drive	4
OAI222	Two, 2 input ORs into 2 input NAND	3
OAI222H	Two, 2 input ORs into 2 input NAND - high drive	6
OAI22224	Four, 2 input ORs into 4 input NAND	8
OAI23	2 input OR into 3 input NAND	3
ORR2	2 input OR	2
ORR2H	2 input OR - high drive	3
ORR3	3 input OR	3
ORR3H	3 input OR - high drive	4
ORR4	4 input OR	3
ORR4H	4 input OR - high drive	4
ORR5	5 input OR	5
XNR2	2 input exclusive NOR	4
XNR2H	2 input exclusive NOR - high drive	4
XOR2	2 input exclusive OR	4
XOR2H	2 input exclusive OR - high drive	4

Table 4. I/O Buffer Cell Index

Buffer	I/O order	Description
PESD	X, P	Hard connection into array with ESD protection
PIC	AI, P	CMOS input buffer, TTL compatible at 3.0V
PICH	AI, P	CMOS input buffer, TTL compatible at 3.0V, high drive
PICI	AI, P	CMOS input buffer, TTL compatible at 3.0V, inverted output
PICS	AI, P	CMOS input buffer with Schmitt trigger, TTL compatible at 3.0V
PICSI	AI, P	CMOS input buffer with Schmitt trigger, TTL compatible at 3.0V, inverted output
PICSV	AI, P	CMOS input buffer with Schmitt trigger, TTL compatible at 3.0V, 5V tolerant
PICSV5	AI, P, VCC	CMOS input buffer with Schmitt trigger, TTL compatible at 3.0V, 5V compliant
PICV	AI, P	CMOS input buffer, TTL compatible at 3.0V, 5V tolerant

Table 4. I/O Buffer Cell Index (Continued)

Buffer	I/O order	Description
PICV5	AI, P, VCC	CMOS input buffer, TTL compatible at 3V, 5V compliant
PID	AI, P, REF, EN	Differential input buffer
PICV	AI, P	CMOS inout buffer, TTL compatible at 3V, 5V tolerant
PICV5	AI, P	CMOS inout buffer, TTL compatible at 3V, 5V compliant
PLL5-125	LCK, OSCCLKOUT, PLF, PVCOBIAS, CLKIN, CPA, CPB, EN, REFCLK, RSTN, TESTCLK, TESTEN, VDDPLL, VSSPLL	125 MHz Max. PLL
PLL5-250	LCK, OSCCLKOUT, PLF, PVCOBIAS, CLKIN, CPA, CPB, EN, REFCLK, RSTN, TESTCLK, TESTEN, VDDPLL, VSSPLL	250 MHz Max. PLL
PO11	P, AO, E0	Tristate output buffer, 2 mA drive
PO11F	P, AO, E0	Tristate output buffer, 2 mA drive, fast slew rate control
PO11S	P, AO, E0	Tristate output buffer, 2 mA drive, slow slew rate control
PO11V	P, AO, E0	Tristate output buffer, 2 mA drive, 5V tolerant
PO11V5	P, AO, E0	Tristate output buffer, 2 mA drive, 5V compliant
PO11VF	P, AO, E0	Tristate output buffer, 2 mA drive, fast slew rate control, 5V tolerant
PO11VS	P, AO, E0	Tristate output buffer, 2 mA drive, slow slew rate control, 5V tolerant
PO22	P, AO, E0	Tristate output buffer, 4 mA drive
PO22F	P, AO, E0	Tristate output buffer, 4 mA drive, fast slew rate control
PO22I	P, AO, E0	Tristate output buffer, 4 mA drive, inverted output
PO22S	P, AO, E0	Tristate output buffer, 4 mA drive, slow slew rate control
PO22V	P, AO, E0	Tristate output buffer, 4 mA drive, 5V tolerant
PO22V5	P, AO, E0	Tristate output buffer, 4 mA drive, 5V compliant
PO22VF	P, AO, E0	Tristate output buffer, 4 mA drive, fast slew rate control, 5V tolerant
PO22VS	P, AO, E0	Tristate output buffer, 4 mA drive, slow slew rate control, 5V tolerant
PO33	P, AO, E0	Tristate output buffer, 6 mA drive
PO33F	P, AO, E0	Tristate output buffer, 6 mA drive, fast slew rate control
PO33S	P, AO, E0	Tristate output buffer, 6 mA drive, slow slew rate control

Table 4. I/O Buffer Cell Index (Continued)

Buffer	I/O order	Description
PO33V	P, AO, E0	Tristate output buffer, 6 mA drive, 5V tolerant
PO33VF	P, AO, E0	Tristate output buffer, 6 mA drive, fast slew rate control, 5V tolerant
PO33VS	P, AO, E0	Tristate output buffer, 6 mA drive, slow slew rate control, 5V tolerant
PO44	P, AO, E0	Tristate output buffer, 8 mA drive
PO44F	P, AO, E0	Tristate output buffer, 8 mA drive, fast slew rate control
PO44S	P, AO, E0	Tristate output buffer, 8 mA drive, slow slew rate control
PO44V	P, AO, E0	Tristate output buffer, 8 mA drive, 5V tolerant
PO44V5	P, AO, E0	Tristate output buffer, 8 mA drive, 5V compliant
PO44VF	P, AO, E0	Tristate output buffer, 8 mA drive, fast slew rate control, 5V tolerant
PO44VS	P, AO, E0	Tristate output buffer, 8 mA drive, slow slew rate control, 5V tolerant
PO55	P, AO, E0	Tristate output buffer, 10 mA drive
PO55F	P, AO, E0	Tristate output buffer, 10 mA drive, fast slew rate control
PO55S	P, AO, E0	Tristate output buffer, 10 mA drive, slow slew rate control
PO55V	P, AO, E0	Tristate output buffer, 10 mA drive, 5V tolerant
PO55VF	P, AO, E0	Tristate output buffer, 10 mA drive, fast slew rate control, 5V tolerant
PO55VS	P, AO, E0	Tristate output buffer, 10 mA drive, slow slew rate control, 5V tolerant
PO66	P, AO, E0	Tristate output buffer, 12 mA drive
PO66F	P, AO, E0	Tristate output buffer, 12 mA drive, fast slew rate control
PO66S	P, AO,E0	Tristate output buffer, 12 mA drive, slow slew rate control
PO66V	P, AO, E0	Tristate output buffer, 12 mA drive, 5V tolerant
PO66VF	P, AO, E0	Tristate output buffer, 12 mA drive, fast slew rate control, 5V tolerant
PO66VS	P, AO, E0	Tristate output buffer, 12 mA drive, slow slew rate control, 5V tolerant
PO77	P, AO, E0	Tristate output buffer, 14 mA drive
PO77F	P, AO, E0	Tristate output buffer, 14 mA drive, fast slew rate control
PO77S	P, AO, E0	Tristate output buffer, 14 mA drive, slow slew rate control
PO77V	P, AO, E0	Tristate output buffer, 14 mA drive, 5V tolerant
PO77VF	P, AO, E0	Tristate output buffer, 14 mA drive, fast slew rate control, 5V tolerant

Table 4. I/O Buffer Cell Index (Continued)

Buffer	I/O order	Description
PO77VS	P, AO, E0	Tristate output buffer, 14 mA drive, slow slew rate control, 5V tolerant
PO88	P, AO, E0	Tristate output buffer, 16 mA drive
PO88F	P, AO, E0	Tristate output buffer, 16 mA drive, fast slew rate control
PO88S	P, AO, E0	Tristate output buffer, 16 mA drive, slow slew rate control
PO88V	P, AO, E0	Tristate output buffer, 16 mA drive, 5V tolerant
PO88VF	P, AO, E0	Tristate output buffer, 16 mA drive, fast slew rate control, 5V tolerant
PO88VS	P, AO, E0	Tristate output buffer, 16 mA drive, slow slew rate control, 5V tolerant
PO99	P, AO, E0	Tristate output buffer, 18 mA drive
PO99F	P, AO, E0	Tristate output buffer, 18 mA drive, fast slew rate control
PO99S	P, AO, E0	Tristate output buffer, 18 mA drive, slow slew rate control
PO99V	P, AO, E0	Tristate output buffer, 18 mA drive, 5V tolerant
PO99VF	P, AO, E0	Tristate output buffer, 18 mA drive, fast slew rate control, 5V tolerant
PO99VS	P, AO, E0	Tristate output buffer, 18 mA drive, slow slew rate control, 5V tolerant
POAA	P, AO, E0	Tristate output buffer, 20 mA drive
POAAF	P, AO, E0	Tristate output buffer, 20 mA drive, fast slew rate control
POAAS	P, AO, E0	Tristate output buffer, 20 mA drive, slow slew rate control
POAAV	P, AO, E0	Tristate output buffer, 20 mA drive, 5V tolerant
POAAVF	P, AO, E0	Tristate output buffer, 20 mA drive, fast slew rate control, 5V tolerant
POAAVS	P, AO, E0	Tristate output buffer, 20 mA drive, slow slew rate control, 5V tolerant
POBB	P, AO, E0	Tristate output buffer, 22 mA drive
POBBF	P, AO, E0	Tristate output buffer, 22 mA drive, fast slew rate control
POBBS	P, AO, E0	Tristate output buffer, 22 mA drive, slow slew rate control
POBBV	P, AO, E0	Tristate output buffer, 22 mA drive, 5V tolerant
POBBVF	P, AO, E0	Tristate output buffer, 22 mA drive, fast slew rate control, 5V tolerant
POBBVS	P, AO, E0	Tristate output buffer, 22 mA drive, slow slew rate control, 5V tolerant
POCC	P, AO, E0	Tristate output buffer, 24 mA drive
POCCF	P, AO, E0	Tristate output buffer, 24 mA drive, fast slew rate control

Table 4. I/O Buffer Cell Index (Continued)

Buffer	I/O order	Description
POCCS	P, AO, E0	Tristate output buffer, 24 mA drive, slow slew rate control
POCV5	P, AO, EO	Tristate output buffer, 16.8 mA drive, 5V compliant
PRD1	P	20 kΩ pull-down terminator
PRD10	P	200 kΩ pull-down terminator
PRD10V5	P	200 kΩ pull-down terminator, 5V compliant
PRD11	P	220 kΩ pull-down terminator
PRD11V5	P	220 kΩ pull-down terminator, 5V compliant
PRD12	P	240 kΩ pull-down terminator
PRD12V5	P	240 kΩ pull-down terminator, 5V compliant
PRD13	P	260 kΩ pull-down terminator
PRD13V5	P	260 kΩ pull-down terminator, 5V compliant
PRD14	P	280 kΩ pull-down terminator
PRD14V5	P	280 kΩ pull-down terminator, 5V compliant
PRD15	P	300 kΩ pull-down terminator
PRD15V5	P	300 kΩ pull-down terminator, 5V compliant
PRD16	P	320 kΩ pull-down terminator
PRD16V5	P	320 kΩ pull-down terminator, 5V compliant
PRD17	P	340 kΩ pull-down terminator
PRD17V5	P	340 kΩ pull-down terminator, 5V compliant
PRD18	P	360 kΩ pull-down terminator
PRD18V5	P	360 kΩ pull-down terminator, 5V compliant
PRD19	P	380 kΩ pull-down terminator
PRD19V5	P	380 kΩ pull-down terminator, 5V compliant
PRD1V5	P	20 kΩ pull-down terminator, 5V compliant
PRD2	P	40 kΩ pull-down terminator
PRD20	P	400 kΩ pull-down terminator
PRD20V5	P	400 kΩ pull-down terminator, 5V compliant
PRD21	P	420 kΩ pull-down terminator
PRD21V5	P	420 kΩ pull-down terminator, 5V compliant
PRD22	P	440 kΩ pull-down terminator
PRD22V5	P	440 kΩ pull-down terminator, 5V compliant
PRD23	P	460 kΩ pull-down terminator

Table 4. I/O Buffer Cell Index (Continued)

Buffer	I/O order	Description
PRD23V5	P	460 kΩ pull-down terminator, 5V compliant
PRD24	P	480 kΩ pull-down terminator
PRD24V5	P	480 kΩ pull-down terminator, 5V compliant
PRD25	P	500 kΩ pull-down terminator
PRD25V5	P	500 kΩ pull-down terminator, 5V compliant
PRD26	P	520 kΩ pull-down terminator
PRD26V5	P	520 kΩ pull-down terminator, 5V compliant
PRD27	P	540 kΩ pull-down terminator
PRD27V5	P	540 kΩ pull-down terminator, 5V compliant
PRD28	P	560 kΩ pull-down terminator
PRD28V5	P	560 kΩ pull-down terminator, 5V compliant
PRD29	P	580 kΩ pull-down terminator
PRD29V5	P	580 kΩ pull-down terminator, 5V compliant
PRD2V5	P	40 kΩ pull-down terminator, 5V compliant
PRD3	P	60 kΩ pull-down terminator
PRD30	P	600 kΩ pull-down terminator
PRD30V5	P	600 kΩ pull-down terminator, 5V compliant
PRD31	P	620 kΩ pull-down terminator
PRD31V5	P	620 kΩ pull-down terminator, 5V compliant
PRD3V5	P	60 kΩ pull-down terminator, 5V compliant
PRD4	P	80 kΩ pull-down terminator
PRD4V5	P	80 kΩ pull-down terminator, 5V compliant
PRD5	P	100 kΩ pull-down terminator
PRD5V5	P	100 kΩ pull-down terminator, 5V compliant
PRD6	P	120 kΩ pull-down terminator
PRD6V5	P	120 kΩ pull-down terminator, 5V compliant
PRD7	P	140 kΩ pull-down terminator
PRD7V5	P	140 kΩ pull-down terminator, 5V compliant
PRD8	P	160 kΩ pull-down terminator
PRD8V5	P	160 kΩ pull-down terminator, 5V compliant
PRD9	P	180 kΩ pull-down terminator
PRD9V5	P	180 kΩ pull-down terminator, 5V compliant

Table 4. I/O Buffer Cell Index (Continued)

Buffer	I/O order	Description
PRU1	P	20 kΩ pull-up terminator
PRU10	P	200 kΩ pull-up terminator
PRU10V5	P	200 kΩ pull-up terminator, 5V compliant
PRU11	P	220 kΩ pull-up terminator
PRU11V5	P	220 kΩ pull-up terminator, 5V compliant
PRU12	P	240 kΩ pull-up terminator
PRU12V5	P	240 kΩ pull-up terminator, 5V compliant
PRU13	P	260 kΩ pull-up terminator
PRU13V5	P	260 kΩ pull-up terminator, 5V compliant
PRU14	P	280 kΩ pull-up terminator
PRU14V5	P	280 kΩ pull-up terminator, 5V compliant
PRU15	P	300 kΩ pull-up terminator
PRU15V5	P	300 kΩ pull-up terminator, 5V compliant
PRU16	P	320 kΩ pull-up terminator
PRU16V5	P	320 kΩ pull-up terminator, 5V compliant
PRU17	P	340 kΩ pull-up terminator
PRU17V5	P	340 kΩ pull-up terminator, 5V compliant
PRU18	P	360 kΩ pull-up terminator
PRU18V5	P	360 kΩ pull-up terminator, 5V compliant
PRU19	P	380 kΩ pull-up terminator
PRU19V5	P	380 kΩ pull-up terminator, 5V compliant
PRU1V5	P	20 kΩ pull-up terminator, 5V compliant
PRU2	P	20 kΩ pull-up terminator
PRU20	P	400 kΩ pull-up terminator
PRU20V5	P	400 kΩ pull-up terminator, 5V compliant
PRU21	P	420 kΩ pull-up terminator
PRU21V5	P	420 kΩ pull-up terminator, 5V compliant
PRU22	P	440 kΩ pull-up terminator
PRU22V5	P	440 kΩ pull-up terminator, 5V compliant
PRU23	P	460 kΩ pull-up terminator
PRU23V5	P	460 kΩ pull-up terminator, 5V compliant
PRU24	P	480 kΩ pull-up terminator

Table 4. I/O Buffer Cell Index (Continued)

Buffer	I/O order	Description
PRU24V5	P	480 kΩ pull-up terminator, 5V compliant
PRU25	P	500 kΩ pull-up terminator
PRU25V5	P	500 kΩ pull-up terminator, 5V compliant
PRU26	P	520 kΩ pull-up terminator
PRU26V5	P	520 kΩ pull-up terminator, 5V compliant
PRU27	P	540 kΩ pull-up terminator
PRU27V5	P	540 kΩ pull-up terminator, 5V compliant
PRU28	P	560 kΩ pull-up terminator
PRU28V5	P	560 kΩ pull-up terminator, 5V compliant
PRU29	P	580 kΩ pull-up terminator
PRU29V5	P	580 kΩ pull-up terminator, 5V compliant
PRU2V5	P	40 kΩ pull-up terminator, 5V compliant
PRU3	P	60 kΩ pull-up terminator
PRU30	P	600 kΩ pull-up terminator
PRU30V5	P	600 kΩ pull-up terminator, 5V compliant
PRU31	P	620 kΩ pull-up terminator
PRU31V5	P	620 kΩ pull-up terminator, 5V compliant
PRU3V5	P	60 kΩ pull-up terminator, 5V compliant
PRU4	P	80 kΩ pull-up terminator
PRU4V5	P	80 kΩ pull-up terminator, 5V compliant
PRU5	P	100 kΩ pull-up terminator
PRU5V5	P	100 kΩ pull-up terminator, 5V compliant
PRU6	P	120 kΩ pull-up terminator
PRU6V5	P	120 kΩ pull-up terminator, 5V compliant
PRU7	P	140 kΩ pull-up terminator
PRU7V5	P	140 kΩ pull-up terminator, 5V compliant
PRU8	P	160 kΩ pull-up terminator
PRU8V5	P	160 kΩ pull-up terminator, 5V compliant
PRU9	P	180 kΩ pull-up terminator
PRU9V5	P	180 kΩ pull-up terminator, 5V compliant
PVCCB	P	Buffer VCC supply pad
PVDDA	VCC, P	Array VDD supply pad

Table 4. I/O Buffer Cell Index (Continued)

Buffer	I/O order	Description
PVDDB	P	Buffer VDD supply pad for standard buffers
PVDDV3B	P	Buffer VDD supply pad for 5V compliant buffers
PVDDVB	P	Buffer VDD supply pad for 5V tolerant buffers
PVSSA	VSS, P	Array VSS supply pad
PVSSB	P	Buffer VSS supply pad

Table 5. Cold Sparing Buffers

Cell Name	I/O order	Description
PO11VZ	P, AO, EO	Tristate output buffer, 1.4 mA drive, for cold sparing, 5V tolerant
PO11Z	P, AO, EO	Tristate output buffer, 2 mA drive, for cold sparing
PO22VZ	P, AO, EO	Tristate output buffer, 2.8 mA drive, for cold sparing, 5V tolerant
PO22Z	P, AO, EO	Tristate output buffer, 4 mA drive, for cold sparing
PO33VZ	P, AO, EO	Tristate output buffer, 4.2 mA drive, for cold sparing, 5V tolerant
PO33Z	P, AO, EO	Tristate output buffer, 6 mA drive, for cold sparing
PO44VZ	P, AO, EO	Tristate output buffer, 5.6 mA drive, for cold sparing, 5V tolerant
PO44Z	P, AO, EO	Tristate output buffer, 8 mA drive, for cold sparing
PO55VZ	P, AO, EO	Tristate output buffer, 7 mA drive, for cold sparing, 5V tolerant
PO55Z	P, AO, EO	Tristate output buffer, 10 mA drive, for cold sparing
PO66VZ	P, AO, EO	Tristate output buffer, 8.4 mA drive, for cold sparing, 5V tolerant
PO66Z	P, AO, EO	Tristate output buffer, 12 mA drive, for cold sparing
PO77VZ	P, AO, EO	Tristate output buffer, 9.8 mA drive, for cold sparing, 5V tolerant
PO77Z	P, AO, EO	Tristate output buffer, 14 mA drive, for cold sparing
PO88VZ	P, AO, EO	Tristate output buffer, 11.2 mA drive, for cold sparing, 5V tolerant
PO88Z	P, AO, EO	Tristate output buffer, 16 mA drive, for cold sparing
PO99VZ	P, AO, EO	Tristate output buffer, 12.6 mA drive, for cold sparing, 5V tolerant
PO99Z	P, AO, EO	Tristate output buffer, 18 mA drive, for cold sparing
POAAVZ	P, AO, EO	Tristate output buffer, 14 mA drive, for cold sparing, 5V tolerant
POAAZ	P, AO, EO	Tristate output buffer, 20 mA drive, for cold sparing
POBBVZ	P, AO, EO	Tristate output buffer, 15.4 mA drive, for cold sparing, 5V tolerant
POBBZ	P, AO, EO	Tristate output buffer, 22 mA drive, for cold sparing
POCCVZ	P, AO, EO	Tristate output buffer, 16.8 mA drive, for cold sparing, 5V tolerant
POCCZ	P, AO, EO	Tristate output buffer, 24 mA drive, for cold sparing

Table 5. Cold Sparing Buffers (Continued)

Cell Name	I/O order	Description
PICVZ	AI, P	Cold sparing CMOS input buffer, TTL compatible at 3V, 5V compliant
PICZ	AI, P	Cold sparing CMOS input buffer, TTL compatible at 3V
PVDDVZB	P	Buffer VDD supply pad for tolerant cold sparing buffers
PVDDZB	P	Buffer VDD supply pad for standard cold sparing buffers
PRD1Z	P	20 kΩ cold sparing pull-down terminator
PRD10Z	P	200 kΩ cold sparing pull-down terminator
PRD11Z	P	220 kΩ cold sparing pull-down terminator
PRD12Z	P	240 kΩ cold sparing pull-down terminator
PRD13Z	P	260 kΩ cold sparing pull-down terminator
PRD14Z	P	280 kΩ cold sparing pull-down terminator
PRD15Z	P	300 kΩ cold sparing pull-down terminator
PRD16Z	P	320 kΩ cold sparing pull-down terminator
PRD17Z	P	340 kΩ cold sparing pull-down terminator
PRD18Z	P	360 kΩ cold sparing pull-down terminator
PRD19Z	P	380 kΩ cold sparing pull-down terminator
PRD20Z	P	400 kΩ cold sparing pull-down terminator
PRD21Z	P	420 kΩ cold sparing pull-down terminator
PRD22Z	P	440 kΩ cold sparing pull-down terminator
PRD23Z	P	460 kΩ cold sparing pull-down terminator
PRD24Z	P	480 kΩ cold sparing pull-down terminator
PRD25Z	P	500 kΩ cold sparing pull-down terminator
PRD26Z	P	520 kΩ cold sparing pull-down terminator
PRD27Z	P	540 kΩ cold sparing pull-down terminator
PRD28Z	P	560 kΩ cold sparing pull-down terminator
PRD29Z	P	580 kΩ cold sparing pull-down terminator
PRD2Z	P	40 kΩ cold sparing pull-down terminator
PRD30Z	P	600 kΩ cold sparing pull-down terminator
PRD31Z	P	620 kΩ cold sparing pull-down terminator
PRD3Z	P	60 kΩ cold sparing pull-down terminator
PRD4Z	P	80 kΩ cold sparing pull-down terminator
PRD5Z	P	100 kΩ cold sparing pull-down terminator
PRD6Z	P	120 kΩ cold sparing pull-down terminator

Table 5. Cold Sparing Buffers (Continued)

Cell Name	I/O order	Description
PRD7Z	P	140 kΩ cold sparing pull-down terminator
PRD8Z	P	160 kΩ cold sparing pull-down terminator
PRD9Z	P	180 kΩ cold sparing pull-down terminator

Table 6. SEU Hardened Cells

Cell Name	Description
HDS	SEU hardened set scan D flip-flop
HDSR	SEU hardened set scan D flip-flop with async. reset
HDSP	SEU hardened set scan D flip-flop with async. preset
HDF	SEU hardened D flip-flop
HDFR	SEU hardened D flip-flop with async. reset
HDFP	SEU hardened D flip-flop with async. preset
HLT	SEU hardened latch
HLTR	SEU hardened latch with async. reset
HTLP	SEU hardened latch with async. preset

Table 7. Specific Buffer Cells

Cell Name	I/O Order	Description
PFILVDS	AI, AIB, P, PN, EO	LVDS compatible input buffer
PFOLVDS25	P, PB, AO, EO, IREF	2.5V VDD range LVDS compatible output buffer
PFOLVDS30	P, PB, AO, EO, IREF	3V VDD range LVDS compatible output buffer
PFOLVDS33	P, PB, AO, EO, IREF	3.3V VDD range LVDS compatible output buffer
PFOLVDSREF	AI, P	IREF buffer for LVDS outputs
PFIPCI	AI, P	PCI compatible 3V input buffer
PFIPCIV	AI, P	PCI compatible 5V input buffer
POPCI	P, AO, EO	PCI compatible 3V output buffer
POPCIV5	P, AO, EO	PCI compatible 5V output buffer

Electrical Characteristics

Absolute Maximum Ratings

Operating Ambient Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Maximum Input Voltage VDD	+0.5V and VCC + 0.5V
Maximum 3.3V Operating Voltage	4V (VDD)
Maximum 5V Operating Voltage	6V (VCC)

*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 8. 2.5V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
T_A	Operating Temperature	All	–	-55	25	125	C
V_{DD}	Supply Voltage	All	–	2.3	2.5	2.7	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	V_{IN} = V_{SS}	-1 70 -5	– –	1 230 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	V_{IN} = $V_{DD\ (Max.)}$	-1 -5 70	– –	1 5 540	µA
Ioz	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd (Max.) No pull resistor	-1	–	1	µA
Vil	Low level Input voltage	CMOS	–	–	–	0.3Vdd	V
		CMOS Schmitt level	–	–	–	0.62	
			–	–	–		
Vih	High level Input voltage	CMOS	–	0.7 Vdd	–	–	V
		CMOS Schmitt level	–	1.56	–	–	
Delta V	CMOS Hysterisis		–	–	0.42	–	V
Iics	Cold sparing leakage input current	PICZ	Vdd = Vss = 0V Vin = 0 to 3.3V	-2		-2	µA
Iocs	Cold sparing leakage output current	POxxZ	Vdd = Vss = 0V Vin = 0 to 3.3V	-2		-2	µA
Vcsth (3)	Supply threshold of cold sparing buffers	POxxZ	Iocs = 100 µA	–	0.5	–	V
V_{OL}	Low-level Output Voltage (4)	PO11	I_{OL} = 0.8 mA, Vdd = Vdd (Min.)	–	–	0.4	V
Voh	High level output voltage (5)	PO11	Ioh = -0.6 mA, Vdd = Vdd (Min.)	2	–	–	V

Table 8. 2.5V DC Characteristics (Continued)

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
Ios	Output short circuit current Iosn Iosp	 PO11 PO11	Vdd = Vdd (Max.), Vout = Vdd Vouy = Vss	–	–	 15 8	mA
Iccsb	Leakage current per cell		Vdd = Vdd (Max.)	–	0.27	4	nA
Iccop	Dynamic current per gate		Vdd = Vdd (Max.)	–		0.3	µW/MHz

1. For standard pull-ups: PRU (#), # = {1-31} index for Ron: Ron = # x RO where RO = 19 kΩ typ, 30 kΩ Max., 12 kΩ Min.
2. For standard pull-downs: PRD (#), # = {1-31} index for Ron: Ron = # x RO where RO = 11 kΩ typ, 30 kΩ Max., 5 kΩ Min.
3. Guaranteed not tested
4. For output buffers PO (1-C) (1-C):

   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive

   IO = 0.8 mA for standard buffers (including cold sparing) measured at Vol = 0.4V
5. For output buffers PO (1-C) (1-C):

   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive

   IO = -0.6 mA for standard buffers (including cold sparing) measured at Voh = 2V

Applicable over recommended operating temperature and voltage range unless otherwise noted.

.

Table 9. 3V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
T_A	Operating Temperature	All	–	-55	25	125	C
V_{DD}	Supply Voltage	All	–	2.3	2.5	2.7	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	V_{IN} = V_{SS}	-1 108 -5	– – –	1 330 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	V_{IN} = $V_{DD(Max.)}$	-1 -5 108	– – –	1 5 825	µA
Ioz	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd (Max.) No pull resistor	-1	–	1	µA
Vil	Low level Input voltage	CMOS	–	–	–	0.8	V
		CMOS Schmitt level	–	–	–	0.72	
Vih	High level Input voltage	CMOS	–	2	–	–	V
		CMOS Schmitt level	–	1.89	–	–	
Delta V	CMOS Hysterisis	–	–	–	0.53	–	V
Iics	Cold sparing leakage input current	PICZ	Vdd = Vss = 0V Vin = 0 to 3.3V	-2	–	-2	µA
Iocs	Cold sparing leakage output current	POxxZ	Vdd = Vss = 0V Vin = 0 to 3.3V	-2	–	-2	µA
Vcsth (3)	Supply threshold of cold sparing buffers	POxxZ	Iocs = 100 µA	–	0.5	–	V
V_{OL}	Low-level Output Voltage (4)	PO11	I_{OL} = 1 mA, Vdd = Vdd(Min.)	– –	– –	0.4	V
Voh	High level output voltage (5)	PO11	Ioh = -0.8 mA, Vdd = Vdd(Min.)	2.4	–	–	V
Ios	Output short circuit current Iosn Iosp	PO11 PO11	Vdd = Vdd(Max.), Vout = Vdd Vouy = Vss	–	–	21 12	mA
Iccsb	Leakage current per cell	–	Vdd = Vdd(Max.)	–	0.6	5	nA
Iccop	Dynamic current per gate	–	Vdd = Vdd(Max.)	–	–	0.5	µW/MHz

1. For standard pull-ups: PRU (#), # = {1-31} index for Ron: Ron = # x RO where RO = 15 kΩ typ, 25 kΩ Max., 10 kΩ Min.
2. For standard pull-downs: PRD (#), # = {1-31} index for Ron: Ron = # x RO where RO = 9 kΩ typ, 25 kΩ Max., 4 kΩ Min.
3. Guaranteed not tested.
4. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = 1 mA for standard buffers (including cold sparing) measured at Vol = 0.4V
5. For output buffers PO (1-C) (1-C):1-C:
   hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = -0.8 mA for standard buffers (including cold sparing) measured at Voh = 2.4V

Table 10. 3.3V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
T_A	Operating Temperature	All	–	-55	25	125	C
V_{DD}	Supply Voltage	All	–	2.3	2.5	2.7	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	V_{IN} = V_{SS}	-1 120 -5	–	1 400 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	V_{IN} = $V_{DD(Max.)}$	-1 -5 150	–	1 5 900	µA
Ioz	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd(Max.) No pull resistor	-1	–	1	µA
Vil	Low level Input voltage	CMOS	–	–	–	0.8	V
		CMOS Schmitt level	–	–	–	0.8	
Vih	High level Input voltage	CMOS	–	2	–	–	V
		CMOS Schmitt level	–	2	–	–	
Delta V	CMOS Hysterisis	–	–	–	0.61	–	V
Iics	Cold sparing leakage input current	PICZ	Vdd = Vss = 0V Vin = 0 to 3.3V	-2	–	-2	µA
Iocs	Cold sparing leakage output current	POxxZ	Vdd = Vss = 0V Vin = 0 to 3.3V	-2	–	-2	µA
Vcsth (3)	Supply threshold of cold sparing buffers	POxxZ	Iocs = 100 µA	–	0.5	–	V
V_{OL}	Low-level Output Voltage (4)	PO11	I_{OL} = 2 mA, Vdd = Vdd(Min.)	– –	–	0.4	V
Voh	High level output voltage (5)	PO11	Ioh = -1.8 mA, Vdd = Vdd(Min.)	2.4	–	–	V
Ios	Output short circuit current Iosn Iosp	PO11 PO11	Vdd = Vdd(Max.), Vout = Vdd Vouy = Vss	–	–	23 13	mA
Iccsb	Leakage current per cell	–	Vdd = Vdd(Max.)	–	0.7	5	nA
Iccop	Dynamic current per gate	–	Vdd = Vdd(Max.)	–	–	0.63	µW/MHz

1. For standard pull-ups: PRU(#), # = {1-31} index for Ron: Ron = # x RO where RO = 14 kΩ typ, 25 kΩ Max., 9 kΩ Min.
2. For standard pull-downs:PRD(#), # = {1-31} index for Ron: Ron = # x RO where RO = 8kΩ typ, 20 kΩ Max., 4 kΩ Min.
3. Guaranteed not tested.
4. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to kΩ x IO = p and n-channel output drive
   IO = 2 mA for standard buffers (including cold sparing) measured at Vol = 0.4V
5. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to kΩ x IO = p and n-channel output drive
   IO = -1.8 mA for standard buffers (including cold sparing) measured at Voh = 2.4V

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 11. 5V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min.	Typ	Max.	Units
T_A	Operating Temperature	All	–	-55	25	125	C
V_{DD}	Supply Voltage	All	–	2.3	2.5	2.7	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	V_{IN} = V_{SS}	-1 180 -5	– – –	1 690 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	V_{IN} = $V_{DD(Max.)}$	-1 -5 30	– – –	1 5 400	µA
Ioz	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd(Max.) No pull resistor	-1	–	1	µA
Vil	Low level Input voltage	PICV, PICV5	–	–	–	0.8	V
		CMOS Schmitt level	–	–	–	0.8	
Vih	High level Input voltage	PICV, PICV5	–	2	–	–	V
		CMOS Schmitt level	–	2	–	–	
Iics	Cold sparing leakage input current	PICZ	Vdd = Vss = 0V Vin = 0 to 3.3V	-2	–	-2	µA
Iocs	Cold sparing leakage output current	POxxZ	Vdd = Vss = 0V Vin = 0 to 3.3V	-2	–	-2	µA
Vcsth (3)	Supply threshold of cold sparing buffers	POxxZ	Iocs = 100 µA	–	0.5	–	V
V_{OL} (4)	Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range	PO11V PO11V PO11V PO11V5 PO11V5 PO11V5	Iol = 0.5 mA Iol = 0.6 mA Iol = 1.2 mA Iol = 1.1 mA Iol = 1.3 mA Iol = 1.5 mA	–	–	0.4	V
Voh (5)	Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range	PO11V PO11V PO11V PO11V5 PO11V5 PO11V5	Ioh = 0.5 mA Ioh = 0.6 mA Ioh = 1.2 mA Ioh = 1.1 mA Ioh = 1.3 mA Ioh = 1.5 mA	2 2.4 2.4 2.4 2.4 2.4	–	–	V
Ios	Output short circuit current Iosn Iosp	PO11V PO11V	Vdd = Vdd(Max.), Vout = Vdd Vouy = Vss	–	–	28 17	mA

1. For 5V tolerant/compliant pull-ups: PRU(#), # = {1-31} index for Ron: Ron = # x RO where RO = 14 kΩ typ, 25 kΩ Max., 8 kΩ Min.
2. For 5V tolerant/compliant pull-downs: PRD(#), # = {1-31} index for Ron: Ron = # x RO where:
   RO = 19 kΩ typ, 45 kΩ Max., 9 kΩ Min. in 3.3V range,
   RO = 23 kΩ typ, 55 kΩ Max., 11 kΩ Min. in 3V range,
   RO = 36 kΩ typ, 80 kΩ Max., 17 kΩ Min. in 2.5V range,
3. Guaranteed not tested.
4. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to kΩ x IO = p and n-channel output drive
   IO = 1.5 mA for compliant buffers (including cold sparing) in 3.3V range (Vcc = 4.5V) measured at Vol = 0.4V
   IO = 1.3 mA for compliant buffers (including cold sparing) in 3.0V range (Vcc = 4.5V) measured at Vol = 0.4V
   IO = 1.1 mA for compliant buffers (including cold sparing) in 2.5V range (Vcc = 4.5V) measured at Vol = 0.4V
5. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to kΩ x IO = p and n-channel output drive
   IO = 1.5 mA for compliant buffers (including cold sparing) in 3.3V range (Vcc = 4.5V) measured at Vol = 2.4V
   IO = 1.3 mA for compliant buffers (including cold sparing) in 3.0V range (Vcc = 4.5V) measured at Vol = 2.4V
   IO = 1.1 mA for compliant buffers (including cold sparing) in 2.5V range (Vcc = 4.5V) measured at Vol = 2.0V

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 12. 2.5V LVDS Driver DC/ AC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
T_A	Operating Temperature	–	-55	125	°C	–
V_{DD}	Supply Voltage	–	2.3	2.7	V	–
|VOD|	Output differential voltage	Rload = 100Ω	230.7	446.5	mV	see Figure 4
Vol	Output voltage low	Rload = 100Ω	1224	1817	mV	see Figure 4
Voh	Output voltage high	Rload = 100Ω	993	1406	mV	see Figure 4
VOS	Output offset voltage	Rload = 100Ω	1108	1610	mV	see Figure 4
|Delta VOD|	Change in |VOD| between "0" and "1"	Rload = 100Ω	0	50	mV	–
|Delta VOS|	Change in |VOS| between "0" and "1"	Rload = 100Ω	0	100	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.3	mA	–
ISAB	Output current	Drivers shorted together	2.4	4.8	mA	–
Rbias	Bias resistor	–	9.8	10.2	KΩ	1 per chip
Ibias	Bias static current	–	5.8	11.7	mA	
F Max.	Maximum operating frequency	VDD = 2.5V ± 0.2V	–	180	MHz	Consumption 14.8 mA
Clock	Clock signal duty cycle	Max. frequency	45	55	%	–
Tfall	Fall time 80-20%	Rload = 100Ω	669	1178	ps	see Figure 4
Trise	Rise time 20-80%	Rload = 100Ω	670	1167	ps	see Figure 4
Tp	Propagation delay	Rload = 100Ω	1270	2660	ps	see Figure 4
Tsk1	Duty cycle skew	Rload = 100Ω	0	110	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 13. 3V LVDS Driver DC/ AC Characteristics

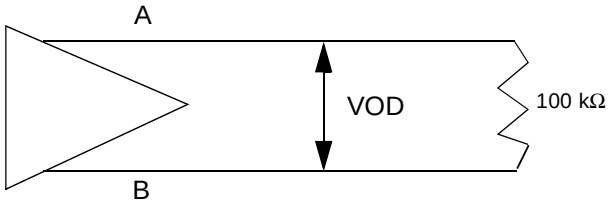
Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
T_A	Operating Temperature	–	-55	125	°C	–
V_{DD}	Supply Voltage	–	2.7	3.3	V	–
|VOD|	Output differential voltage	Rload = 100Ω	244	462	mV	see Figure 4
Vol	Output voltage low	Rload = 100Ω	1088	1775	mV	see Figure 4
Voh	Output voltage high	Rload = 100Ω	828	1358	mV	see Figure 4
VOS	Output offset voltage	Rload = 100Ω	958	568	mV	see Figure 4
|Delta VOD|	Change in |VOD| between "0" and "1"	Rload = 100Ω	0	50	mV	–
|Delta VOS|	Change in |VOS| between "0" and "1"	Rload = 100Ω	0	150	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.3	mA	–
ISAB	Output current	Drivers shorted together	2.6	5	mA	–
Rbias	Bias resistor	–	12.8	13.2	KΩ	1 per chip
Ibias	Bias static current	–	6.5	13.8	mA	–
F Max.	Maximum operating frequency	VDD = 2.5V ± 0.2V	–	200	MHz	Consumption 18.6 mA
Clock	Clock signal duty cycle	Max. frequency	45	55	%	–
Tfall	Fall time 80-20%	Rload = 10Ω	512	968	ps	see Figure 4
Trise	Rise time 20-80%	Rload = 100Ω	512	970	ps	see Figure 4
Tp	Propagation delay	Rload = 100Ω	1150	2300	ps	see Figure 4
Tsk1	Duty cycle skew	Rload = 100Ω	0	70	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 14. 3.3V LVDS Driver DC/ AC Characteristics

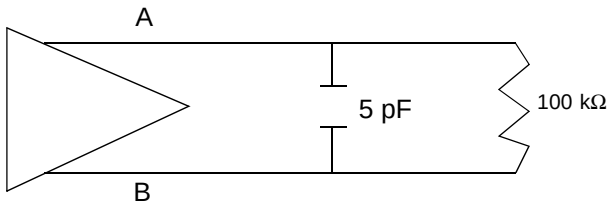
Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
T_A	Operating Temperature	–	-55	125	°C	–
V_{DD}	Supply Voltage	–	3	3.3	V	–
|VOD|	Output differential voltage	Rload = 100Ω	251.4	452.2	mV	see Figure 4
Vol	Output voltage low	Rload = 100Ω	1071	1731	mV	see Figure 4
Voh	Output voltage high	Rload = 100Ω	804	1323	mV	see Figure 4
VOS	Output offset voltage	Rload = 100Ω	937	1527	mV	see Figure 4
|Delta VOD|	Change in |VOD| between "0" and "1"	Rload = 100Ω	0	50	mV	–
|Delta VOS|	Change in |VOS| between "0" and "1"	Rload = 100Ω	0	200	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.2	mA	–
ISAB	Output current	Drivers shorted together	2.6	4.8	mA	–
Rbias	Bias resistor	–	16.3	16.7	kΩ	1 per chip
Ibias	Bias static current	–	7	14.6	mA	–
F Max.	Maximum operating frequency	VDD = 2.5V ± 0.2V	–	220	MHz	Consumption 14.8 mA
Clock	Clock signal duty cycle	Max. frequency	45	55	%	–
Tfall	Fall time 80-20%	Rload = 100Ω	445	838	ps	see Figure 4
Trise	Rise time 20-80%	Rload = 100Ω	445	841	ps	see Figure 4
Tp	Propagation delay	Rload = 100Ω	1120	2120	ps	see Figure 4
Tsk1	Duty cycle skew	Rload = 100Ω	0	80	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

Figure 4. Test Termination Measurements



$$OS = \frac{(VA + VB)}{2}$$

Figure 5. Rise and Fall Measurements



Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 15. LVDS Receiver DC/ AC Characteristics (preliminary)

Symbol	Parameter	Test Condition	Min.	Max.	Units	Comments
T_A	Operating Temperature	–	-55	125	°C	–
V_{DD}	Supply Voltage	–	2.3	3.6	V	–
Vi	Input voltage range	–	0	2400	mV	–
Vidth	Input differential voltage	–	-100	+100	mV	–
Tp	Propagation delay	Cout = 50 fF, VDD = 2.5V ± 0.2V Cout = 50 fF, VDD = 3.0V ± 0.3V Cout = 50 fF, VDD = 3.3V ± 0.3V	0.9 0.7 0.7	3.5 2.7 2.4	ns	–
Tskew	Duty cycle distortion	Cout = 50 fF	-	500	ps	–

Table 16. I/O Buffers DC Characteristics

Symbol	Parameter	Test Condition	Typical	Units
C_{IN}	Capacitance, Input Buffer (die)	3V	2.4	pF
C_{OUT}	Capacitance, Output Buffer (die)	3V	5.6	pF
$C_{I/O}$	Capacitance, Bi-Directional	3V	6.6	pF

Testability Techniques

For complex designs, involving blocks of memory and/or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs and the number of functional vectors that would need to be created to exercise them fully, strongly suggests the use of more efficient techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in-self-test logic must be employed, in addition to functional test patterns, to provide both the user and Atmel the ability to test the finished product.

An example of a highly complex design could include a PLL for clock management or synthesis, a microcontroller or DSP engine or both, SRAM to support the microcontroller or DSP engine, and glue logic to support the interconnectivity of each of these blocks. The design of each of these blocks must take into consideration the fact that the manufactured device will be tested on a high performance digital tester. Combinations of parametric, functional, and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

The type of block dictates the type of testability technique to be employed. The PLL will, by construction, provide access to key nodes so that functional and/or parametric testing can be performed. Since a digital tester must control all the clocks during the testing of a Gate Array/Embedded Array, provision must be made for the VCO to be bypassed. Atmel's PLLs include a multiplexing capability for just this purpose. The addition of a few pins will allow other portions of the PLL to be isolated for test, without impinging upon the normal functionality.

In a similar vein, access to microcontroller, DSP, and SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with the minimum amount of preconditioning. SRAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins provides a method for providing this accessibility.

The glue logic can be designed using full SCAN techniques to enhance its testability.

It should be noted that, in almost all of these cases, the purpose of the testability technique is to provide Atmel a means to assess the structural integrity of a Gate Array/Embedded Array, i.e., sort devices with manufacturing-induced defects. All of the techniques described above should be considered supplemental to a set of patterns which exercise the functionality of the design in its anticipated operating modes.

Advanced Packaging

The MH1RT Series gate arrays are offered in a wide variety of standard ceramic packages, including quad flatpacks (CQFP), multi layers quad flatpacks (MQFP), pin grid arrays (CPGA) and a BGA based on ceramic land grid arrays (CLGA). High volume onshore and offshore contractors can provide assembly and test for commercial or industrial quality grades, when agreed. Custom package designs are also available as required to meet a customer's specific needs, and are supported through Atmel's package design center. When a standard package cannot meet a customer's need, a package can be designed to precisely fit the application and to maintain the performance obtained in silicon. Atmel has delivered custom-designed packages in a wide variety of configurations.

Table 17. Packaging Options

Package Type	Pin Count
PQFP(1)	44 to 304
Power Quad(1)	144 to 304
L/TQFP(1)	32 to 216
PBGA(1)	121 to 676
MQFP	84 to 352
CLGA(1)	349, 472, 564 (1.27 mm pitch)

Note: 1. Contact Atmel for availability.

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