GENERAL DESCRIPTION

The M926-02 is a PLL (Phase Locked Loop) based clock generator that uses an internal VCSO (Voltage Controlled SAW Oscillator) to produce a very low jitter output clock. From the **M926-02-622.0800**, an output clock frequency of 622.08 or 155.52MHz is provided from six LVPECL clock output pairs. (Other frequencies are available; consult factory.) The accuracy of the output frequency is assured by the internal PLL that phase-locks the internal VCSO to the reference input frequency (19.44MHz for the **M926-02-622.0800**). The input reference can either be an external crystal, utilizing the internal crystal oscillator, or a stable external clock source such as a packaged crystal oscillator.

FEATURES

- **Output clock frequency range 150MHz to 700MHz (Consult factory for frequency availability)**
- **Selectable divider chooses one of two frequencies**
- **Six identical LVPECL output pairs (same frequency)**
- **Jitter 0.7ps rms (@622.08MHz, over 12kHz-20MHz), typ.**
- **Ideal for OC-48/STM-16 clock reference**
- **Output-to-output skew < 100ps**
- **External XTAL or LVCMOS reference input**
- **Selectable external feed-through clock input**
- **STOP clock control (Logic 1 stops output clocks)**
- **Integrated SAW (surface acoustic wave) delay line**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

PIN ASSIGNMENT (9 x 9 mm SMT)

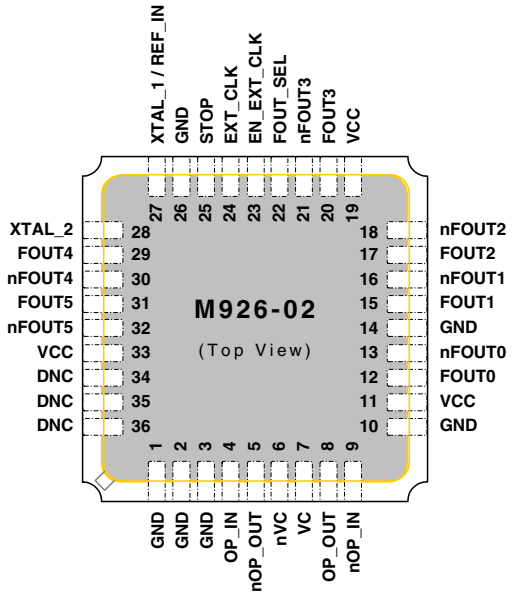


Figure 1: Pin Assignment

Example Output Frequency Configurations

(M926-02-622.0800)

Ref Clock Frequency (MHz)	VCSO Frequency (MHz)	P Divider Value	Output Frequency (MHz)
19.44	622.08	1	622.08
		4	155.52

Table 1: Example Output Frequency Configurations

SIMPLIFIED BLOCK DIAGRAM

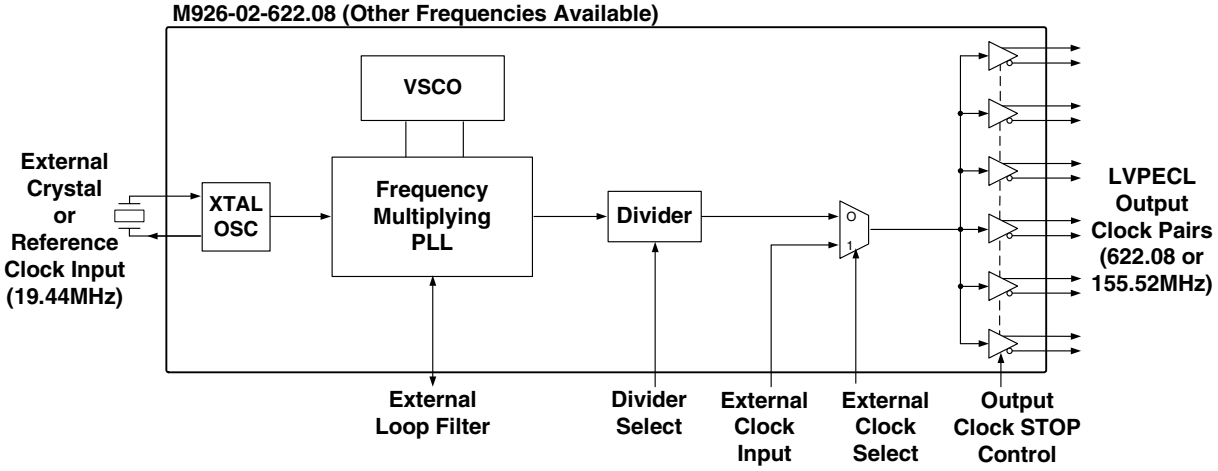


Figure 2: Simplified Block Diagram

DETAILED BLOCK DIAGRAM

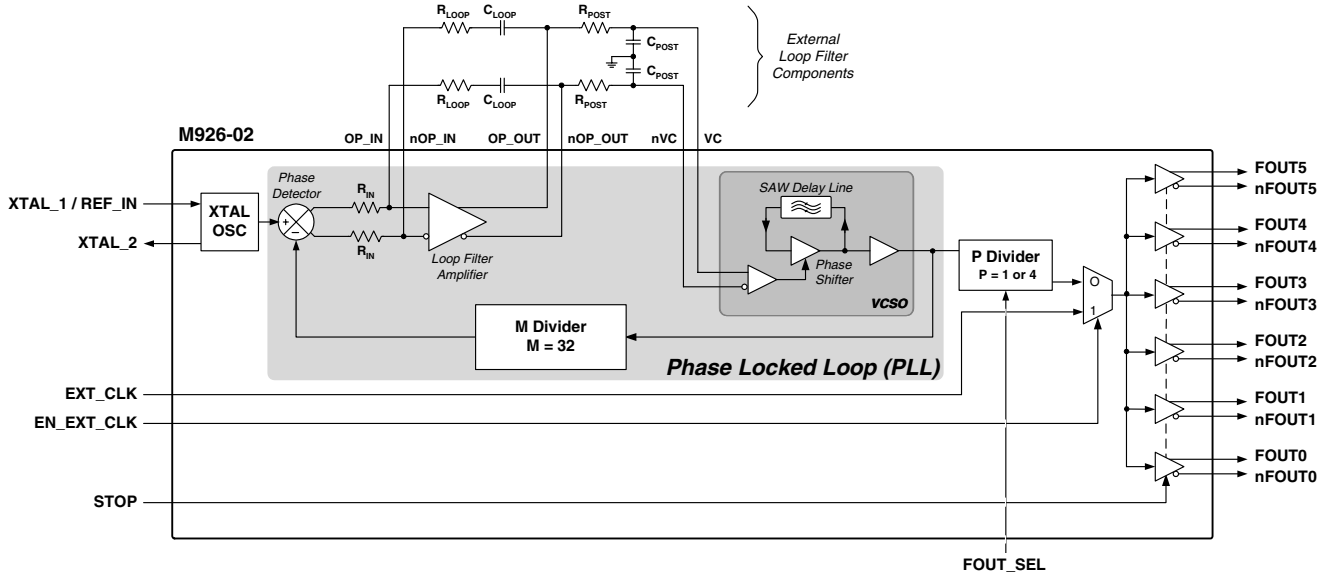


Figure 3: Detailed Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 5.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12, 13	FOUT0, nFOUT0	Output	No internal terminator	Clock output pairs, differential LVPECL output (622.08 or 155.52 MHz for the **M926-02-622.0800**)
15, 16	FOUT1, nFOUT1			
17, 18	FOUT2, nFOUT2			
20, 21	FOUT3, nFOUT3			
29, 30	FOUT4, nFOUT4			
31, 32	FOUT5, nFOUT5			
22	FOUT_SEL	Input		Determines post-PLL divider value: When FOUT_SEL = 0, P = 1 When FOUT_SEL = 1, P = 4
23	EN_EXT_CLK	Input	Internal pull-down resistor[1]	Logic 1 enables the EXT_CLK input. Use Logic 0 for normal operation.
24	EXT_CLK	Input		External clock feed-through: 0 to 200 MHz
25	STOP	Input	Internal pull-down resistor[1]	Logic 1 stops clock outputs. Use Logic 0 for normal operation.
27	XTAL_1 / REF_IN	Input		External crystal connection. Also accepts LVCMOS/LVTTL compatible clock source.
28	XTAL_2	Input		External crystal connection. Leave unconnected when driving pin 27 with external clock reference.
34, 35, 36	DNC		Do Not Connect.	Internal nodes. Connection to these pins can cause erratic device operation.

Table 2: Pin Descriptions

Note 1: For typical value of internal pull-down resistor, see **DC Characteristics**, **Pull-down** on pg. 6 for typical value.

FUNCTIONAL DESCRIPTION

The M926-02 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to an input reference clock.

The M926-02 combines the flexibility of a VCSO (Voltage Controlled SAW Oscillator) with the stability of a crystal oscillator.

Input Reference

The 19.44MHz input reference can either be an external, discrete crystal device or a stable external clock source such as a packaged crystal oscillator:

- If an external crystal is used with the on-chip crystal oscillator circuit (XTAL OSC), the external crystal should be a parallel-resonant, fundamental mode crystal. Apply it to the XTAL_1 / REF_IN and XTAL_2 input pins. External crystal load capacitors are also required.
- If an external LVCMOS/LVTTL clock source is used, apply it to the XTAL_1 / REF_IN input pin.

In either case, the reference clock is supplied directly to the phase detector of the PLL.

> *The* EX_CLK *pin is available for a clock feed-through mode for testing. See "External Clock Feed-through" on pg. 3.*

The PLL

The PLL (Phase Locked Loop) includes the phase detector, the VCSO, and a feedback divider (labeled "M Divider").

The feedback divider is a digital circuit that divides the VCSO output frequency by a numerical value "M" in order to match the input reference frequency.

By controlling the frequency and phase of the VCSO, the phase detector precisely locks the frequency and phase of the feedback divider output to that of the input reference. This creates an output frequency that is a multiple of the reference frequency (which is output from the VCSO).

The relationship between the VCSO output frequency, the M Divider, and the input reference frequency is defined as follows:

$$Fvcso = M \times Fxtal$$

For the **M926-02-622.0800** *(see "Ordering Information" on pg. 8):*

- VCSO output frequency = 622.08MHz
- M = 32
- Input reference frequency = 19.44MHz

Therefore, for the **M926-02-622.0800**:

$$622.08\text{MHz} = 32 \times 19.44\text{MHz}$$

The VCSO center output frequency of 622.08MHz enables the product of M × input crystal frequency to fall within the lock range of the VCSO.

Post-PLL Divider

The M926-02 also features a post-PLL divider (labeled "P Divider") for selecting one of two output frequencies (e.g., 622.08 or 155.52 MHz).

The FOUT_SEL pin determines the P Divider value:

- When FOUT_SEL = 0, P = 1.
- When FOUT_SEL = 1, P = 4.

External Clock Feed-through

The EXT_CLK pin provides an input for an external single-ended clock that directly drives the LVPECL clock outputs. This pin is intended for system debugging and performance evaluation..

EN_EXT_CLK	Logic 1 enables the EXT_CLK input. Use Logic 0 for normal operation.
EXT_CLK	Apply an external LVCMOS/LVTTL clock source for 0 to 200 MHz feed-through operation. Leave inactive for normal operation.[1]

Note 1: In applications where EXT_CLK is active while the SAW PLL signal path is enabled, it is necessary to gate the EXT_CLK to minimize jitter in the LVPECL output pairs. See the *PCB Design Guidelines for ICS SAW PLLs* application note at www.icst.com/products/appnotes/M000-AN-001.PCBdesign.pdf

STOP Clock

The STOP pin puts the output clock into a static condition.

Logic 1	Output clocks are static
Logic 0	Output clocks enabled for normal operation

APPLICATION INFORMATION

This section includes information on the optional external crystal and on the external loop filter.

The subsections on the loop filter provide example component values and also briefly describe the SAW PLL simulator tool and additional application information available at www.icst.com.

External Crystal Specifications

If an external crystal is used with the on-chip crystal oscillator circuit (XTAL OSC), the external crystal should have the following general specifications:

Crystal Specifications

	Parameter	Min	Typ	Max	Unit
	Crystal Type		AT-cut quartz		
	Mode of Oscillation		Fundamental		
f_0	Frequency Range	16		40	MHz
ESR	Equivalent Series Resistance			50	Ω
	Spurious Response (non-harmonic)			-40	dBc
C_L	Load Capacitance, parallel load resonant	16		32	pF
P_0	Drive Level	0.1		1.0	mW

Table 3: Crystal Specifications

The external crystal will be applied to the XTAL_1 / REF_IN and XTAL_2 input pins. External crystal load capacitors are also required.

Recommended External Crystal Configuration

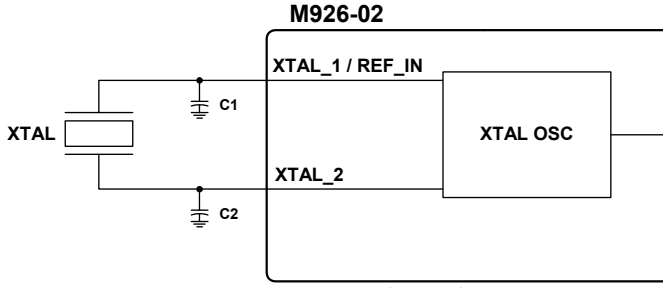


Figure 4: Recommended External Crystal Configuration

XTAL Load Capacitance Specification = 18 pF
C1 = 27 pF
C2 = 33 pF

External load capacitors C1 and C2 present a load of 15 pf to the crystal (they are seen in series by the crystal through the common ground connection). With the additional of PCB trace capacitance and M926-02 input capacitance, the total load to the crystal is about 18 pf.

External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M926-02 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 5).

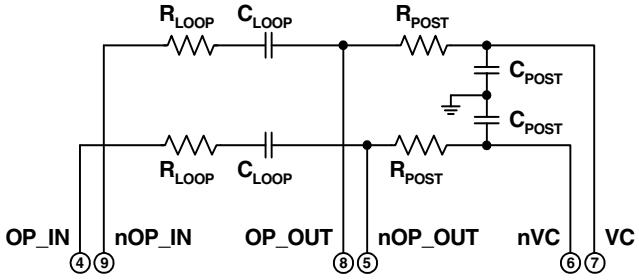


Figure 5: External Loop Filter

The loop filter is implemented as a differential circuit to minimize system noise interference. Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here. See Table 4, Example External Loop Filter Component Values, below.

Example External Loop Filter Component Values

PLL Bandwidth (kHz)	Damping Factor	R loop (kΩ)	C loop (µF)	R post (kΩ)	C post (pF)
0.395	2.0	1.5	4.70	20	3300
1.2	2.9	4.7	1.00	20	1000
10 [1]	2.4	39.0	0.01	20	240

Table 4: Example External Loop Filter Component Values

Note 1: Recommended for minimum output jitter when using a crystal or crystal oscillator reference.

Refer to the M926-02 product web page at www.icst.com/products/summary/m926-02.htm for additional product information.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

Refer to the SAW PLL Simulator Software web page at www.icst.com/products/calculators/m2000filterSWdesc.htm for additional information.

SAW PLL Application Notes Available

The ICS web site (www.icst.com) also has application notes on:

- PCB layout guidelines (including special detailed instructions for preventing issues such as external reference crosstalk)
- Any new special device application details that may become available
- Instructions for using PLL simulator software
- Guidelines for PCB fabrication (including recommended PCB footprint, solder mask, and furnace profile)

Refer to the SAW PLL Application Notes web page at www.icst.com/products/appnotes/SawPllAppNotes.htm for application notes and any additional product information that may become available.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 5: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature	Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 6: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = 622.08MHz,[1] LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
	I_{CC}	Power Supply Current			350		mA
Logic Inputs	V_{IH}	Input High Voltage	FOUT_SEL, EN_EXT_CLK, EXT_CLK, STOP	2		V_{cc} +0.3	V
	V_{IL}	Input Low Voltage		-0.3		0.8	V
	I_{IH}	Input High Current				150	µA
	I_{IL}	Input Low Current		-5.0			µA
Reference Clock Input	V_{IH}	Input High Voltage	XTAL_1 / REF_IN (XTAL_2 disconnected)	(V_{cc} / 2) +0.5		V_{cc} +0.3	V
	V_{IL}	Input Low Voltage		-0.3		(V_{cc} / 2) +0.5	V
	I_{IH}	Input High Current				150	µA
	I_{IL}	Input Low Current		-5.0			µA
All Inputs	C_{IN}	Input Capacitance, All Inputs	FOUT_SEL, EN_EXT_CLK, EXT_CLK, STOP, XTAL_1 / REF_IN			4	pF
Pull-down	$R_{pulldown}$	Internal Pull-down Resistor	EN_EXT_CLK, STOP		51		kΩ
Differential Output	V_{OH}	Output High Voltage	FOUT, nFOUT (0-5)	V_{cc} -1.4		V_{cc} -1.0	V
	V_{OL}	Output Low Voltage		V_{cc} -2.0		V_{cc} -1.7	V
	V_{P-P}	Peak to Peak Output Voltage		0.6		0.85	V

Table 7: DC Characteristics

Note 1: For other VCSO center frequencies, contact ICS

AC Characteristics

Unless implied otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = 622.08MHz,[1] LVPECL outputs terminated with 50Ω to V_{CC} - 2V

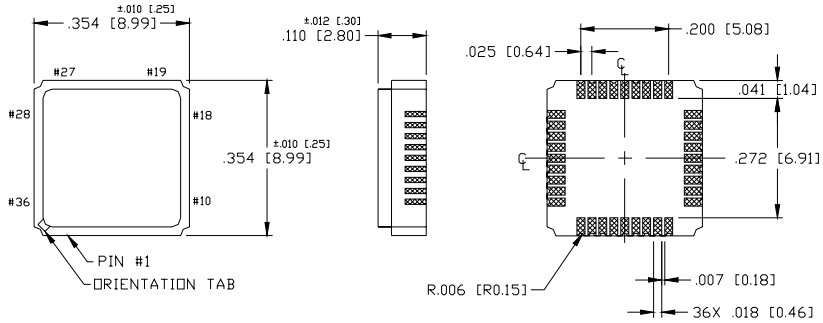
Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions
F_{OUT}	Output Frequency Range		75		175	MHz	FOUT_SEL=1 [1]
F_{IN}	Nominal Input Frequency, XTAL_1 / REF_IN			19.44		MHz	
APR	VCSO Pull-Range		±100	±150		ppm	
Φn	Single Side Band Phase Noise @622.08MHz	1kHz Offset		-100		dBc/Hz	
		10kHz Offset		-110		dBc/Hz	
		100kHz Offset		-134		dBc/Hz	
J(t)	Jitter (rms)			0.7	1.0	ps	12kHz to 20MHz
t_{DC}	Output Duty Cycle, High Time		45	50	55	%	
t_R	Output Rise Time	FOUT, nFOUT (0-5)	200	275	350	ps	20% to 80%
t_F	Output Fall Time	FOUT, nFOUT (0-5)	200	275	350	ps	20% to 80%
t_S	Output Skew	Between Any Pair			100	ps	
	EXT_CLK Frequency	EXT_CLK	0		200	MHz	

Table 8: AC Characteristics

Note 1: For other VCSO center frequencies, contact ICS

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:



Refer to the SAW PLL application notes web page at www.icst.com/products/appnotes/SawPllAppNotes.htm for application notes, including recommended PCB footprint, solder mask, and furnace profile.

NOTES:
1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ±.005 [.13]

Figure 6: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

Part Numbering Scheme

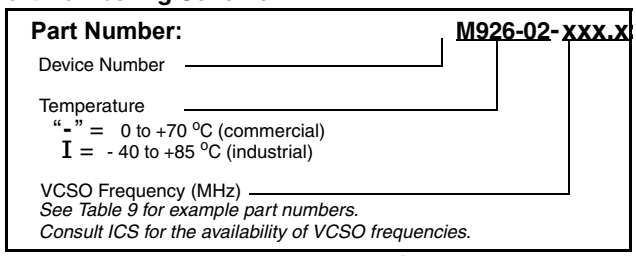


Figure 7: Part Numbering Scheme

Example Part Numbers

For Output Frequencies (MHz)	Temperature	Order Part Number
622.08 (and 155.52)	commercial	**M926-02-622.0800**
	industrial	**M926-02I622.0800**
600 to 700 (and 150 to 187.5)	commercial	**M926-02-xxx.xxxx**
	industrial	**M926-02Ixxx.xxxx**

Table 9: Example Part Numbers

Consult ICS for the availability of VCSO frequencies