32 K × 8 Very Low Power CMOS SRAM Rad Tolerant

Introduction

The M65656G is a very low power CMOS static RAM organized as 32768 × 8 bits.

Atmel Wireless & Microcontrollers brings the solution for applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments or embarked systems.

Using an array of six transistors (6T) memory cells, the M65656G combines an extremely low standby supply current (Typical value = 0.1 µA) with a fast access time at 40 ns. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

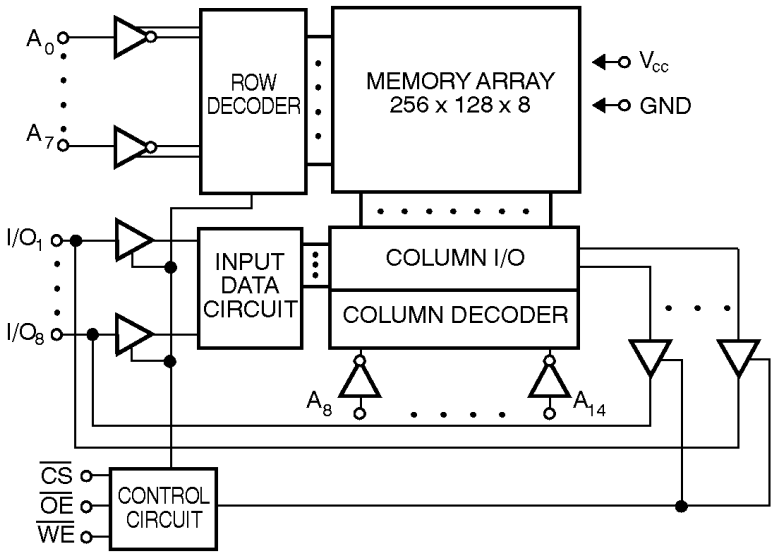
The M65656G is processed according to the methods of the latest revision of the MIL STD 883 (class B or S), ESA SCC 9000 and QML.

Features

- Access time
  40, 55 ns
- Very low power consumption
  active : 50 mW (typ)
  standby : 0.5 µW (typ)
  data retention : 0.4 µW (typ)
- Wide temperature range : –55 to + 125°C
- 300 and 600 mils width package
- TTL compatible inputs and outputs
- Asynchronous
- Single 5 volt supply
- Equal cycle and access time
- Gated inputs : no pull-up/down resistors are required

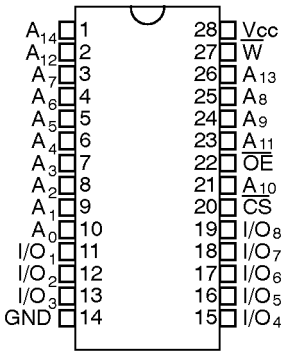
Interface

Block Diagram



Pin Configuration

Side Brazed 300 mils 28 pins
Multilayer Flat Pack 28 pins 400 mils



(Top View)

Pin Names

A_0-A_{14} :	Address inputs	$\overline{CS}$:	Chip-Select
I/O0-I/O7 :	Input/Output	$\overline{W}$:	Write Enable
V_{CC} :	Power	$\overline{OE}$:	Output Enable
GND :	Ground		

Truth Table

$\overline{CS}$	$\overline{W}$	$\overline{OE}$	INPUTS/ OUTPUTS	MODE
H	X	X	Z	Deselect/ POWER-DOWN
L	H	L	DATA OUT	Read
L	L	X	DATA IN	Write
L	H	H	Z	Output Disable

L = low, H = high, X = H or L, Z = high impedance

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : . . . . . -0.3 V to + 7.0 V
Input or Output voltage applied : . . . . . (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : . . . . . –65 ºC to + 150 ºC
Electro static discharge voltage . . . . . > 2000 V (MIL STD 883, METHOD 3015)

Operating Range

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	V_{CC} = 5 V ± 10 %	– 55 °C to + 125 °C

DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH(1)	input high voltage	2.2	–	Vcc + 0.3	V

Note : 1. VIH max = Vcc + 0.3 V, VIL min = –0.3 V or –1.0 pulse 50 ns.

Capacitance

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	8	pF
Cout (2)	Output capacitance	–	–	12	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

DC Parameter

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (3)	Input leakage current	– 1.0	–	1.0	µA
IOZ (3)	Output leakage current	– 1.0	–	1.0	µA
VOL (4)	Output low voltage	–	–	0.4	V
VOH (4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 4 mA, IOH = –1.0 mA.

Consumption

SYMBOL	PARAMETER	M65656G V – 45	M65656G V – 55	UNIT	VALUE
ICCSB (5)	Standby supply current	5	5	mA	max
ICCSB1 (6)	Standby supply current	100	100	µA	max
ICCOP (7)	Operating supply current	85	85	mA	max

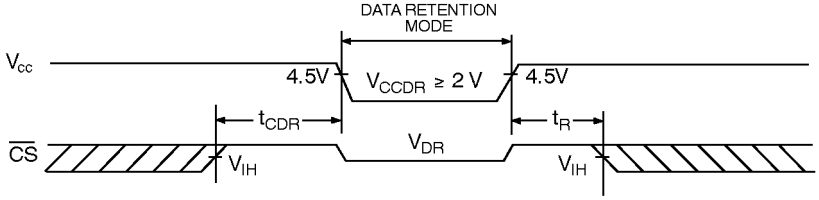
Notes : 5. $\overline{CS}$ ≥ VIH, Vin ≥ VIH or Vin ≤ VIL.
6. $\overline{CS}$ ≥ Vcc – 0.3 V, Iout = 0 mA. Vin ≥ Vcc – 0.3 V or Vin ≤ 0.3 V.
7. Vcc max, Iout = 0 mA, Vin = Gnd/Vcc. Duty cycle 100 %, F = 5 MHz, derating = 12 mA/MHz.

Data Retention Mode

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc – 0.2 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ must be kept between Vcc -0.3 V and 70 % of Vcc during the power up and power down transitions.
4. The RAM can begIn operation > TR after Vcc reaches the minimum operating voltage (4.5 V).

Timing



Data Retention Characteristics

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (8)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (9)	–	–	ns
ICCDR1 (10)	Data retention current @ 2.0 V : M-65656GV		0.1	80	µA
ICCDR2 (10)	Data retention current @ 3.0 V : M-65656GV		0.3	90	µA

Notes : 8. TA = 25°C.
9. TAVAV = Read cycle time.
10. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested at Vcc = 2 V.

AC Parameters

AC Conditions

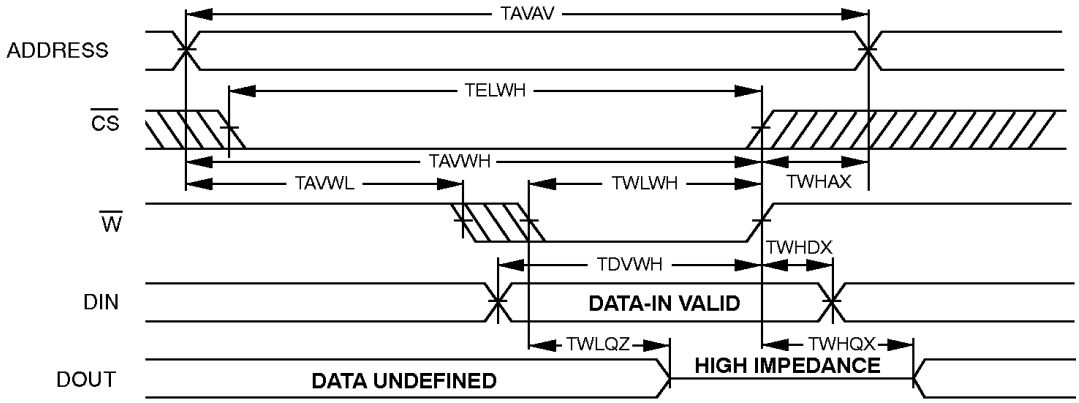
Input pulse levels : . . . . . Gnd to 3.0 V
Input rise : . . . . . 5 ns
Input timing reference levels : . . . . . 1.5 V
Output load : . . . . . See fig. 1a, 1b

Write Cycle

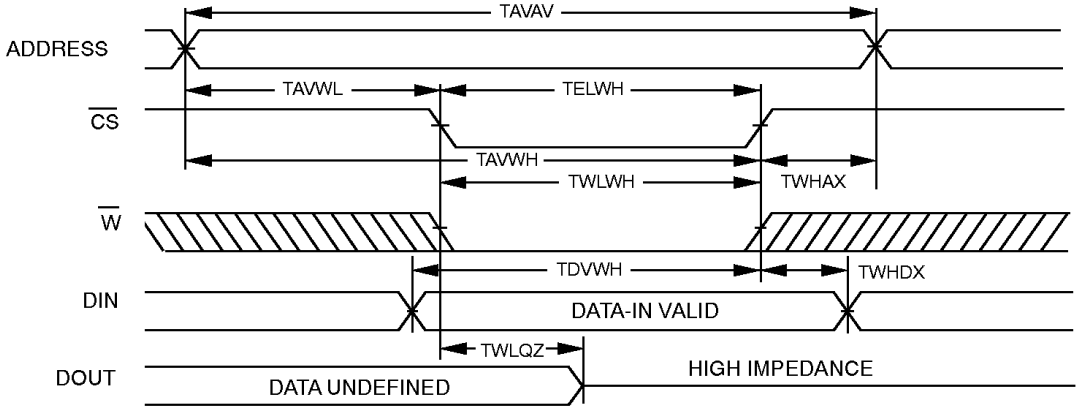
SYMBOL	PARAMETER	M65656G – 40	M65656G – 55	UNIT	VALUE
TAVAV	Write cycle time	40	55	ns	min
TAVWL	Address set-up time	0	0	ns	min
TAVWH	Address valid to end of write	30	40	ns	min
TDVWH	Data set-up time	22	25	ns	min
TELWH	$\overline{CS}$ low to write end	30	40	ns	min
TWLQZ (11)	Write low to high Z	15	20	ns	max
TWLWH	Write pulse width	30	40	ns	min
TWHAX	Address hold to end of write	0	0	ns	min
TWHDX	Data hold time	0	0	ns	min
TWHQX (11)	Write high to low Z	0	0	ns	min

Notes : 11. Specified with C_L = 5 pF (see figure 1b). Guaranteed but not tested.

Write Cycle 1 : $\overline{W}$ Controlled (note 12)



Write Cycle 2 : $\overline{CS}$ Controlled (note 12)



Note : 12. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$ = VIH.

AC Test Loads and Waveforms

Figure 1 a

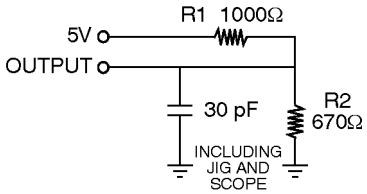


Figure 1 b

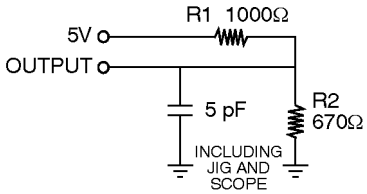
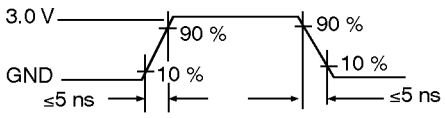
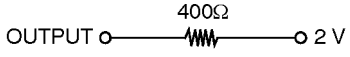


Figure 2



Equivalent to : THEVENIN EQUIVALENT

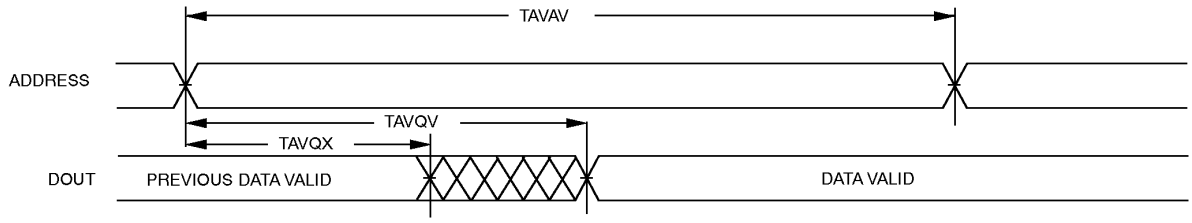


Read Cycle

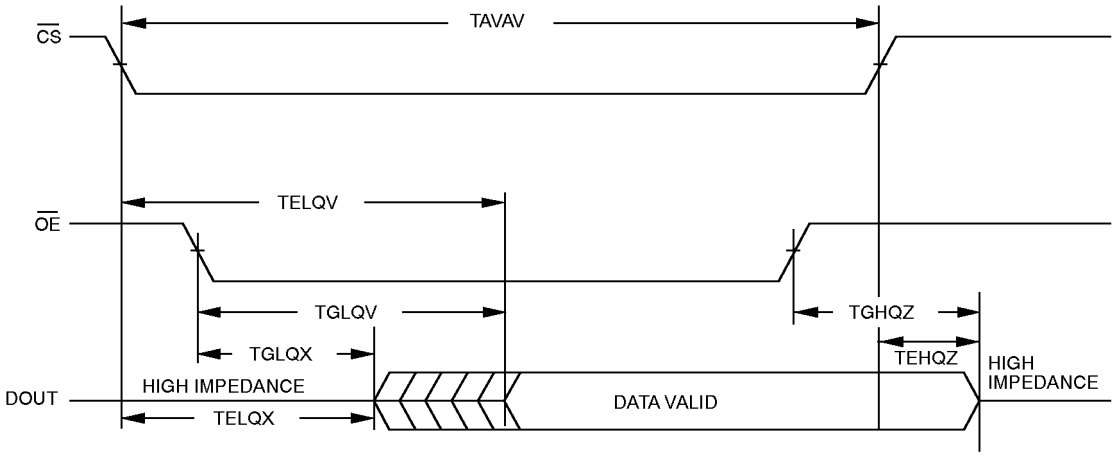
SYMBOL	PARAMETER	M65656G – 40	M65656G – 55	UNIT	VALUE
TAVAV	Read cycle time	40	55	ns	min
TAVQV	Address access time	40	55	ns	max
TAVQX	Address valid to low Z	5	5	ns	min
TELQV	Chip-select access time	40	55	ns	max
TELQX(13)	$\overline{CS}$ low to low Z	5	5	ns	min
TEHQZ(13)	$\overline{CS}$ high to high Z	15	15	ns	max
TGLQV	Output Enable access time	20	25	ns	max
TGLQX(13)	$\overline{OE}$ low to low Z	5	5	ns	min
TGHQZ(13)	$\overline{OE}$ high to high Z	15	20	ns	max

Notes : 13. Specified with C_L = 5 pF (see figure 1b). Guaranteed but not tested.

Read Cycle nb 1 (notes 14, 15)

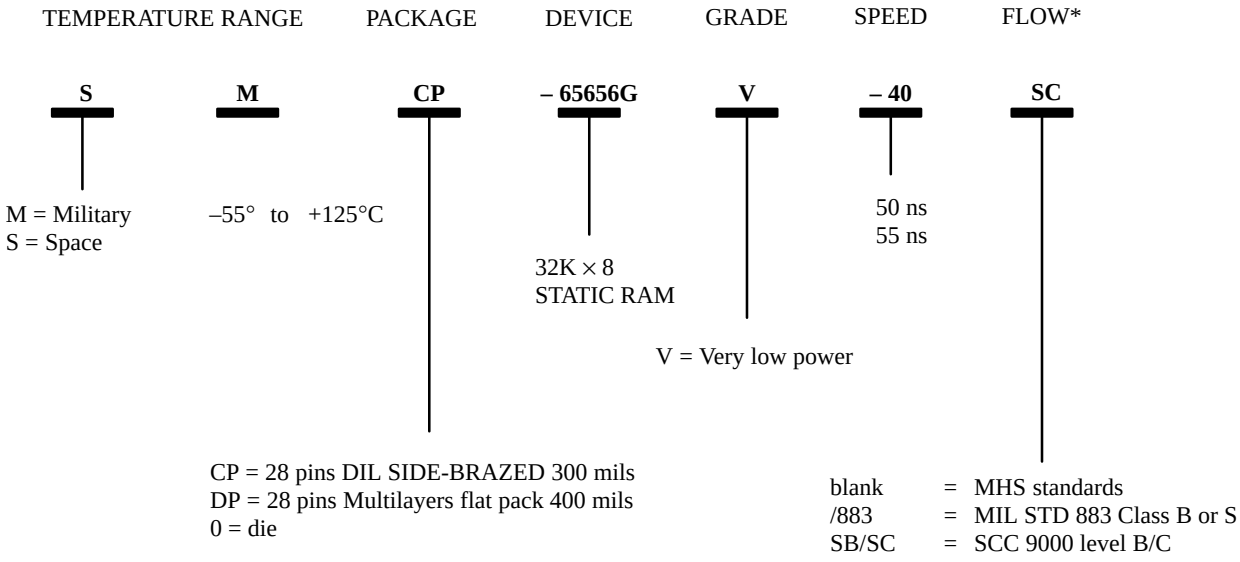


Read Cycle nb 2 (notes 14, 16)



Notes : 14. $\overline{W}$ is high for read cycle.
15. Device is continuously selected $\overline{CS}$ & $\overline{OE}$ = VIL.
16. Address valid prior to or coincident with $\overline{CS}$ transition low.

Ordering Information



* For ordering in QML quality level, use the QML PIN according to SMD number (to be defined).