PRELIMINARY

June 2004

LP3994

50mA CMOS Voltage Regulator with Enable Contol

General Description

The LP3994 regulator provides 1.5V and 1.8V outputs options at up to 50mA load current suitable for Bluetooth applications. Other voltage options up to 3.3V are available for general use within the range of portable, battery-powered equipment. The LP3994 provides an accurate output voltage with low quiescent current at full current. Good noise performance is obtained without a Noise Bypass Capacitor. The low quiescent current in operation can be reduced to virtually zero when the device is disabled via a logic signal to the enable input. In conjuction with small space saving capacitors, the small package size of the microSMD devices results in a regulator solution with a very small footprint for any given application.

The LP3994 also features short-circuit and thermal-shutdown protection.

Performance is specified for a -40°C to 125°C temperature range.

This device is available with output voltages of 1.5V and 1.8V in both microSMD and LLP packages, however other voltages and alternative packages may be made available, please contact your local NSC sales office.

Features

- 4 Pin MicroSMD Package/ 6 Pin LLP
- No Noise Bypass Capacitor Required
- Logic Controlled Enable
- Stable with Low ESR Ceramic Capacitors
- Fast turn ON
- Thermal-Overload and Short Circuit Protection

Key Specifications

■ Input Voltage Range 2.5 to 5.5V 1.5 to 3.3V ■ Output Voltage Range ■ Output Current 50mA ■ Noise Figure $95\mu V_{RMS}$ ■ PSRR 70dB ■ Fast Startup 10µs Output Capacitor 1µF Low ESR ■ Virtually Zero I_Q(Disabled) 0.001µA

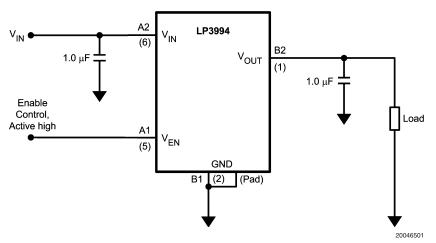
Package

Tiny 4 Pin micro SMD 1014μm by 1014μm by 600μm 6 pin LLP SOT23 footprint

Applications

- Bluetooth Devices
- Battery Powered Devices
- Portable Information Appliances

Typical Application Circuit

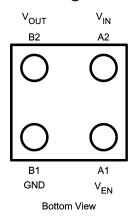


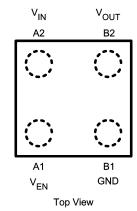
Pin Descriptions

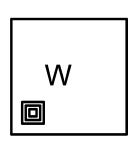
Packages micro SMD-4 and LLP-6

Pin No		Symbol	Name and Function		
micro	Pin No				
SMD	LLP				
A1	5	V _{EN}	Enable Input; Enables the Regulator when ≥ 1.2V		
			Disables the Regulator when ≤ 0.4V		
B1	2	GND	Common Ground		
B2	1	V _{OUT}	Voltage output. A 1.0µF Low ESR Capacitor should be connected		
			to this Pin. Connect this output to the load circuit.		
A2	6	V _{IN}	Voltage Supply Input. A 1.0µF capacitor should be connected at		
			this input.		
	3		No Connection. Do not connect to any other device pins.		
	4		No Connection. Do not connect to any other device pins.		

Connection Diagrams





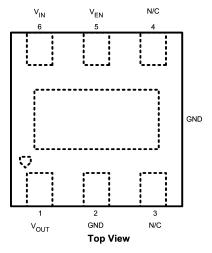


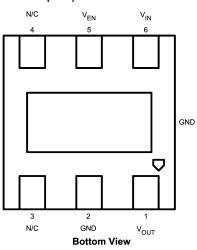
Top Marking

20046502

micro SMD-4 Package Top View See NS package number TLA04

LLP- 6 Package (SOT23 footprint)





20046507

Top View
See NS Package Number LDE06A

Ordering Information

For micro SMD Package

Please contact Sales Office for Availability

Output Voltage (V)	Grade	LP3994 Supplied as 1000 Units, Tape and Reel	LP3994 Supplied as 3000 Units, Tape and Reel
1.5	STD	LP3994TL-1.5	LP3994TLX-1.5
1.8	STD	LP3994TL-1.8	LP3994TLX-1.8

For microSMD Package (Lead Free)

Please contact Sales Office for Availability

Output Voltage (V)	Grade	LP3994 Supplied as 1000 Units, Tape and Reel	LP3994 Supplied as 3000 Units, Tape and Reel
1.5	STD	LP3994TL-1.5NOPB	LP3994TLX-1.5NOPB
1.8	STD	LP3994TL-1.8NOPB	LP3994TLX-1.8NOPB

For LLP Package

Please contact Sales Office for Availability

Output Voltage (V)	Grade	LP3994 Supplied as 1000 Units, Tape and Reel	LP3994 Supplied as 3000 Units, Tape and Reel	Package Marking
1.5	STD	LP3994LD-1.5	LP3994LDX-1.5	L028B
1.8	STD	LP3994LD-1.8	LP3994LDX-1.8	L029B

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage -0.3 to 6.5V

Output Voltage -0.3 to $(V_{IN} + 0.3V)$ to

6.5V (max)

Enable Input Voltage $-0.3 \text{ to } (V_{IN} + 0.3V) \text{ to}$

6.5V (max) Junction Temperature (T_J) Range

Junction Temperature 150°C

Lead Temp.

microSMD 260°C

LLP 235°C

Storage Temperature -65 to 150°C

Continuous Power

Dissipation(Note 3) Internally Limited

ESD Rating (Note 4)

Human Body Model 2KV
Machine Model 200V

Operating Conditions(Note 1)

Input Voltage 2.5 to 5.5V Enable Input Voltage 0 to $(V_{IN} + 0.3V)$ Junction Temperature (T_I) Range -40° C to 125° C

Ambient Temperature (T_A) Range

(Note 5) -40 to 85°C

Thermal Properties

Junction to Ambient Thermal Resistance(Note 6)

 θ_{JA} microSMD package 220°C/W θ_{JA} LLP package 88°C/W

Electrical Characteristics(Notes 2, 7)

Unless otherwise noted, $V_{EN} = 1.2$, $V_{IN} = V_{OUT} + 1.0V$, $C_{IN} = 1 \mu F$, $I_{OUT} = 1 mA$, $C_{OUT} = 1 \mu F$. Typical values and limits appearing in normal type apply for $T_J = 25$ °C. Limits appearing in **boldface** type apply over the full temperature range for operation, -40 to +125°C. (Notes 13, 14)

Symbol	Parameter		Conditions		Тур	Max	Units
Device Ou	tput: V _{OUT} ≤ 1.8V				•		
V _{IN}	Input Voltage			2.5		5.5	V
	Output Voltage Tolerance	Output Voltage Tolerance		-60		+60	mV
ΔV_{OUT}	Line Regulation Error	$V_{IN} = (V_{OUT(NC)})$ $I_{OUT} = 1mA$	$V_{IN} = (V_{OUT(NOM)} + 1.0V)$ to 5.5V, $I_{OUT} = 1$ mA		0.005	0.07	%/V
	Load Regulation Error	I _{OUT} = 1mA to	50mA		100	400	μV/mA
IQ	Quiescent Current	microSMD: I _{OUT} = 0mA			15	35	
			I _{OUT} = 50mA		22	50	
		LLP:	I _{OUT} = 0mA		15	40	μΑ
			I _{OUT} = 50mA		25	65	
	Quiescent Current(Disabled)	$V_{EN} = 0.4V$			0.001	1.5	1
Device Ou	tput: V _{OUT} > 1.8V	•			•		
V _{IN}	Input Voltage			2.5		5.5	V
ΔV_{OUT}	Output Voltage Tolerance	oltage Tolerance Over full line and load regulation.		-90		+90	mV
	Line Regulation Error	$V_{IN} = (V_{OUT(NOM)} + 1.0V)$ to 5.5V, $I_{OUT} = 1$ mA			0.005	0.1	%/V
	Load Regulation Error	I _{OUT} = 1mA to 50mA			100	500	μV/mA
	Dropout Voltage	I _{OUT} = 1mA			1.5	4.5	1,,
	(where applicable)	I _{OUT} = 50mA			75	140	mV
IQ	Quiescent Current	microSMD:	I _{OUT} = 0mA		18	50	μΑ
			I _{OUT} = 50mA		22	60	
		LLP:	I _{OUT} = 0mA		20	55	
		I _{OUT} = 50mA			22	65	1
	Quiescent Current(Disabled) V _{EN} = 0.4V			0.001	1.5		
Full V _{OUT} I	RANGE	•		•	•		
I _{LOAD}	Load Current	(Notes 8, 9)	(Notes 8, 9)				μΑ
I _{sc}	Short Circuit Current Limit	(Note 12)				235	mA

Electrical Characteristics(Notes 2, 7) (Continued)

Unless otherwise noted, $V_{EN} = 1.2$, $V_{IN} = V_{OUT} + 1.0V$, $C_{IN} = 1 \mu F$, $I_{OUT} = 1 mA$, $C_{OUT} = 1 \mu F$. Typical values and limits appearing in normal type apply for $T_J = 25$ °C. Limits appearing in **boldface** type apply over the full temperature range for operation, -40 to +125°C. (Notes 13, 14)

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
PSRR	Power Supply Rejection Ratio	f = 100Hz, I _{OUT} = 1mA to 50mA		70			
		f = 50kHz, I _{OUT} = 1mA to 50mA		30		-10	
		f = 1MHz, I _{OUT} = 1mA		50		dB	
		f = 1MHz, I _{OUT} = 50mA		40			
E _{EN}	Output noise Voltage (Note 9)	BW = 100Hz to 100kHz,		95		<u></u>	
		$V_{IN} = 4.2V$, $I_{OUT} = 1mA$				μV _{RMS}	
T _{SHUTDOWN}	Thermal Shutdown Temperature			160		°C	
	Thermal Shutdown Hysteresis			20			
Enable Conf	trol Characteristics		•				
I _{EN}	Maximum Input Current at	$V_{EN} = 0.0V$ and $V_{IN} = 5.5V$		0.015			
	V _{EN} Input			0.015		μA	
V _{IL}	Low Input Threshold	V _{IN} = 2.5V to 5.5V			0.4	V	
V _{IH}	High Input Threshold	V _{IN} = 2.5V to 5.5V	1.2			V	
Timing Char	racteristics		•				
T _{ON1}	Turn On Time (Note 9)	10 to 90% of V _{OUT(NOM)} (Note 10)		10	20	μS	
T _{ON2}		To 95% Level (Note 11)		35	100		
Transient	Line Transient Response δV _{OUT}	Figure 1 (Note 9)			20	mV	
Response	Load Transient Response δV _{OUT}	Figure 2 (Note 9)			70		

Note 1: Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All Voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage

Note 4: The human body is 100pF discharge through 1.5kW resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 5: In applications where high power dissipation and/or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature $(T_{J(max-op)})$, is dependant on the maximum operating junction temperature $(T_{J(max-op)})$, the maximum power dissipation $(P_{D(max)})$, and the junction to ambient thermal resistance in the application (θ_{JA}) . This relationship is given by :-

$$T_{A(max)} = T_{J(max-op)} - (P_{D(max)} x \theta_{JA})$$

See Applications section.

Note 6: Junction to ambient thermal resistance is highly application and board layout dependent. In applications where high maximum power dissipation exists, the thermal dissipation issues should be addressed in the board layout design.

Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 8: The device maintains the regulated output voltage without the load.

Note 9: This electrical specification is guaranteed by design.

Note 10: Time for V_{OUT} to rise from 10 to 90% of $V_{OUT(nom)}$. (figure 1)

Note 11: Time from $V_{EN} = 1.2V$ to $V_{OUT} = 95\%(V_{OUT(nom)})$.

Note 12: Short circuit current is measured on the input supply line at the point when the short circuit condition reduces the output voltage to 95% of its nominal value.

Note 13: CIN, and COUT: Low ESR surface mont devices used in setting electrical characteristics.

Note 14: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production at $T_J = 25^{\circ}C$ or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Output Capacitor, Recommended Specifications

Symbol	Parameter	Conditions	Min	Тур	Max	Units
C _o	Output Capacitor	Capacitance(Note 15)	0.7	1.0		μF
		ESR		5	500	mΩ

Note 15: The capacitor tolerance should be ±30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitor types are recommended to meet the full device temperature range, however X5R, Y5V, and Z5U types may be used with careful consideration of the application and its operating conditions. (See Capacitor Sections in Application Hints.)

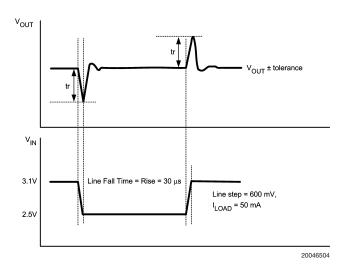


FIGURE 1. Line Transient Response Requirement.

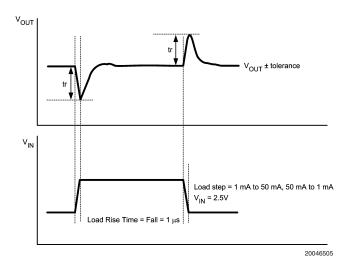
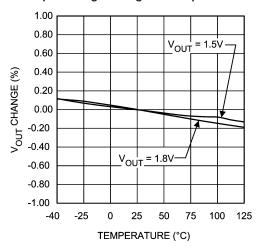


FIGURE 2. Load Transient Response Requirement.

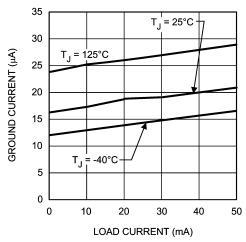
$\begin{tabular}{ll} \textbf{Typical Performance Characteristics.} & \textbf{Unless otherwise specified, } C_{IN} = C_{OUT} = 1.0 \ \mu F \ Ceramic, \\ V_{IN} = V_{OUT} + 1.0 V, T_A = 25 \ ^{\circ}C, \ V_{EN} \ pin \ is \ tied \ to \ V_{IN}. \\ \end{tabular}$

Output Voltage Change vs Temperature



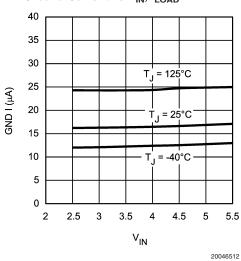
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Ground Current vs Load Current

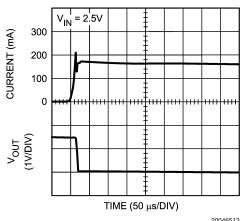


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Ground Current vs V_{IN} , $I_{LOAD} = 1mA$

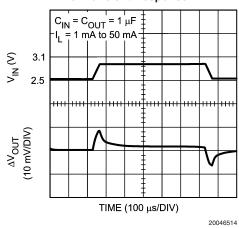


Short Circuit Current

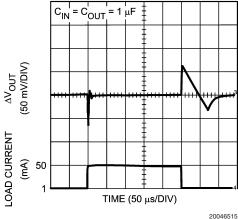


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Line Transient Response

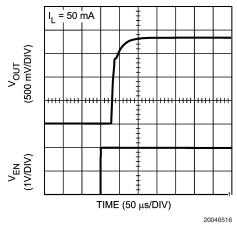


Load Transient Response

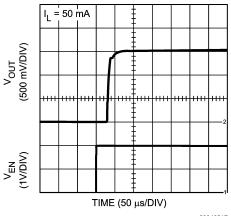


Typical Performance Characteristics. Unless otherwise specified, $C_{IN} = C_{OUT} = 1.0 \mu F$ Ceramic, $V_{IN} = V_{OUT} + 1.0V$, $T_A = 25^{\circ}C$, V_{EN} pin is tied to V_{IN} . (Continued)

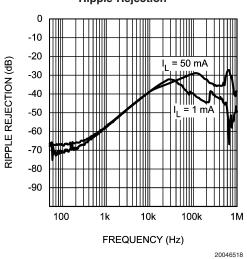
Enable Start Up Timing, $(V_{OUT} = 1.8V)$



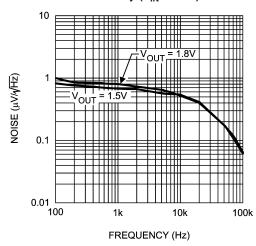
Enable Start Up Timing, $(V_{OUT} = 1.5V)$



Ripple Rejection



Noise Density (V_{IN} = 4.2V)



20046519

Application Hints

EXTERNAL CAPACITORS

In common with most regulators, the LP3994 requires external capacitors for regulator stability. The LP3994 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance and to ensure that their value remains within specification over the full operating range.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a $1.0\mu F$ capacitor be connected between the LP3994 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain $\simeq 1.0 \mu F$ over the entire operating temperature range.

OUTPUT CAPACITOR

Correct selection of the output capacitor is essential to ensure stable operation in the intended application.

The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. These conditions include DC-Bias, frequency and temperature. Unstable operation may result if the capacitance drops below the minimum specified value. (See the Capacitor Characteristics section).

The LP3994 is designed specifically to work with very small ceramic output capacitors. A 1.0µF ceramic capacitor (dielectric type X7R) with ESR between $5m\Omega$ to $500m\Omega$, is suitable in the LP3994 application circuit. X5R type capacitors may be used but have a narrower temperature range. With these capacitors and others types (Y5v, Z6U) that may be used, selection of the capacitor for any application is dependant on the range of operating conditions and temperature range for that application. (see section on Capacitor Characteristics).

It may also be possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

It is also recommended that the output capacitor be placed within 1cm from the output pin and returned to a clean ground line.

NO-LOAD STABILITY

The LP3994 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3994 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values around the $1\mu F$ value, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area. Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical $1\mu F$ ceramic capacitor is in the range of $20m\Omega$ to $40m\Omega$, which easily meets the ESR requirement for stability for the LP3994.

For both input and output capacitors careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general. A study of manufacturers data on 0402 case size capacitors shows that these devices may drop below the minimum specified capacitance due to DC-Bias conditions in conjunction with other parameters such as temperature and are thus not recommended for use.

The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of $\pm 15\%$ over the temperature range -55°C to +125°C. The X5R has a similar tolerance over the reduced temperature range of -55°C to +85°C. Most large value ceramic capacitors ($\geq 2.2\mu F$) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C. Therefore X7R is recommended over these other capacitor types in applications where the temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the $1\mu F$ to $4.7\mu F$ range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

Application Hints (Continued)

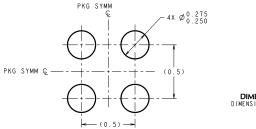
ENABLE

The LP3994 features an active high Enable pin, $V_{\rm EN}$, which turns the device on when pulled high. When not enabled the regulator output is off and the device typically consumes 1nA.

If the application does not require the Enable switching feature, the V_{EN} pin should be tied to V_{IN} to keep the regulator output permanently on.

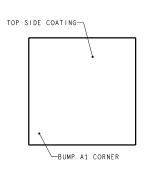
To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and $V_{\text{IH}}.$

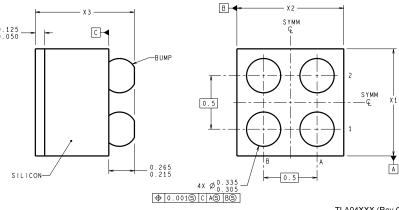
Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



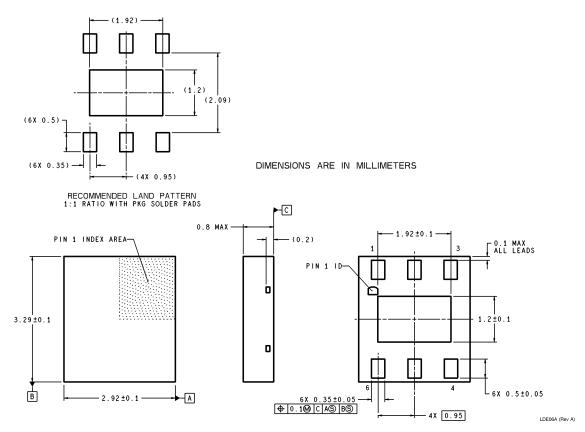


TLA04XXX (Rev C)

micro SMD, 4 Bump, Package (TLA04)
NS Package Number TLA04AAA
The dimensions for X1, X2 and X3 are given as:

X1 = 1.014 +/- 0.03mm X2 = 1.014 +/- 0.03mm X3 = 0.600 +/- 0.075mm

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LLP, 6 Lead, Package (SOT23 Land)
NS Package Number LDE06A

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