National Semiconductor

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LM2633
Advanced Two-Phase Synchronous Triple Regulator Controller for Notebook CPUs

General Description

The LM2633 is a feature-rich IC that combines three regulator controllers - two current mode synchronous buck regulator controllers and a linear regulator controller.

The two switching regulator controllers operate 180˚ out of phase. This feature reduces the input ripple RMS current, resulting in a smaller input filter.

The first switching controller (Channel 1) features an Intel mobile CPU compatible precision 5-bit digital-to-analog converter which programs the output voltage from 0.925V to 2.00V. It is also compatible with the dynamic VID requirements. The second switching controller (Channel 2) is adjustable between 1.25V to 6.0V.

Use of synchronous rectification and pulse-skip operation at light load achieves high efficiency over a wide load range. Fixed-frequency operation can be obtained by disabling the pulse-skip mode.

Current-mode feedback control assures excellent line and load regulation and a wide loop bandwidth for good response to fast load transient events. Current mode control is achieved through sensing the Vds of the top FET and thus an external sense resistor is not necessary.

A power good signal is available to indicate the general health of the output voltages.

A unique feature is the analog soft-start for the switching controllers is independent of the slew rate of the input voltage. This will make the soft start behavior more predictable and controllable. An internal 5V rail is available externally for boot-strap circuitry (only) when no 5V is available from other sources.

Current limit for either of the two switching channels is achieved through sensing the top FET V_{DS} and the value is adjustable. The two switching controllers have under-voltage and over-voltage latch protections, and the linear regulator has under-voltage latch protection. Under-voltage latch can be disabled or delayed by a programmable amount of time.

The input voltage for the switching channels ranges from 5V to 30V, which makes possible the choice of different battery chemistries and options.

Features

GENERAL

- Three regulated output voltages
- 4.5V to 30V input range
- Power good function
- Input under-voltage lockout
- Thermal shutdown
- Tiny TSSOP package

SWITCHING SECTION

- Two channels operating 180˚ out of phase
- Separate on/off control for each channel
- Current mode control without sense resistor
- Skip-mode operation available
- Adjustable cycle-by-cycle current limit
- Negative current limit
- Analog soft start independent of input voltage slew rate
- Power ground pins separate
- Output UVP and OVP
- Programmable output UVP delay
- 250kHz switching frequency (for Vin < 17V)
- Channel 1 output from 0.925V to 2.00V
- ±1.5% DAC accuracy from 0˚C to 125˚C
- ±1.5% initial tolerance for Channel 2
- Dynamic VID change ready
- Power good flags VID changes
- Channel 2 output from 1.3V to 6.0V

LINEAR SECTION

- Output voltage adjustable
- 50mA maximum driving current
- Output UVP
- ±2% initial tolerance

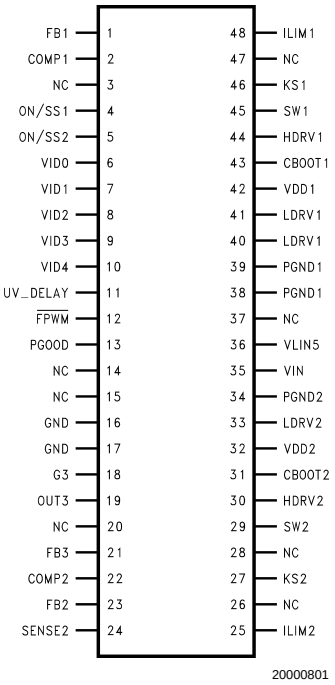
Applications

- Power supply for CPUs of notebook PCs that require the SpeedStep™ technique
- Power supply for information appliances
- General low voltage DC/DC buck regulators

SpeedStep™ is a trademark of Intel Corporation.

Connection Diagram

TOP VIEW



48-Lead TSSOP (MTD)
Order Number LM2633MTD
See NS Package Number MTD48

Pin Descriptions

FB1 (Pin 1): The feedback input for Channel 1. Connect to the load directly.

COMP1 (Pin 2): Channel 1 compensation network connection (connected to the output of the voltage error amplifier).

NC (Pins 3, 14, 15, 20, 26, 28, 37 and 47): No internal connection.

ON/SS1 (Pin 4): Adding a capacitor to this pin provides a soft-start feature which minimizes inrush current and output voltage overshoot; A lower than 0.8V input (open-collector type) at this pin turns off Channel 1; also if both ON/SS1 and ON/SS2 pins are below 0.8V, the whole IC goes into *shut down mode*.

ON/SS2 (Pin 5): Adding a capacitor to this pin provides a soft-start feature which minimizes inrush current and output voltage overshoot; A lower than 0.8V input (open-collector type) at this pin turns off Channel 2; also if both ON/SS1 and ON/SS2 pins are below 0.8V, the whole IC goes into *shut down mode*.

VID4-0 (Pins 6-10): Voltage identification code. Each pin has an internal pull-up. They can accept open collector compatible 5-bit binary code from the CPU. The code table is shown in *Table 3*.

UV_ DELAY (Pin 11): A capacitor from this pin to ground adjusts the delay for the output under-voltage lockout.

$\overline{\text{FPWM}}$ (Pin 12): When $\overline{\text{FPWM}}$ is low, pulse-skip mode operation at light load is disabled. The regulator is forced to operate in constant frequency mode.

PGOOD (Pin 13): : A constant monitor on the output voltages. It indicates the general health of the regulators. For more information, *see Power Good Truth Table (Table 2*) and *Power Good Function* in *Operation Descriptions*.

GND (Pin 16-17): Low-noise analog ground.

G3 (Pin 18): Connect to the base or gate of the linear regulator pass transistor.

OUT3 (Pin 19): Connect to the output of the linear regulator.

FB3 (Pin 21): The feedback input for the linear regulator, connected to the center of the external resistor divider.

COMP2 (Pin 22): Channel 2 compensation network connection (it's the output of the voltage error amplifier).

FB2 (Pin 23): The feedback input for Channel 2. Connect to the center of the output resistor divider.

SENSE2 (Pin 24): Remote sense pin of Channel 2. This pin is used for skip-mode operation.

ILIM2 (Pin 25): Current limit threshold setting for Channel 2. It sinks at a constant 10 µA current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 2.

KS2 (Pin 27): The Kelvin sense for the drain of the top MOSFET of Channel 2.

SW2 (Pin 29): Switch-node connection for Channel 2, which is connected to the source of the top MOSFET.

HDRV2 (Pin 30): Top gate-drive output for Channel 2. HDRV2 is a floating drive output that rides on SW2 voltage.

CBOOT2 (Pin 31): Bootstrap capacitor connection for Channel 2 top gate drive. It is the positive supply rail for Channel 2 top gate drive.

VDD2 (Pin 32): The supply rail for Channel 2 bottom gate drive.

LDRV2 (Pin 33): Bottom gate-drive output for Channel 2.

PGND2 (Pin 34): Power ground for Channel 2.

VIN (Pin 35): The regulator input voltage supply.

VLIN5 (Pin 36): The output of the internal 5V linear regulator. Bypass to the ground with a 1UF ceramic capacitor. When regulator input voltage is 5V, this pin can be tied to VIN pin to improve light-load efficiency.

PGND1 (Pin 38-39): Power ground for Channel 1.

LDRV1 (Pin 40-41): Bottom gate-drive output for Channel 1.

VDD1 (Pin 42): The supply rail for the Channel 1 bottom gate drive.

CBOOT1 (Pin 43): Bootstrap capacitor connection for Channel 1 top gate drive. It is the positive supply rail for Channel 1 top gate drive.

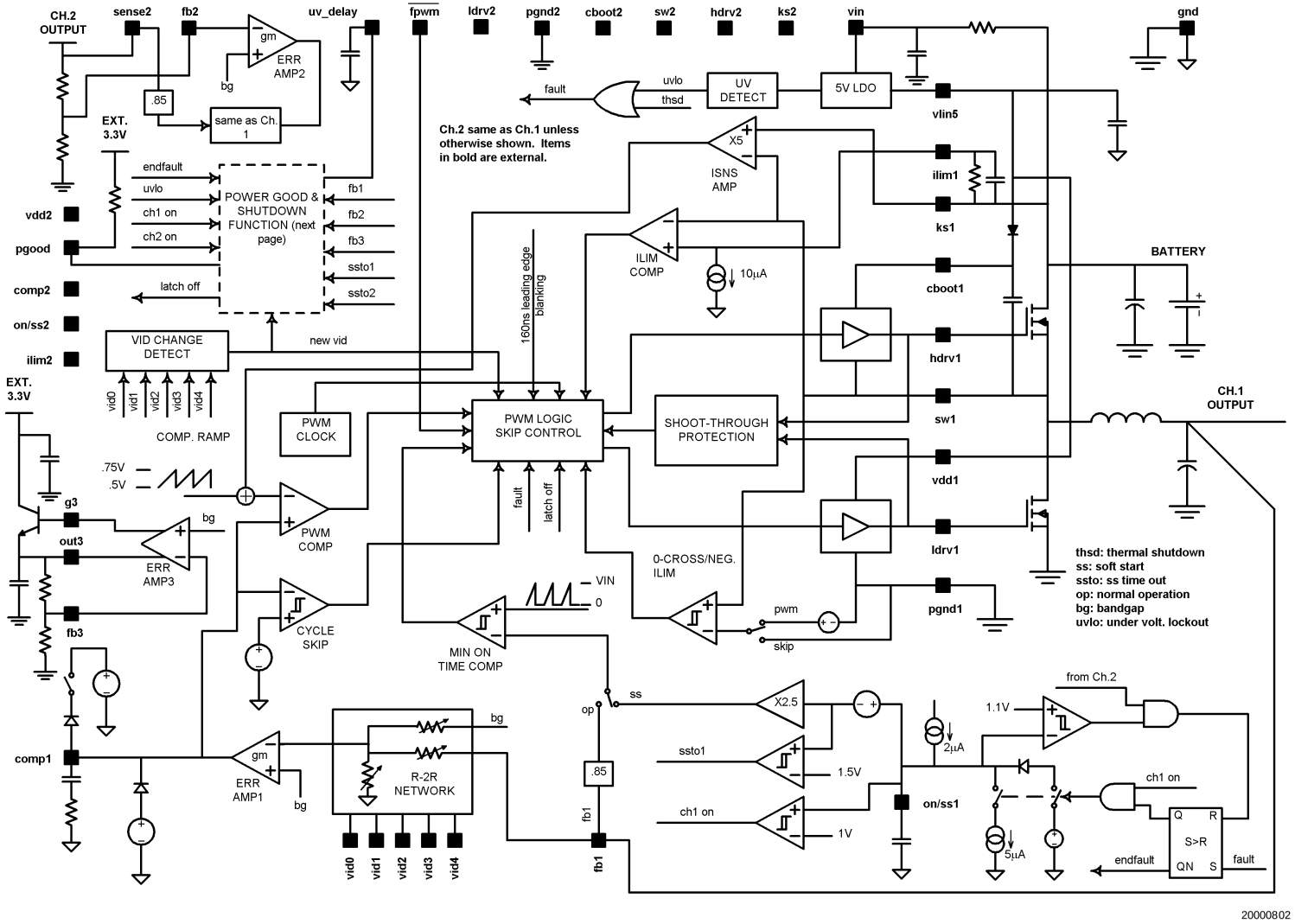
HDRV1 (Pin 44): Top gate-drive output for Channel 1. HDRV1 is a floating drive output that rides on SW1 voltage.

SW1 (Pin 45): Switch-node connection for Channel 1, which is connected to the source of the top MOSFET.

KS1 (Pin 46): The Kelvin sense for the drain of the top MOSFET of Channel 1.

ILIM1 (Pin 48): Current limit threshold setting for Channel 1. It sinks at a constant 10 µA current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 1.

Block Diagram



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Block Diagram (Continued)

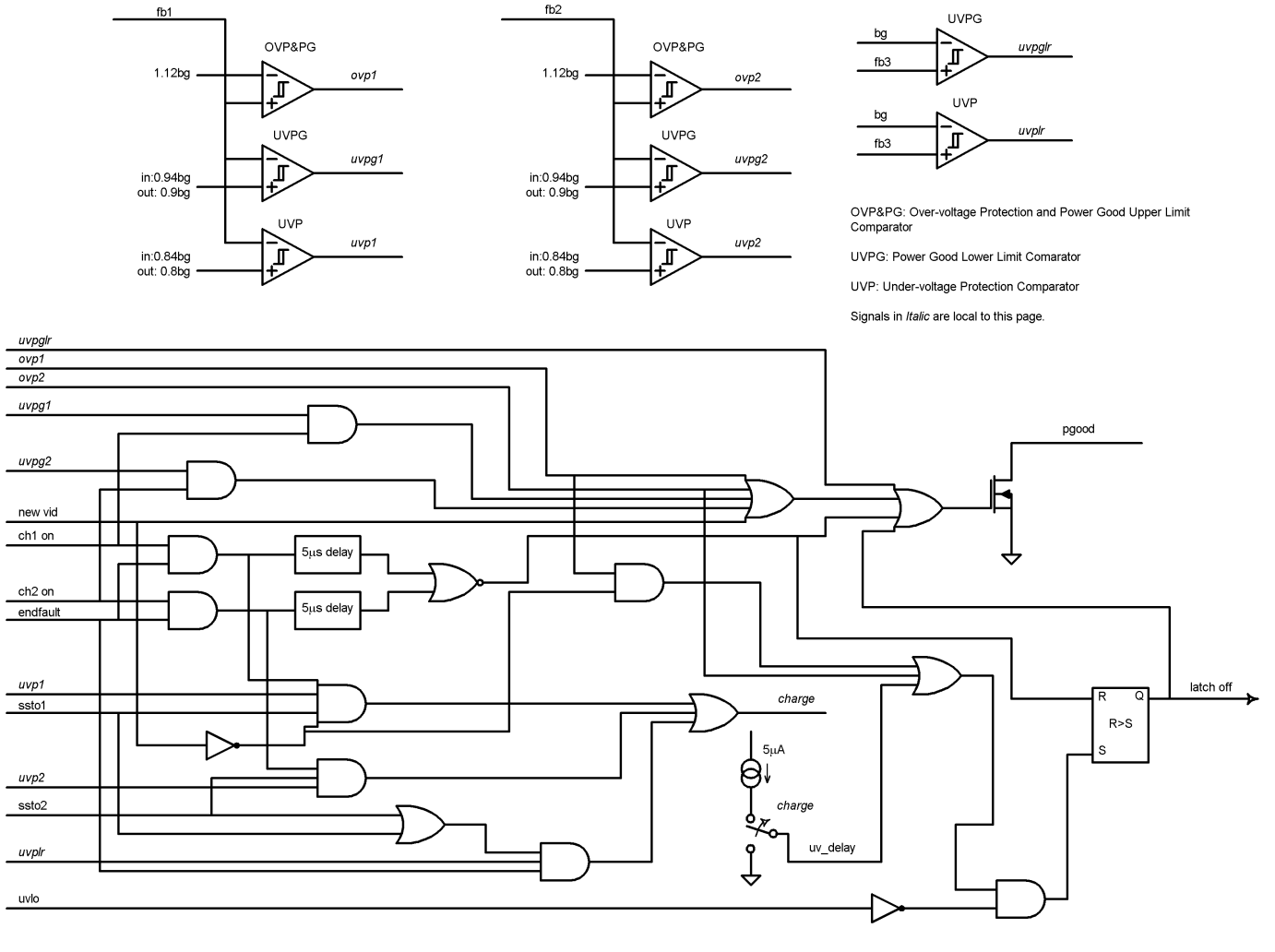

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TABLE 1. Shut Down Latch Truth Table

Input												Output
ovp1	ovp2	uvp1	uvp2	uvplr	new vid	ch1 on	ch2 on	fault	ssto1	ssto2	uv_delay	latch off
1					0	Σ=1		0				1
	1					Σ=1		0				1
		1			0	1		0	1		cap	1
			1				1	0		1	cap	1
				1		Σ = 1		0	Σ = 1		cap	1
All other combinations												0

Note 1: 'Σ=1' means at least one variable is high.

Note 2: 'Fault' is the logic OR of UVLO and thermal shutdown.

Note 3: 'Cap' means the pin has a capacitor of appropriate value between it and ground.

Note 4: Positive logic is used.

Note 5: For meanings of the variables, refer to the block diagrams.

Note 6: A blank value means 'don't care'.

TABLE 2. Power Good Truth Table

Input										Output
ovp1	ovp2	uvpg1	uvpg2	uvpglr	new vid	ch1 on	ch2 on	fault	latch off	PGOOD
1										0
	1									0
		1								0
			1							0
				1						0
					1					0
						π = 0				0
								1		0
									1	0
All other combinations										1

Note 7: "π = 0" means at least one variable is low.

Note 8: Positive logic is used.

Note 9: A blank value means 'don't care'.

Note 10: For meanings of the variables, refer to the block diagrams.

TABLE 3. VID Code and DAC Output

VID4	VID3	VID2	VID1	VID0	DAC Voltage (V)
1	1	1	1	1	No CPU*
1	1	1	1	0	*0.925*
1	1	1	0	1	0.950
1	1	1	0	0	0.975
1	1	0	1	1	1.000
1	1	0	1	0	1.025
1	1	0	0	1	1.050
1	1	0	0	0	1.075
1	0	1	1	1	*1.100*
1	0	1	1	0	1.125
1	0	1	0	1	1.150
1	0	1	0	0	1.175
1	0	0	1	1	1.200
1	0	0	1	0	1.225

TABLE 3. VID Code and DAC Output (Continued)

VID4	VID3	VID2	VID1	VID0	DAC Voltage (V)
1	0	0	0	1	1.250
1	0	0	0	0	1.275
0	1	1	1	1	No CPU
0	1	1	1	0	*1.30*
0	1	1	0	1	*1.35*
0	1	1	0	0	*1.40*
0	1	0	1	1	1.45
0	1	0	1	0	*1.50*
0	1	0	0	1	*1.55*
0	1	0	0	0	*1.60*
0	0	1	1	1	1.65
0	0	1	1	0	1.70
0	0	1	0	1	1.75
0	0	1	0	0	1.80
0	0	0	1	1	1.85
0	0	0	1	0	1.90
0	0	0	0	1	1.95
0	0	0	0	0	*2.00*

*This code is set to 0.900V for convenience.

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltages from the indicated pins to GND/PGND:	
VIN, KS1, KS2, SW1, SW2	−0.3V to 31V
ILIM1, ILIM2	−0.3V to 31V
VID0-VID4	−0.3V to 5V
VLIN, VDD1, VDD2, PGOOD	−0.3V to 6V
FB1, FB2, SENSE2, G3, FB3, OUT3	−0.3V to 6V
CBOOT1	−0.3V to SW1+ 7V
CBOOT2	−0.3V to SW2+ 7V
ON/SS1, ON/SS2	−0.3V to 5V
$\overline{\text{FPWM}}$	−0.3V to 7V
Power Dissipation (T_A = 25˚C), (Note 12)	1.56W
Junction Temperature	+150˚C
ESD Rating (Note 14)	2kV
Ambient Storage Temperature Range	−65˚C to +150˚C
Soldering Dwell Time, Temperature (Note 13)	
Wave	4 sec, 260˚C
Infrared	10sec, 240˚C
Vapor Phase	75sec, 219˚C

Operating Ratings (Note 11)

VIN (VIN and VLIN5 tied together)	4.5V to 5.5V
VIN (VIN and VLIN5 separate)	5.0V to 30V
Junction Temperature 1	0˚C to +125˚C
Junction Temperature 2	−40˚C to +125˚C
VDD1, VDD2	4.5V to 5.5V

Electrical Characteristics

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25˚C. Limits appearing in **boldface** type apply over 0˚C to +125˚C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
ΔV_{out1_load}	Channel 1 Load Regulation (Note 17)	V_{COMP1} moves from 0.5V to 1.5V, VID4:0=01101		0		mV
ΔV_{out2_load}	Channel 2 Load Regulation (Note 17)	V_{COMP2} moves from 0.5V to 1.5V		1.5		mV
ΔV_{fb}	Line Regulation (for the two switching regulators)	5.0V ≤ VIN ≤ 30V, VID4:0=01101		2		mV
I_{vin}	Input Supply Current with the Switching Channels ON	V_{FB} = 0.9V, no VLIN5 DC Current (Note 18)		1.5	**2.4**	mA
I_{vin_sd}	Input Supply Current with the IC Shut Down	$V_{ON/SS1}$ = $V_{ON/SS2}$ = 0V (Note 19)		10	18	µA
V_{vlin5}	VLIN5 Output Voltage	I_{VLIN5} = 0 to 25mA, 5.5V < VIN < 30V	4.7	5.0	5.3	V
V_{cl}	Currentr Limit Comparator Offset			tbd		mV
I_{ilim_pos}	ILIM1 and ILIM2 Pins Sink Current		**8**	10	**12**	µA
V_{ilim_neg}	Negative Current Limit (SWx vs PGNDx voltage)			45		mV
I_{ss_sc}	Soft Start Charge Current		0.5	2.25	4	µA
I_{ss_sk}	Soft Start Sink Current	In UVLO or thermal shutdown		2		µA
V_{ss_on}	Soft Start ON Threshold			1.2		V
V_{ssto}	Soft Start Timeout Threshold	(Note 20)		3.5		V
V_{uvd}	UV_DELAY Threshold	VLIN5 = 5V (Note 21)		2.1		V
I_{delay}	UV_DELAY Source Current		1.0	5	9.0	µA

Electrical Characteristics (Continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25˚C. Limits appearing in **boldface** type apply over 0˚C to +125˚C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
I_{vid}	VID4:0 Internal Pull Up Current			6	13	µA
V_{uvlo_thr}	VIN Under-voltage Lockout (UVLO) Threshold	Rising Edge		4.2	**4.5**	V
V_{uvlo_hys}	VIN UVLO Hysteresis			300		mV
V_{uvp1}	Channel 1 V_{OUT} Under-voltage Shutdown Latch Threshold (Measured at the FB1)	VID4:0 = 01100	**73**	80	**83**	$\%V_{OUT}$
$V_{uvp2, 3}$	Channels 2 and 3 V_{OUT} Undervoltage Shutdown Latch Threshold (Measured at the FB2 and FB3)	VID4:0 = 01100	**76**	80	**86**	$\%V_{OUT}$
V_{ovp1}	V_{OUT} Overvoltage Shutdown Latch Threshold for Channel 1 (Measured at the FB1)		**110**	114	**119**	$\%V_{OUT}$
V_{ovp2}	V_{OUT} Overvoltage Shutdown Latch Threshold for Channel 2 (Measured at the FB2)		**109**	112	**115**	$\%V_{OUT}$
V_{lreg_thr}	V_{OUT} Low Regulation Comparator Enable Threshold for Channels 1 and 2			91.5		$\%V_{OUT}$
V_{lreg_hys}	Hysteresis of Low Regulation Comparator			7		$\%V_{OUT}$
V_{pwrbad}	Regulator Window Detector Thresholds (PGOOD from High to Low)		**85**	88		$\%V_{OUT}$
		(Note 22)	**110**	112	**119**	
V_{pwrgd}	Regulator Window Detector Thresholds (PGOOD from Low to High)		**90**	93	**97**	$\%V_{OUT}$
Gate Drive (For Channel 1 Switching Regulator Controller)						
I_{boot1}	CBOOT Leakage Current	V_{CBOOT1} = 7V		100		nA
	HDRV1 Source Current	V_{HDRV1} = V_{SW1} =0V, V_{CBOOT1} = 5V		1.3		A
	HDRV1 Sink Current	V_{HDRV1} = 5V		tbd		A
	LDRV1 Source Current	V_{LDRV1} = 0V		1.2		A
	LDRV1 Sink Current	V_{LDRV1} = 5V		3		A
	HDRV1 High-Side FET On-Resistance			1.84		Ω
	LDRV1 High-Side FET On-Resistance			tbd		Ω

Electrical Characteristics (Continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25˚C. Limits appearing in **boldface** type apply over 0˚C to +125˚C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
	LDRV1 Low-Side FET On-Resistance			0.5		Ω
Gate Drive (For Channel 2 Switching Regulator Controller)						
I_{boot2}	CBOOT Leakage Current	V_{CBOOT2} = 7V		100		nA
	HDRV2 Source Current	V_{HDRV2} = V_{SW2} =0V, V_{CBOOT2} = 5V		tbd		A
	HDRV2 Sink Current	V_{HDRV2} = 5V		tbd		A
	LDRV2 Source Current	V_{LDRV2} = 0V		tbd		A
	LDRV2 Sink Current	V_{LDRV2} = 5V		tbd		A
	HDRV2 FET On-Resistance			tbd		Ω
	LDRV2 FET On-Resistance			tbd		Ω
Oscillator						
F_{osc}	Oscillator Frequency		**225**	250	**275**	kHz
T_{off_min}	Minimum Off-Time			400		ns
T_{on_min}	Minimum On-Time			220		ns
Error Amplifier						
I_{fb1}	Feedback Input Bias Current, Channel 1	V_{FB1} = 2.4V		55		µA
I_{fb2}	Feedback Input Bias Current, Channel 2	V_{FB2} = 1.36V		18		nA
I_{fb3}	Feedback Input Bias Current, Channel 3	V_{FB3} = 1.36V		70		nA
I_{comp1}, I_{comp2}	COMP Output Sink Current	V_{FB1} = 150% of measured 1.4V DAC, V_{FB2} = 150% of measured bandgap, V_{COMP1} = V_{COMP2} = 1V		60		µA
V_{comp_max}	COMP Pin Maximum Voltage		tbd	1.96		V
Gm	Transconductance			576		µmho
DAC Output and V_{FB2}						
ΔV_{dac}	Channel 1 DAC Output Voltage Accuracy	VCOMP1 = 1V, DAC codes from 1.3V to 1.6V	**−1.5**		**1.5**	%
		VCOMP1 = 1V, DAC codes from 0.925V to 1.25V and from 1.65V to 2.00V	**−1.7**		**1.7**	
V_{fb2}	Channel 2 DC Output Voltage Accuracy	COMP2 pin from 0.5V to 1.8V	**1.217**	1.238	**1.259**	V
Linear Regulator Controller						
V_{fb3}	Channel 3 DC Output Voltage Accuracy		**1.215**	1.24	**1.265**	V
V_{g3_sk}	G3 Sink Current			20		µA
I_{g3_sc}	G3 Minimum Source Current			20		mA
V_{g3_max}	G3 Maximum Voltage			3.6		V
Logic Inputs and Outputs						

Electrical Characteristics (Continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25˚C. Limits appearing in **boldface** type apply over 0˚C to +125˚C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
V_{ih}	Minimum High Level Input Voltage (FPWM, VID0-VID4)		**2.0**			V
V_{il}	Maximum Low Level Input Voltage (FPWM, ON/SS1, ON/SS2, VID0-VID4)				**0.8**	V
I_{oh_pg}	PGOOD Output High Current	PGOOD = 5.7V (Note 23)		5		µA
V_{ol_pg}	PGOOD Output Low Voltage	PGOOD Sinking 20 µA		0.3		V

Electrical Characteristics

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25˚C. Limits appearing in **boldface** type apply over −40˚C to +125˚C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
ΔV_{out1_load}	Channel 1 Load Regulation (Note 17)	V_{COMP1} moves from 0.5V to 1.5V, VID4:0=01101		0		mV
ΔV_{out2_load}	Channel 2 Load Regulation (Note 17)	V_{COMP2} moves from 0.5V to 1.5V		1.5		mV
ΔV_{fb}	Line Regulation (for the two switching regulators)	5.0V ≤ VIN ≤ 30V, VID4:0=01101		2		mV
I_{vin}	Input Supply Current with the Switching Channels ON	V_{FB} = 0.9V, no VLIN5 DC Current (Note 18)		1.5	**2.5**	mA
I_{vin_sd}	Input Supply Current with the IC Shut Down	$V_{ON/SS1}$ = $V_{ON/SS2}$ = 0V (Note 19)		10	18	µA
V_{vlin5}	VLIN5 Output Voltage	I_{VLIN5} = 0 to 25mA, 5.5V < VIN < 30V	4.7	5.0	5.3	V
V_{cl}	Currentr Limit Comparator Offset			tbd		mV
I_{ilim_pos}	ILIM1 and ILIM2 Pins Sink Current		**7**	10	**13**	µA
V_{ilim_neg}	Negative Current Limit (SWx vs PGNDx voltage)			45		mV
I_{ss_sc}	Soft Start Charge Current		0.5	2.25	4	µA
I_{ss_sk}	Soft Start Sink Current	In UVLO or thermal shutdown		2		µA
V_{ss_on}	Soft Start ON Threshold			1.2		V
V_{ssto}	Soft Start Timeout Threshold	(Note 20)		3.5		V
V_{uvd}	UV_DELAY Threshold	VLIN5 = 5V (Note 21)		2.1		V
I_{delay}	UV_DELAY Source Current		1.0	5	9.0	µA
I_{vid}	VID4:0 Internal Pull Up Current			6	13	µA

Electrical Characteristics (Continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25˚C. Limits appearing in **boldface** type apply over −40˚C to +125˚C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
V_{uvlo_thr}	VIN Under-voltage Lockout (UVLO) Threshold	Rising Edge		4.2	**4.6**	V
V_{uvlo_hys}	VIN UVLO Hysteresis			300		mV
V_{uvp1}	Channel 1 V_{OUT} Under-voltage Shutdown Latch Threshold (Measured at the FB1)	VID4:0 = 01100	**72**	80	**84**	$\%V_{OUT}$
$V_{uvp2, 3}$	Channels 2 and 3 V_{OUT} Undervoltage Shutdown Latch Threshold (Measured at the FB2 and FB3)	VID4:0 = 01100	**75**	80	**87**	$\%V_{OUT}$
V_{ovp1}	V_{OUT} Overvoltage Shutdown Latch Threshold for Channel 1 (Measured at the FB1)		**109**	114	**120**	$\%V_{OUT}$
V_{ovp2}	V_{OUT} Overvoltage Shutdown Latch Threshold for Channel 2 (Measured at the FB2)		**108**	112	**116**	$\%V_{OUT}$
V_{lreg_thr}	V_{OUT} Low Regulation Comparator Enable Threshold for Channels 1 and 2			91.5		$\%V_{OUT}$
V_{lreg_hys}	Hysteresis of Low Regulation Comparator			7		$\%V_{OUT}$
V_{pwrbad}	Regulator Window Detector Thresholds (PGOOD from High to Low)		**84**	88		$\%V_{OUT}$
		(Note 22)	**109**	112	**120**	
V_{pwrgd}	Regulator Window Detector Thresholds (PGOOD from Low to High)		**89**	93	**98**	$\%V_{OUT}$
Gate Drive (For Channel 1 Switching Regulator Controller)						
I_{boot1}	CBOOT Leakage Current	V_{CBOOT1} = 7V		100		nA
	HDRV1 Source Current	$V_{HDRV1} = V_{SW1}$ =0V, V_{CBOOT1} = 5V		1.3		A
	HDRV1 Sink Current	V_{HDRV1} = 5V		tbd		A
	LDRV1 Source Current	V_{LDRV1} = 0V		1.2		A
	LDRV1 Sink Current	V_{LDRV1} = 5V		3		A
	HDRV1 High-Side FET On-Resistance			1.84		Ω
	LDRV1 High-Side FET On-Resistance			tbd		Ω
	LDRV1 Low-Side FET On-Resistance			0.5		Ω
Gate Drive (For Channel 2 Switching Regulator Controller)						

Electrical Characteristics (Continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25˚C. Limits appearing in **boldface** type apply over −40˚C to +125˚C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
I_{boot2}	CBOOT Leakage Current	V_{CBOOT2} = 7V		100		nA
	HDRV2 Source Current	V_{HDRV2} = V_{SW2} =0V, V_{CBOOT2} = 5V		tbd		A
	HDRV2 Sink Current	V_{HDRV2} = 5V		tbd		A
	LDRV2 Source Current	V_{LDRV2} = 0V		tbd		A
	LDRV2 Sink Current	V_{LDRV2} = 5V		tbd		A
	HDRV2 FET On-Resistance			tbd		Ω
	LDRV2 FET On-Resistance			tbd		Ω
Oscillator						
F_{osc}	Oscillator Frequency		**225**	250	**275**	kHz
T_{off_min}	Minimum Off-Time			400		ns
T_{on_min}	Minimum On-Time			220		ns
Error Amplifier						
I_{fb1}	Feedback Input Bias Current, Channel 1	V_{FB1} = 2.4V		55		µA
I_{fb2}	Feedback Input Bias Current, Channel 2	V_{FB2} = 1.36V		18		nA
I_{fb3}	Feedback Input Bias Current, Channel 3	V_{FB3} = 1.36V		70		nA
I_{comp1}, I_{comp2}	COMP Output Sink Current	V_{FB1} = 150% of measured 1.4V DAC, V_{FB2} = 150% of measured bandgap, V_{COMP1} = V_{COMP2} = 1V		91		µA
V_{comp_max}	COMP Pin Maximum Voltage		tbd	1.96		V
Gm	Transconductance			576		µmho
DAC Output and V_{FB2}						
ΔV_{dac}	Channel 1 DAC Output Voltage Accuracy	VCOMP1 = 1V, DAC codes from 1.3V to 1.6V	**−2.0**		**2.0**	%
		VCOMP1 = 1V, DAC codes from 0.925V to 1.25V and from 1.65V to 2.00V	**−2.2**		**2.2**	
V_{fb2}	Channel 2 DC Output Voltage Accuracy	COMP2 pin from 0.5V to 1.8V	**1.212**	1.238	**1.264**	V
Linear Regulator Controller						
V_{fb3}	Channel 3 DC Output Voltage Accuracy		**1.209**	1.24	**1.271**	V
V_{g3_sk}	G3 Sink Current			20		µA
I_{g3_sc}	G3 Minimum Source Current			20		mA
V_{g3_max}	G3 Maximum Voltage			3.6		V
Logic Inputs and Outputs						
V_{ih}	Minimum High Level Input Voltage (FPWM, VID0-VID4)		**2.2**			V

Electrical Characteristics (Continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25˚C. Limits appearing in **boldface** type apply over −40˚C to +125˚C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
V_{il}	Maximum Low Level Input Voltage (FPWM, ON/SS1, ON/SS2, VID0-VID4)				**0.7**	V
I_{oh_pg}	PGOOD Output High Current	PGOOD = 5.7V (Note 23)		5		µA
V_{ol_pg}	PGOOD Output Low Voltage	PGOOD Sinking 20 µA		0.3		V

Note 11: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics table.

Note 12: Maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 1.56W rating results from using 150˚C, 25˚C, and 80˚C/W for T_{JMAX}, T_A, and θ_{JA} respectively. A θ_{JA} of 90˚C/W represents the worst-case condition of no heat sinking of the 48-pin TSSOP. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation should be derated by 12.5mW per ˚C above 25˚C ambient. The LM2633 actively limits its junction temperature to about 150˚C.

Note 13: For detailed information on soldering plastic small-outline packages, refer to the Packaging Databook available from National Semiconductor Corporation.

Note 14: Except for ILIM1 and ILIM2 pins, which are 1.5kV. For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.

Note 15: A typical is the center of characterization data taken with $T_A = T_J$ = 25˚C. Typical data are not guaranteed.

Note 16: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with $T_A = T_J$ = 25˚C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 17: This test simulates heavy load condition by changing COMP pin voltage.

Note 18: This parameter indicates how much current the LM2633 is drawing from the input supply when it is functioning but not driving external MOSFETs or a bipoloar transistor.

Note 19: This parameter indicates how much current the LM2633 is drawing from the input supply when it is completely shut off.

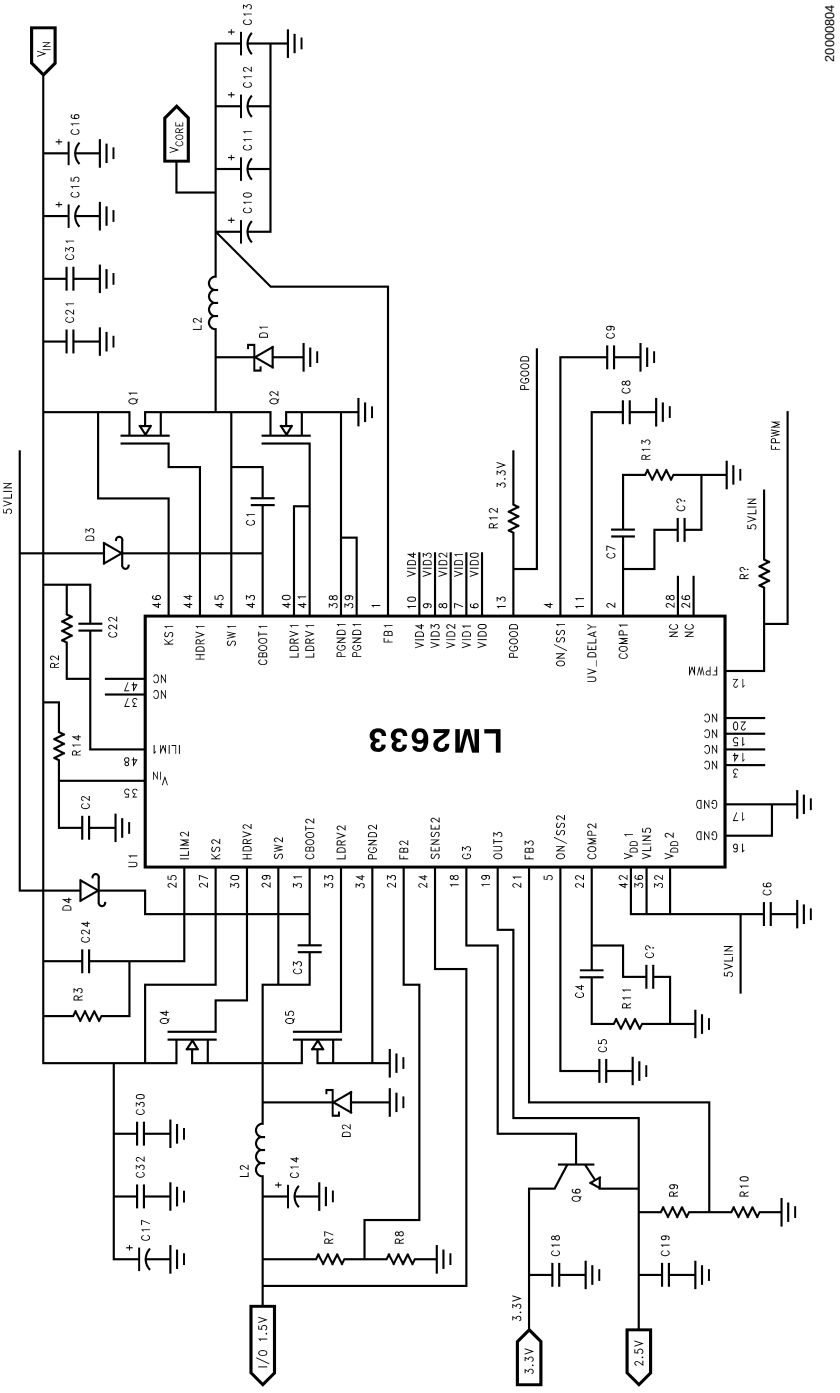
Note 20: When ON/SS1,2 pins are charged above this voltage, the under voltage protection feature is enabled.

Note 21: Above this voltage, the under-voltage protection is enabled.

Note 22: This is the same as over-voltage protection threshold.

Note 23: This is the amount of current PGOOD sinks when PGOOD is high and is forced to the voltage indicated

Typical Application



Operation Descriptions

General

The LM2633 is a combination of three voltage regu-lator controllers. Among them, two are switching regulator controllers and one is a linear regulator controller. The two switching controllers, Channel 1 and Channel 2, operate 180° out of phase. They can be independently enabled and disabled. The linear controller, or Channel 3, cannot be disabled but can be left unused. Channel 1 output voltage is set by an internal DAC, which accepts a 5-bit VID code from pins 6 through 10. Channels 2 and 3 output voltages are adjusted with a voltage divider. Both switching channels are synchronous and em-ploy peak current mode control scheme. Protection features include over-voltage protection (Ch1 and 2), under-voltage protection (all channels), and positive and negative peak current limit (Ch1 and 2). UVP function can be delayed by an arbitrary amount of time. Input voltage to the switching regulators can range from 4.5V to 30V. The linear regulator typically takes a 3.3V input voltage and its output volt-age can go up to 3.8V. The power good function always monitors all three output voltages.

Soft Start

If the ON/SSx pin is connected to ground instead of to a capacitor, the corresponding channel is turned off and will not start up.

Assume the ON/SSx pin is connected to a capacitor and the rest of the circuit is set up correctly. When the input voltage rises above the 4.2V threshold, the internal circuitry is powered on, the ON/SSx pin should be held at 1.1V, and a 2µA current starts to charge the capacitor connected between the ON/SSx pin and ground. When the ON/SSx pin voltage exceeds 1.2V, the corresponding channel is turned on. A MIN_ON_TIME comparator generates the soft start PWM pulses. As the ON/SSx pin voltage ramps up, the duty cycle grows, causing the output voltage to ramp up. During this time, the error amplifier output voltage is clamped at 0.8V, and the duty cycle generated by the PWM comparator is ignored. When the corresponding output voltage exceeds 99% of the set target voltage, the mode of the channel transitions from soft start to operating. As a result, the high clamp at the output of the error amplifier is switched to 2V. Beyond this point, once the PWM pulses generated by the PWM comparator are wider than that generated by the MIN_ON_TIME comparator, the PWM comparator takes over and starts to regulate the output voltage. That is, peak current mode control now takes place.

The speed at which the duty cycle grows depends on the capacitance of the soft start capacitor. The higher the capacitance, the slower the speed. However, that speed is independent of how fast the input voltage grows. That is because the ramp signal used to generate the soft start duty cycle has a peak value proportional to input voltage, making the product of duty cycle and input voltage a value that is independent of input voltage. This feature makes the soft start process more predictable and reliable because whether the input power supply goes through a soft start process or is applied abruptly does not affect the LM2633 soft start.

During soft start, under-voltage protection is disabled. But over-voltage protection and current limit are in place.

When the ON/SSx pin voltage exceeds 3.5V, a soft start time out signal (sstox) will be issued. This signal enables the under-voltage protection. See the Under-Voltage Protection section.

Shutdown Mode

If both ON/SSx pins are pulled low, the IC will be in shut down mode. Both top gate-drives of the two switching channels are turned off while both bottom gate-drives remain on. The linear channel is also disabled.

The same thing happens to the gate drives when the input voltage is below the UVLO threshold.

Turning Off a Switching Channel

A switching channel can be turned off by pulling its ON/SSx pin below about 1.1V. Upon detecting a low level on ON/SSx pin, the corresponding top gate-drive will be turned off and the bottom gate-drive will be turned on. In a high current application, it may be necessary to take special measures to make sure that the output voltage does not go too negative during shutdown. One of those measures is to add a Schottky diode in parallel with output capacitors. Another measure is to fine tune the power stage parameters such as inductance and capacitance values.

Fault State

Whenever the input voltage becomes too low (less than 3.9V), or the IC is too hot and enters thermal shut down mode, a 'fault' signal will be generated internally. This signal will discharge the capacitor connected between the ON/SSx pin and ground with 3mA of current until the pin reaches 1.1V. The switching channels will be turned off upon seeing this signal.

In the fault state, OVP and UVP are disabled

Force-PWM Mode

This mode applies to both switching channels si-multaneously. The force-PWM mode is activated by pulling the FPWM pin to logic low. In this mode, the top FET and the bottom FET gate signals are always complementary to each other. The 0-CROSSING / NEGATIVE CURRENT LIMIT comparator detects the negative current limit. In force-PWM mode, the regulator always operates in Continuous Conduction Mode (CCM) and its duty cycle (approximately V_{OUT} / V_{IN} is almost independent of load.

The force-PWM mode is good for applications where fixed switching frequency is required.

In force-PWM mode, the top FET has to be turned on for a minimum of 220ns each cycle. However, when the required duty cycle is less than the minimum value, the skip comparator will be activated and pulses will be skipped to maintain regulation.

Skip Comparator

Whenever the COMPx pin voltage goes below the 0.5V threshold, the PWM cycles will be 'skipped' until that voltage again exceeds the threshold.

Pulse-Skip Mode

This mode is activated by pulling the FPWM pin to a TTL-compatible logic high and applies to both switching channels simultaneously. In this mode, the 0-CROSSING / NEGATIVE CURRENT LIMIT comparator detects the bottom FET current. Once the bottom FET current flows from source to drain, the bottom FET will be turned off. This prevents negative inductor current. In force-PWM operation, the inductor current is allowed to go negative, so the regulator is always in Continuous Conduction Mode (CCM), no matter what the load is. In CCM, duty cycle is almost independent of the load, and is roughly Vout divided by V_{IN}. In pulse-skip

Operation Descriptions (Continued)

mode, the regulator enters Discontinuous Conduction Mode (DCM) under light load. Once the regulator enters DCM, its duty cycle droops as the load current decreases. The regulator operates in DCM PWM mode until its duty cycle falls below 85% of the CCM duty cycle, when the MIN_ON_TIME comparator takes over. It forces 85% CCM duty cycle which causes the output voltage to continuously rise and COMPx pin voltage (error amplifier output voltage) to continuously droop. When the COMPx pin voltage hits the 0.5V level, the CYCLE_SKIP comparator toggles, causing the present switching cycle to be 'skipped', i.e., both FETs remain off during the whole cycle. As long as the COMPx pin voltage is below 0.5V, no switching of the FETs will happen. As a result, the output voltage will droop, and the COMPx pin voltage will rise. When the COMPx pin goes above the 0.5V level, the CYCLE_SKIP comparator flips and allows a 85% CCM duty cycle pulse to happen. If the load current is so small that this single pulse is enough to bring output voltage up to such a level that the COMPx pin drops below 0.5V again, the pulse skipping will happen again. Otherwise it may take a number of consecutive pulses to bring the COMPx pin voltage down to 0.5V again. As the load current increases, it takes more and more consecutive pulses to discharge the COMPx voltage to 0.5V. When the load current is so high that the duty cycle exceeds the 85% CCM duty cycle, then pulse-skipping disappears. In pulse-skip mode, the frequency of the switching pulses decreases as the load current decreases.

The LM2633 needs to sense the output voltages directly in the pulse-skip mode operation. For Channel 1 this is realized through the FB1 pin. For Channel 2, it is realized by connecting SENSE2 pin to the output.

The LM2633 pulse-skip mode helps the light load efficiency for two reasons. First, it does not turn on the bottom FET, this eliminates circulating energy and reduces gate drive power loss. Second, the top FET is only turned on when necessary, rather than every cycle, also reduces gate drive power loss.

Current Sensing and Current Limiting

Sensing of the inductor current for feedback control is accomplished through sensing the drain-source voltage of the top FET when it is turned on. There is a leading edge blanking circuitry that forces the top FET to be on for at least 160ns. Beyond this mini-mum on time, the output of the PWM comparator is used to turn off the top FET. The blanking circuitry is being used to blank out the noise associated with the turning on of the top FET.

Current limit is implemented using the same V_{ds} information. See *Figure 1*.

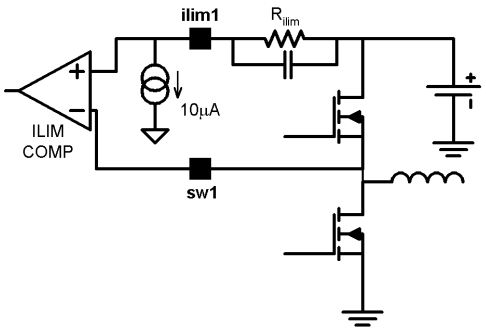


FIGURE 1. Current Limit Method

There is a 10mA current sink on the ILIMx pin. When an external resistor is connected between ILIMx pin and top FET drain, a DC voltage is established be-tween the two nodes. When the top FET is turned on, the voltage across the FET is proportional to the inductor current. If the inductor current is too high, SWx pin voltage will be lower than the ILIMx voltage, causing the comparator to toggle and thus the top FET will be turned off immediately. The comparator is disabled when the top FET is turned off and dur-ing the leading edge blanking time.

Negative Current Limit

The negative current limit is put in place to ensure that the inductor will not saturate during a negative current flow and cause excessive current to flow through the bottom FET. The negative current limit is realized through sensing the bottom FET V_{ds}. An internal reference voltage is used to compare with the bottom FET Vds when it is on. Upon seeing too high a Vds, the bottom FET will be turned off. The negative current limit is activated in force PWM mode, or also in the case of Channel 1, whenever there is a dynamic VID change.

Active Frequency Control

As the input / output voltage differential increases, the on time of the top FET as regulated by the feed-back control circuitry may approach the minimum value, i.e. the blanking time. That will cause unst-ble operations such as pulse skipping and uneven duty cycles. To avoid such an issue, the LM2633 is designed in such a way that when input voltage rises above about 17V, the PWM frequency starts to droop. The on time of the top FET will remain roughly the same as input voltage increases and frequency droops, so that the duty cycle gets lower and lower.

The main impact of this shift in PWM frequency is the inductor ripple current and output voltage ripple. Regulator design should take this into account.

Operation Descriptions (Continued)

Shutdown Latch State

This state is typically caused by an output under voltage or over voltage event. In this state, both switching channels have their top FETs turned off, and their bottom FETs turned on. The linear channel is not affected unless the error event is caused by it.

There are two methods to release the system from the latch state. One is to create a fault state (see the corresponding section) by either bringing down the input voltage to below 3.9V UVLO threshold and then bringing it back to above 4.2V, or somehow by causing the system to enter thermal shut down. Another method is to pull both ON/SSx pins below 1V and then release them.

After the latch is released, the two switching chan-nels will go through the normal soft start process. The linear channel output voltage will not be affected unless the UVLO method is used to release the latch or unless the error event is caused by the linear channel.

Over-voltage Protection

This protection feature is implemented in the two switching channels and not the linear channel. Refer to *Table 1*. As long as there is at least one switching channel enabled, and the LM2633 is not in fault state, any over voltage event at any of the two switching channels' output will cause system to enter the shut down latch state.

However, if the over voltage event happens only on Channel 1 after a dynamic VID change signal is issued and before the change completes, the system will not enter the shut down latch state. See the Dynamic VID Change section.

Under-voltage Protection

The UVP feature is implemented in all three channels.

If the UV_DELAY pin is pulled to ground, then the under-voltage protection feature is disabled. Otherwise, if a capacitor is connected between the UV_DELAY pin and ground, the UVP is enabled. Assume UVP is enabled and the system is not in fault state. If a switching channel is enabled, and its soft start time out signal (sstox, see soft start section) is asserted, then an under voltage event at the output of that channel will cause the system to enter the shut down latch state.

However, if the under voltage event happens only on Channel 1 after a dynamic VID change signal is issued and before the change completes, the system will not enter the shut down latch state. See the Dynamic VID Change section.

For the linear channel, if there is at least one switching channel on, and at least one soft start time out signal has been issued, and if the system is not in fault state, then an under voltage event at the linear regulator output will cause the system to enter shut down latch state.

When the system reacts on an under voltage event, a 5mA current will be charging the capacitor con-nected to the UV_DELAY pin and when its voltage exceeds 2.1V, the system immediately enters shut down latch state.

For details, see the block diagram and Shut Down Latch Truth Table.

Power Good Function

The power good function is a general indication of the health of the regulators. The function is realized through an internal MOSFET tied from the PGOOD pin to ground. Power good signal is asserted by turning off that MOSFET.

The internal power good MOSFET will not be turned on unless at least one of the following occurs:

1. There is an output over voltage event in at least one of the switching channels.
2. The output voltage of any of the three channels is below the power good lower limit, regardless of ON/SSx pin voltage level.
3. Whenever Channel 1 is going through a dynamic VID change.
4. System is in the shut down mode.
5. System is in the fault state.
6. System is in the shut down latch state.

Power good higher limit is the same as that of the OVP function.

In cases 2 and 3 above, if the corresponding output voltage(s) recovers, PGOOD will be asserted again. But there is a built-in hysteresis. See V_{pwrgd} in the Electrical Characteristics table. The above information is also available in Power Good Truth Table.

When the internal power good MOSFET is turned on, the PGOOD pin will be pulled to ground. When it is turned off, the PGOOD pin is floating (open-drain). The on resistance of the power good MOSFET is about 15kΩ.

Dynamic VID Change

During normal operation, if Channel 1 sees a change in the VID pattern, a NEW VID signal will be issued. Upon seeing the NEW VID signal, power good will be deasserted, UVP and OVP of Channel 1 will be disabled temporarily, and Channel 1 goes through a special step to quickly ramp the output voltage to the new value.

If the new output voltage is higher than the old voltage, Channel 1 will rely on the control loop to change the output voltage. If the new value is lower than the old one, the top FET is going to remain off while the bottom FET is going to remain on. This will cause the output capacitor to discharge through the inductor. The 0-CROSSING / NEGATIVE CURRENT LIMIT comparator will detect for negative over current, even if the LM2633 is in pulse-skip mode. When the negative current limit is reached, bottom FET will be turned off, forcing the inductor current to flow through the body diode of the top FET to the input supply. When next clock cycle comes, the bottom FET will be turned on again, and it will not be turned off until the negative current limit is reached again. During this process, if the output voltage goes below the new voltage, the NEW VID signal will be deasserted. At this time, power good function will be released, OVP and UVP will be enabled and the bottom FET will be turned off. The normal control loop takes over after the output voltage droops below the new DAC voltage.

Internal 5V Supply

The internal 5V supply is generated from the VIN voltage through an internal linear regulator. This 5V supply is mainly for internal circuitry use, but can also be used externally (through the VLIN5 pin) for convenience. A typical use of this 5V is supplying the bootstrap circuitry for top drivers and supplying the voltage needed by the bottom drivers (through the VDDx pins). But since this 5V is generated by a linear

Operation Descriptions (Continued)

regulator, it may hurt the light load efficiency, especially when VIN voltage is high. So if there is a separate 5V available that is generated by a switching power supply, it may be a good idea to use that 5V to power the bootstrap circuitry and the VDDx pins for better efficiency and less thermal stress on the LM2633.

In shut down mode, the VLIN5 pin will go to 5.5V. So it is recommended not to use this voltage for purposes other than the bootstrap circuitry and VDDx pins.

When the power stage input voltage can be guaranteed to be within 4.5V to 5.5V, the VLIN5 pin can be tied to the VIN pin directly. In this mode, all 5V currents are directly coming from power stage input rail VIN and power loss due to the internal linear regulation is no longer an issue.

Design Procedures

CPU Core / GTL Bus Power Supply

Nomenclature

ESR - Equivalent Series Resistance.

Loading transient - a load transient when the load current goes from minimum load to full load.

Unloading transient - a load transient when the load current goes from full load to minimum load.

C_{min} - minimum allowed output capacitance.

C_{max} - maximum allowed output capacitance.

D - duty cycle.

f - switching frequency.

I_{nlim} - negative current limit level.

I_{ilim} - positive current limit (ILIM1)pin current.

I_{irrm} - maximum input current ripple RMS value.

I_{load} - load current.

I_{rip} - output inductor peak-to-peak ripple current.

$\pm\delta\%$ - CPU core voltage regulation window.

$\pm\epsilon\%$ - LM2633 initial DAC tolerance.

ΔV_{c_s} - maximum allowed CPU core voltage excursion during a load transient, as derived from CPU specifications.

ΔI_{c_s} - maximum load current change, as specified by the CPU manufacturer.

R_e - total combined ESR of output capacitors.

R_{e_s} - maximum allowed total combined ESR of the output capacitors, as derived from CPU load transient specifications.

R_{ilim} - current limit adjustment resistance. See current sensing and current limiting.

t_{max} - maximum allowed dynamic VID transition time.

t_{peak} - time for the CPU core voltage to reach its peak value during an unloading transient.

V_{in} - input voltage to the switching regulators.

V_n - nominal output voltage.

V_{old} - nominal CPU core voltage before dynamic VID change.

V_{new} - nominal CPU core voltage after dynamic VID change.

V_{rip} - peak-to-peak output ripple voltage.

L - inductance of the output inductor.

General

Designing a power supply involves many tradeoffs. A good design is usually a design that makes good tradeoffs. Today's synchronous buck regulators typically run at a 200kHz to 300kHz switching frequency. Beyond this range, switching loss becomes excessive, and below this range, inductor size becomes unnecessarily large. The LM2633 has a fixed operating frequency of 250kHz when VIN voltage is below about 17V, and has decreased frequency when VIN voltage exceeds 17V. See Active Frequency Control section.

In a mobile CPU application, both the CPU core and the GTL bus exhibit large and fast load current swings. The load current slew rate during such a transient is usually well beyond the response speed of the regulator.To meet the regulation specification, special considerations should be given to the component selection. For example, the total combined ESR of the output capacitors must be lower than a certain value. Also because of the tight regulation specification, only a small budget can be assigned to ripple voltage, typically less than 20mV. It is found that starting from a given output voltage ripple will often result in fewer design iterations.

The design procedures that follow are generally appropriate for both the CPU core and the GTL bus power supplies, although emphasis is placed on the former. When there is a difference between the two, it will be pointed out.

Output Capacitor Selection

Type of output capacitors

Different type of capacitors often have different combinations of capacitance and ESR. High-capacitance multi-layer ceramic capacitors (MLCs) have very low ESR, typically 12mΩ, but also relatively low capacitance - up to 100µF. Tantalum capacitors can have fairly low ESR, such as 18mΩ, and pretty high capacitance - up to 1mF. Aluminum capacitors can have very high capacitance and fairly low ESR. OSCON capacitors can achieve ESR values that are even lower than those of MLCs' and with higher capacitance.

Tutorial on load transient response

Skip to the next subsection when a quick design is desired. The control loop of the LM2633 can be made fast enough so that when a worst-case load transient happens, duty cycle will saturate (meaning it jumps to either 0% or D_{max}). If the control loop is fast enough, the worst situation for a load transient will be that the transient happens when the following three are also happening. One, present PWM pulse has just finished. Two, input voltage is the highest. Three, the load current goes from maximum down to minimum (referred to as an unloading transient). *Figure 2* shows how inductor current changes during a worst-case load transient. The reasons are as follows. In a mobile CPU application, the input/output voltage differential, which is applied across the inductor during a loading transient, is higher than the output voltage, which is applied across the inductor during an unloading transient.

Output Capacitor Selection

(Continued)

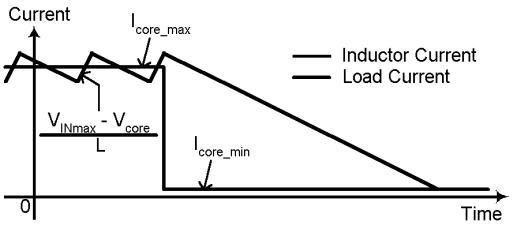


FIGURE 2. Worst-case Load Transient

That means the inductor current changes slower during an unloading transient than during a loading transient. The slower the inductor current changes during a load transient, the higher output capacitance is needed. That is why an unloading transient is the worst case. If the load transient happens when the present PWM pulse has just finished, the inductor current will be the highest, which means highest initial charging current for the output capacitors. Finally, the higher the input voltage, the higher the inductor ripple current and the higher the initial charging current for the output capacitors.

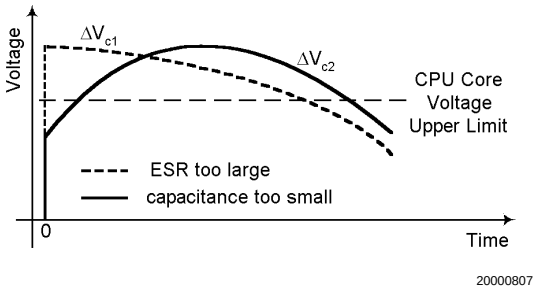


FIGURE 3. Load Transient Spec. Violation

Because the response speed of the regulator is slow compared to a typical CPU load transient, the regulator has to rely heavily on the output capacitors to handle the load transient. The initial overshoot or undershoot is caused by the ESR of the output capacitors. How the output voltage recovers after that initial excursion depends on how fast the output in-ductor current ramps and how large the output capacitance is. See *Figure 3*. If the total combined ESR of the output capacitors is not low enough, the initial output voltage excursion will violate the specification, see ΔV_{c1}. If the ESR is low enough, but there is not enough output capacitance, output voltage will have too much an extra excursion and travel outside the specification window, before it returns to its nominal value, see ΔV_{c2}.

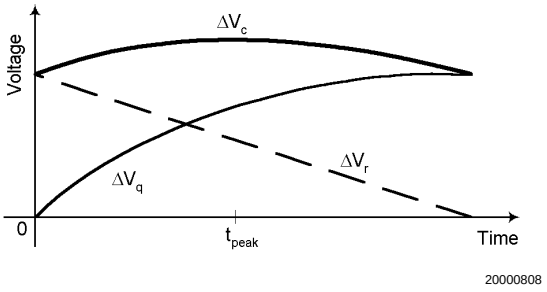


FIGURE 4. Delta Output Voltage Components

During a load transient, the delta output voltage ΔV_c has two changing components. One is the delta voltage across the ESR (ΔV_r), the other is the delta voltage caused by the gained charge (ΔV_q). Both delta voltages change with time. For ΔV_r, the equation is:

$$\Delta V_r = \left(\Delta I_{c\_s} - \frac{V_N}{L} .t\right) .R_e \quad (1)$$

and for ΔV_q, the equation is:

$$\Delta V_q = -\frac{V_N}{2LC} .t^2 + \frac{\Delta I_{c\_s}}{C} .t \quad (2)$$

The total change in output voltage during such a load transient is:

$$\Delta V_c = \Delta V_r + \Delta V_q \quad (3)$$

From *Figure 4* it can be told that ΔV_c will reach its peak value at some point in time and then it is going to decrease. The larger the output capacitance is, the earlier the peak will happen. If the capacitance is large enough, the peak will occur at the beginning of the transient. In other words, ΔV_c will decrease monotonically after the transient happens. To find the peak position, let the derivative of ΔV_c go to zero, and the result is:

$$t_{peak} = \frac{\Delta I_{c\_s}.L}{V_N} - C.R_e \quad (4)$$

The target is to find the capacitance value that will yield, at t_{peak}, a ΔV_c that equals ΔV_{c_s}. By plugging t_{peak} expression into the ΔV_C expression and equating the latter to ΔV_{c_s}, the following formula is obtained:

$$C_{min} = \frac{L.\left[\Delta V_{c\_s} - \sqrt{(\Delta V_{c\_s})^2 - (\Delta I_{c\_s}.R_e)^2}\right]}{V_n . R_e^2} \quad (5)$$

Notice it is already assumed the total ESR is no greater than R_{e_s} otherwise the term under the square root will be a negative value.

Output Capacitor Selection

(Continued)

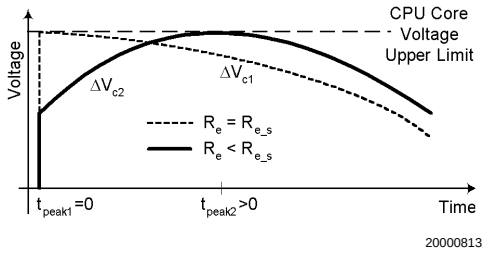


FIGURE 5. $R_e = R_{e\_s}$ vs $R_e < R_{e\_s}$

There are two scenarios when calculating the C_{min}. See *Figure 5*. One is that R_e is equal to R_{e_s} so there is absolutely no room for ΔV_q, which means t_{peak} = 0s. The other is that R_e is smaller than R_{e_s} so there is some room for ΔV_q, which means tpeak is greater than zero. However, it is not necessary to differentiate between the two scenarios when figuring out the C_{min} by above formula.

Allowed transient voltage excursion

The allowed output voltage excursion during a load transient is:

$$\Delta V_{c\_s} = (\delta\% - \varepsilon\%).V_n - \frac{1}{2}V_{rip} \quad (6)$$

Example: V_n = 1.35V, δ% = 7.5%, ϵ = 1.4%, V_{rip} = 20mV

$$\Delta V_{c\_s} = (7.5\% - 1.4\%) \times 1.35 - \frac{20mV}{2} = 72mV$$

Since the ripple voltage is included in the calculation of ΔV_{c_s}, the inductor ripple current should not be included in the worst-case load current excursion. That is, the worst-case load current excursion should be simply ΔI_{c_s}.

Maximum ESR calculation

No matter how much capacitance there is, if the total combined ESR is not less than a certain value, the load transient requirement will not be met.

The maximum allowed total combined ESR is:

$$R_{e\_s} = \frac{\Delta V_{c\_s}}{\Delta I_{c\_s}} \quad (7)$$

Example: ΔV_{c_s} = 72mV, ΔI_{c_s} = 10A. Then R_{e_s} = 7.2mΩ.

Maximum ESR criterion can be used when the capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used.

Minimum capacitance calculation

In a CPU core or a GTL bus power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the input voltage is the highest and when the present switching cycle has just finished. The corresponding minimum capacitance is calculated as follows:

$$C_{min} = \frac{L \times \left[\Delta V_{c\_s} - \sqrt{(DV_{c\_s})^2 - (\Delta I_{c\_s} \times R_e)^2}\right]}{V_n \times R_e^2} = 1.33mF \quad (8)$$

Notice it is already assumed the total ESR is no greater than R_{e_s}, otherwise the term under the square root will be a negative value.

Example: R_e = 6mΩ, V_n = 1.35V, ΔV_{c_s} = 72mV, ΔI_{c_s} = 10A, L = 2µH

$$C_{min} = \frac{2\mu H\left[72mV - \sqrt{(72mV)^2 - (10A \times 6m\Omega)^2}\right]}{1.35 \times (6m\Omega)^2} = 1.33mF$$

Generally speaking, C_{min} decreases with decreasing R_e, ΔI_{c_s}, and L, but with increasing V_n and ΔV_{c_s}.

Maximum capacitance calculation

This subsection applies to Channel 1 / CPU core power supply only.

If there is a need to change the CPU core voltage dynamically (see Dynamic VID Change), there will be a maximum output capacitance restriction. If the output capacitance is too large, it will take too much time for the CPU core voltage to ramp to the new value, violating the maximum transition time specification. The worst-case dynamic VID change is one that takes the largest step down at no load. The maximum capacitance as determined by the way LM2633 implements the VID change can be calculated as follows:

$$C_{max} = \frac{t_{max}.(I_{nlim} + 2.I_{load})}{2.(V_{old} - V_{new})} \quad (9)$$

Example: t_{max} = 100µs, I_{nlim} = 20A, V_{old} = 1.6V, V_{new} = 1.35V, I_{load} = 0.

$$C_{max} = \frac{100\ \mu s \times 20A}{2 \times (1.6V - 1.35V)} = 4\ mF$$

Generally speaking, C_{max} decreases with decreasing t_{max}, I_{nlim} and I_{load}, but with increasing voltage step.

Output Inductor Selection

The size of the output inductor can be determined from the assigned output ripple voltage budget and the impedance of the output capacitors at switching frequency. The equation to determine the minimum inductance value is as follows:

$$L_{min} = \frac{V_{in\_max} - V_n}{\min(V_{in\_max}, 17V)} \cdot \frac{V_n.R_e}{f.V_{rip}} \quad (10)$$

where $\min(V_{in\_max}, 17V)$ means the smaller of V_{in_max} and 17V. The reason this term is not simply V_{in_max} is that the switching frequency droops with increasing V_{in} when V_{in} is higher than 17V. See Active Frequency Control.

In the above equation, R_e is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to R_e. In the case of ceramic capacitors, replace R_e with the true impedance.

Output Inductor Selection (Continued)

Example 1: V_{in_max} = 21V, V_n = 1.6V, V_{rip} = 26mV, R_e = 6mΩ, f = 250kHz.

$$L_{min} = \frac{21V - 1.6V}{17V} \cdot \frac{1.6V \times 6m\Omega}{250kHz \times 26mV} = 1.7\mu H$$

Example 2: V_{in_max} = 18V, V_n = 1.35V, V_{rip} = 20mV, R_e = 6mΩ, f = 250kHz.

$$L_{min} = \frac{18V - 1.35V}{17V} \cdot \frac{1.35V \times 6m\Omega}{250kHz \times 20mV} = 1.6\mu H$$

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest CPU core voltages and their load transient requirements should be considered. If an inductance value larger than L_{min} is selected, make sure the Cmin requirement is not violated. Priority should be given to parameters that are not flexible or more costly. For example, if there are very few types of capacitors to choose from, it may be a good idea to adjust the inductance value so that a requirement of 3.2 capacitors can be reduced to 3 capacitors.

Inductor ripple current is often the criterion for selecting an output inductor. However, in the CPU core or GTL bus application, it is usually of less priority. That is partly because the stringent output ripple voltage requirement automatically limits the inductor ripple current level. It is nevertheless a good idea to double check the ripple current. The equation is:

$$I_{rip\_max} = \frac{V_{in\text{-}max} - V_n}{f.L} \cdot \frac{V_n}{\min(V_{in\_max}, 17V)} \quad (11)$$

where min(V_{in_max}, 17V) means the smaller of V_{in_max} and 17V.

What is more important is the ripple content, which is defined by I_{rip_max} / I_{load_max}. Generally speaking, a ripple content of less than 50% is ok. Too high a ripple content will cause too much loss in the inductor.

Example: V_{in_max} = 21V, V_n = 1.6V, f = 250kHz, L = 1.7µH.

$$I_{rip\_max} = \frac{21V - 1.6V}{250kHz \times 1.7\mu H} \cdot \frac{1.6V}{17V} = 4.3A$$

If the maximum load current is 14A, then the ripple content is 4.3A / 14A = 30%.

When choosing the inductor, the saturation current should be higher than the maximum peak inductor current. The RMS current rating should be higher than the maximum load current.

MOSFET Selection

Bottom FET Selection

During normal operations, the bottom FET is turned on and off at almost zero voltage. So only conduction loss is present in the bottom FET. The bottom FET power loss peaks at the maximum input voltage and load current. The most important parameter when choosing the bottom FET is the on resistance. The less the on resistance, the less the power loss. The equation for the maximum allowed on resistance at room temperature for a given FET package, is:

$$Rds\_max = \frac{1}{I^2_{load\_max} \cdot \left(1 - \frac{V_n}{V_{in\_max}}\right)} \times \frac{T_{j\_max} - T_{a\_max}}{\left[1 + TC.(T_{j\_max} - 25°C/W)\right]} . R_{\theta ja} \quad (12)$$

where T_{j_max} is the maximum allowed junction temperature in the FET, T_{a_max} is the maximum ambient temperature, $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET, and TC is the temperature coefficient of the on resistance which is typically 4000ppm/˚C.

If the calculated on resistance is smaller than the lowest value available, multiple FETs can be used in parallel. If the design criterion is to use the highest R_{ds} FET, then the R_{ds_max} of a single FET can be increased due to reduced current. In the case of two FETs in parallel, multiply the calculated on resis-tance by 4 to obtain the on resistance for each FET. In the case of three FETs, that number is 9. Since efficiency is very important in a mobile PC, having the lowest on resistance is usually more important than fully utilizing the thermal capacity of the package. So it is probably better to find the lowest R_{ds} FET first, and then determine how many are needed.

Example: T_{j_max} = 100˚C, T_{a_max} = 60˚C, $R_{\theta ja}$ = 60˚C/W, V_{in_max} = 21V, V_n = 1.6V, and I_{load_max} = 10A.

$$Rds\_max = \frac{1}{(10A)^2 \cdot \left(1 - \frac{1.6V}{21V}\right)} \times \frac{100^oC - 60^oC}{\left[1 + 0.004/^oC \cdot (100^oC - 25^oC)\right] \cdot 60^oC/W} = 5.6m\Omega$$

If the lowest on resistance FET has a R_{ds_max} of 10mΩ, then two can be used in parallel. The temperature rise on each FET will not go to T_{j_max} because each FET is now dissipating only half of the total power.

Alternatively, two 22mΩ FETs can be used in parallel, with each FET reaching T_{j_max}. This may lower the FET cost, but will double the power loss.

Top FET Selection

The top FET has two types of losses - the switching loss and the conduction loss. The switching loss mainly consists of the cross-over loss and the bottom diode reverse recovery loss. It is rather difficult to estimate the switching loss. A general starting point is to allot 60% of the top FET thermal capacity to switching loss. The best way to find out is still to test it on bench. The equation for calculating the on resistance of the top FET is thus:

$$Rds\_max = \frac{V_{in\_min}}{2.5 \times I^2_{load\_max} \cdot V_n} \times \frac{T_{j\_max} - T_{a\_max}}{\left[1 + TC \cdot (T_{j\_max} - 25°C/W)\right] \cdot R_{\theta ja}} \quad (13)$$

MOSFET Selection (Continued)

where T_{j_max} is the maximum allowed junction temperature in the FET, T_{a_max} is the maximum ambient temperature, $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET, and TC is the temperature coefficient of the on resistance which is typically 4000ppm/˚C.

Example: T_{j_max} = 100˚C, T_{a_max} = 60˚, $R_{\theta ja}$ = 60˚C/W, V_{in_min} = 14V, V_n = 1.6V, and I_{load_max} = 10A.

$$R_{ds\_max} = \frac{14V}{2.5 \times (10A)^2 \times 1.6V} \times \frac{100^oC - 60^oC}{[1+0.004/^oC \cdot (100^oC - 25^oC)] \cdot 60^oC/W} = 18m\Omega$$

Since the switching loss usually increases with bigger FETs, choosing a top FET with a much smaller on resistance sometimes may not yield noticeable lower temperature rise and better efficiency.

Current Limit Setting

What is actually monitored and limited is the peak drain-source voltage of the top FET. The equation for current limit resistor is as follows:

$$R_{ilim} = \frac{I_{load\_lim} + \frac{1}{2} \times I_{rip\_max}}{I_{ilim\_min}} \times R_{ds\_max} \times [1+TC.(T_{j\_max} - 25^oC)] \quad (14)$$

where I_{load_lim} is the desired load current limit level and I_{ilim_min} is the minimum current sink level at the ILIM1 pin. This calculated R_{ilim} value guarantees that the minimum current limit will not be less than I_{load_lim}.

Example: I_{load_lim} = 16A, I_{rip_max} = 4.3A, R_{ds_max} = 18mΩ, T_{j_max} = 100˚C, I_{ilim_min} = 8µA

$$R_{ds\_max} = \frac{16A + \frac{1}{2} \times 4.3A}{8\mu A} \times 18\mu\Omega \times [1+0.004/^oC \cdot (100^oC - 25^oC)] = 53k\Omega \approx 53.6k\Omega$$

It is recommended that a 1% tolerant resistor be used and its resistance should not be lower than the calculated value.

Input Capacitor Selection

The fact that the two switching channels of the LM2633 are 180˚ out of phase will help reduce the RMS value of the ripple current seen by the input capacitors. That will help extend input capacitor life span and result in a more efficient system. In a mobile CPU application, both the CPU core and GTL bus voltages are rather low compared to the input voltage. The corresponding duty cycles are therefore less than 50%, which means there will be no over-lapping between the two channels' input current pulses. The equation for calculating the maximum total input ripple RMS current is therefore:

$$I_{irrm} = \sqrt{I_1^2 D_1(1-D_1) + I_2^2 D_2(1-D_2) - 2I_1 I_2 D_1 D_2} \quad (15)$$

where I1 is maximum load current of Channel 1, I2 is the maximum load current of Channel 2, D1 is the duty cycle of Channel 1, and D2 is the duty cycle of Channel 2.

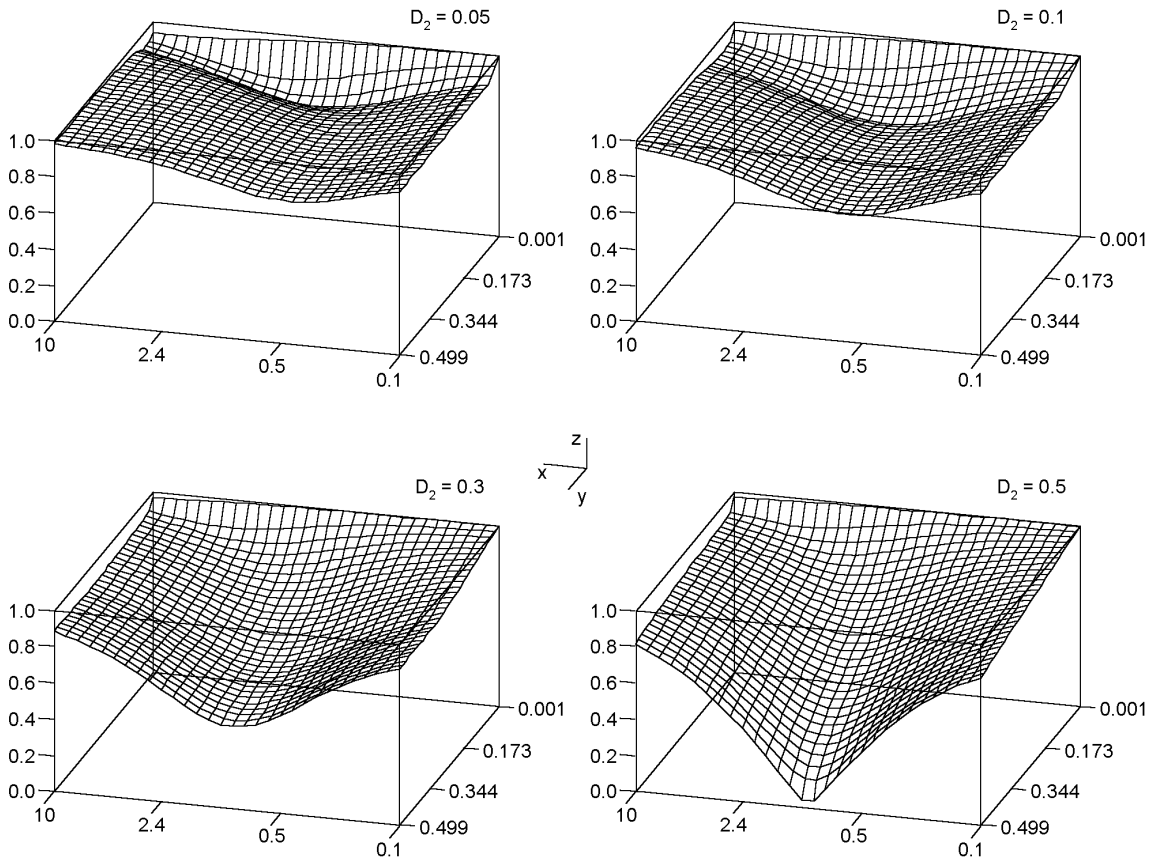
Example: $I_{load\_max\_1}$ = 6.8A, $I_{load\_max\_2}$ = 2A, D1 = 0.09, and D2 = 0.1.

$$I_{irrm} = [(6.8A)^2 \times 0.09 \times (1-0.09) + (2A)^2 \times 0.1 \times (1-0.1) - 2 \times 6.8A \times 2A \times 0.09 \times 0.1]^{0.5} = 1.97A$$

Choose input capacitors that can handle 1.97A ripple RMS current at highest ambient temperature. The input capacitors should also meet the voltage rating requirement. In this case, a SANYO OSCON capacitor 25SP33M, or a Taiyo Yuden ceramic capacitor TMK325BJ475, will meet both requirements. Comparison: If the two channels are operating in phase, the ripple RMS value would be 2.52A. The equation for calculating ripple RMS current takes the same form as the one above but the meanings of the variables change. I1 is the sum of the maximum load currents, D1 is the small duty cycle of the two, D2 is the difference between the two duty cycles, and I2 is the maximum load current of the channel that has larger duty cycle.

Figure 6 shows how the reduction of input ripple RMS current brought by the 2-phase operation varies with load current ratio and duty cycles. From the plots, it can be seen that the benefit of the 2-phase operation tends to maximize when the two load currents tend to be equal. Another conclusion is that the ratio increases rapidly when one channel's duty cycle is catching up with the other channel's and then becomes almost flat when the former exceeds the latter. So the absolute optimal operating point in terms of input ripple is at D1 = D2 = 0.5 and $I_{load\_max\_1} = I_{load\_max\_2}$, when the input ripple current is zero for 2-phase operation.

Input Capacitor Selection (Continued)



x axis - load current ratio: Channel 1 vs. Channel 2
y axis - Channel 1 duty cycle (D_1)
z axis - input ripple RMS current ratio: 2-phase vs. in-phase

20000884

FIGURE 6. Input Ripple RMS Current Ratio: 2-phase vs. In-phase

Control Loop Design

Samll Signal Model

The buck regulator small signal model is shown in *Figure 7*. The model is obtained by applying the current-controlled PWM switch derived by Vorperian and by omitting portions that are irrelevant in a buck topology.

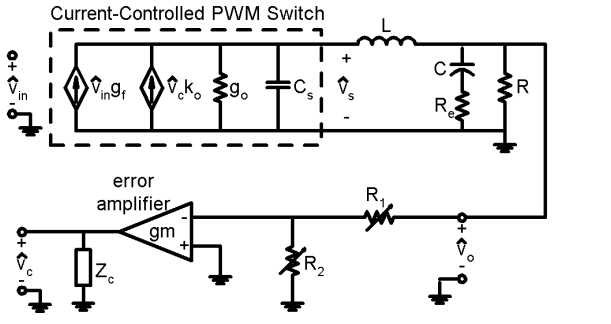


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FIGURE 7. Small Signal Model of Buck Regulators

In the model, the DC output conductance of the PWM switch is:

Control Loop Design (Continued)

$$g_o = \frac{1}{Lf}\left[D'm_c - 0.5\right] \quad (16)$$

Where

$$D' = 1-D \quad (17)$$

$$m_c = 1 + \frac{S_e}{S_n} \quad (18)$$

$$S_e = V_m \bullet f \quad (19)$$

$$S_n = \frac{D'V_{in}}{L} \times R_i \quad (20)$$

$$R_j = R_{ds} \bullet \rho \quad (21)$$

S_e is the correction ramp slope, S_n is the on-time slope of the current sense waveform, V_m is the peak-peak value of the correction ramp, f is the PWM frequency, V_{in} is input voltage, R_i is the transfer function from inductor current to ramp voltage, R_{ds} is the top FET on resistance and r is the gain of the current sense amplifier.

The coefficient of the first current source is:

$$g_f = D \times g_o - \frac{D(1-D)}{2L \times f} \quad (22)$$

and the coefficient of the second current source is:

$$k_o = \frac{1}{R_i} \quad (23)$$

The output capacitance of the PWM switch is:

$$C_s = \frac{1}{L \cdot \pi^2 f^2} \quad (24)$$

The DC resistance of the FET switches and of the inductor is not included here because its value is usually much smaller than the load resistance.

Control-Output Transfer Function

The control voltage in a peak-current mode scheme such as that of the LM2633 is the current command. At any instant that voltage determines the level of the inductor current (from an average-model point of view). The control-output transfer function is obtained by letting the small signal component of the input voltage be zero (i.e. .). The expression for the control-output transfer function is:

$$G(s) = \frac{\hat{V}_o}{\hat{V}_c} = k_o \times R \times \frac{1 + sCR_e}{s^3 \times \alpha = s^2 \times \beta + s \times \gamma + \delta} \quad (25)$$

Where

$$\alpha = LC_sC(R + R_e) \quad (26)$$

$$\beta = g_oLC(R + R_e) + C_s(CRR_e + L) \quad (27)$$

$$\gamma = C(R + R_e) + g_o(CRR_e + L) + C_sR \quad (28)$$

$$\delta = 1 + g_oR \quad (29)$$

For a reasonable design, the output filter has large attenuations at large complex frequencies (i.e. large s values). At s values where 1/sC is smaller than R_e, the transfer function can be re-written as:

$$\frac{\hat{V}_o}{\hat{V}_c} = k_oR_e \times \frac{1}{1 + \frac{s}{2\pi f_nQ} + \frac{s^2}{(2\pi f_n)^2}} \quad (30)$$

Where

$$f_n = \frac{f}{2} \quad (31)$$

$$Q = \frac{1}{\pi\,(D'mc - 0.5)} \quad (32)$$

Since the denominator of the control-output transfer function is a third-order polynomial, and its coefficients are positive real numbers, the transfer function either has one real pole and two complex poles that are complex conjugates or has three real poles. Thus it can be approximately written in the following format:

$$G(s) = \frac{\hat{V}_o}{\hat{V}_c} \cong M.F_p(s).F_h(s) \quad (33)$$

Where

$$M = \frac{R}{R_i} \cdot \frac{1}{1 + \frac{R}{Lf}\left(D'm_c - 0.5\right)} \quad (34)$$

and

$$F_p(s) = \frac{1 + \frac{s}{2\pi f_z}}{1 + \frac{s}{2\pi f_p}} \quad (35)$$

where

$$f_z = \frac{1}{CR_e} \quad (36)$$

and

$$F_h(s) = \frac{1}{1 + \frac{s}{2\pi f_nQ} + \frac{s^2}{(2\pi f_n)^2}} \quad (37)$$

The value of f_p can be determined by comparing the denominators of *Equation (21)* and *Equation (25)*. The result is:

$$f_p \cong \frac{1}{2\pi CR} + \frac{1}{2\pi LCF}\left(D'm_c - 0.5\right) \quad (38)$$

Control Loop Design (Continued)

From the above expressions, it can be seen that the control-output transfer function has three poles and one zero. Of the three poles, one is a real pole (f_p) that is located at low frequency, the other two are either complex conjugates that are located at half the switching frequency (f_n), or are separated real poles, depending on the Q value. When Q value is less than 0.5, the two high frequency poles will become two real poles.

From *Equation (24)* it can be told that Q will become negative when $m_c < 1/(2D')$. A negative Q value means an unstable system because the control-output transfer function will have a right-half-plane pole.

$$D' = 1 - \frac{1.6V}{10V} = 0.84$$

$$R_j = 10m\Omega \times 5 = 50m\Omega$$

$$S_e = 0.25V \times 250kHz = 62.5mV/\mu s$$

$$S_n = \frac{0.84 \times 10V}{1.5\mu H} \times 50m\Omega = 280mV/\mu s$$

$$m_c = 1 + \frac{62.5}{280} = 1.22$$

$$f_n = 250kHz \div 2 = 125kHz$$

$$Q = \frac{1}{\pi \times (0.84 \times 1.22 - 0.5)} = 0.61$$

$$f_p = \frac{1}{2\pi \times 2mF \times 0.4\Omega} + \frac{0.84 \times 1.22 - 0.5}{2\pi \times 1.5mH \times 2\mu F \times 250kHz} = 310Hz$$

$$f_z = \frac{1}{2\pi \times 2mF \times 9m\Omega} = 8.8kHz$$

$$M = \frac{0.4\Omega}{50m\Omega} \times \frac{1}{1 + \frac{0.4\Omega}{1.5\mu H \times 250kHz}\left(0.84 \times 1.22 - 0.5\right)} = 5.1$$

The resulting gain plot is shown in *Figure 8* as the asymptotic plot. The plots of the actual gain and phase as computed by *Equation (25)* are also shown.

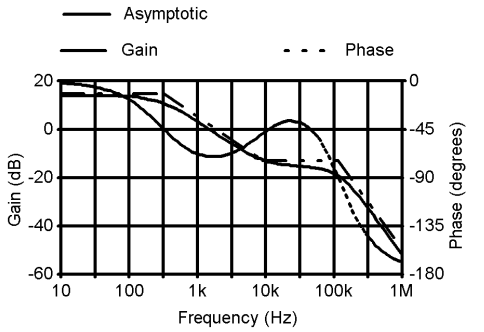


FIGURE 8. Example Control-Output Transfer Function Bode Plot

It should be noted that load resistance only changes the low frequency gain. This is because the location of the low frequency pole changes with load.

Frequency Compensation Design

The general purpose to compensate the loop is to meet static and dynamic performance requirements while maintaining stability. Loop gain is what is usually checked for small-signal performance. Loop gain is equal to the product of control-output transfer function (or so-called 'plant') and the output-control transfer function (i.e. the compensation network transfer function). Different compensation schemes result in different trade-offs among static accuracy, transient response speed and degree of stability, etc.

Generally speaking it is a good idea to have a loop gain slope that is −20dB/decade from a very low frequency to well beyond cross-over frequency. The cross-over frequency should not exceed one-fifth of the switching frequency, i.e. 50kHz in the case of LM2633. The higher the bandwidth, the potentially faster the load transient speed. However, if the duty cycle saturates during the load transient, then further increasing the small signal bandwidth will not help. In the context of CPU core or GTL bus power supply, a small-signal bandwidth of 20kHz to 30kHz should be sufficient if output capacitors are not just MLCs.

Since the control-output transfer function usually has very limited low frequency gain (see *Figure 8*), it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain especially the DC gain will be very large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the plant shape. If a typical shape such a that shown in *Figure 8* is assumed, then the following can be done to create a −20dB/decade roll-off of the loop gain.

Place the first zero at f_p, the second pole at f_z, and the second zero at f_n, then the resulting loop gain plot will be of −20dB/dec slope from zero frequency up to f_n (half the switching frequency).

Figure 9 shows the gain plot of such a two-pole two-zero (more accurately, a lag-lag) compensation network, where f_{z1}, f_{z2} and f_{p2} are the first zero, second zero and second pole frequencies. The first pole f_{p1} is located at zero frequency.

Control Loop Design (Continued)

TABLE 4. R1 and R2 Values vs. VID

VID4:0	V_{DAC} (V)	R_1	R_2	r = R2/(R1+R2)
00000	2.00	25k	17.1k	0.41
00001	1.95	25k	18.4k	0.42
00010	1.90	25k	17.4k	0.41
00011	1.85	25k	21.4k	0.46
00100	1.80	25k	19.3k	0.43
00101	1.75	25k	22.0k	0.47
00110	1.70	25k	22.1k	0.47
00111	1.65	25k	30.0k	0.55
01000	1.60	25k	24.5k	0.49
01001	1.55	25k	27.3k	0.52
01010	1.50	25k	26.0k	0.51
01011	1.45	25k	34.6k	0.58
01100	1.40	25k	29.3k	0.54
01101	1.35	25k	36.0k	0.59
01110	1.30	25k	36.4k	0.59
01111	NO CPU	25k	64.3k	0.72
10000	1.275	12.5k	23.2k	0.65
10001	1.250	12.5k	25.7k	0.67
10010	1.225	12.5k	24.5k	0.66
10011	1.200	12.5k	32.1k	0.72
10100	1.175	12.5k	27.5k	0.69
10101	1.150	12.5k	33.3k	0.73
10110	1.125	12.5k	33.6k	0.73
10111	1.100	12.5k	56.2k	0.82
11000	1. 075	12.5k	39.6k	0.76
11001	1.050	12.5k	47.4k	0.79
11010	1.025	12.5k	43.4k	0.78
11011	1.000	12.5k	75.0k	0.86
11100	0.975	12.5k	53.7k	0.81
11101	0.95	12.5k	81.8k	0.87
11110	0.925	12.5k	83.7k	0.87
11111	0.900	12.5k	∞	1

The signal path from output voltage to control voltage is the feedback path. It typically contains a voltage divider, an error amplifier and a compensation network. Those are shown In *Figure 7* as R_1, R_2, the gm amplifier, and Z_c. For Channel 1 of the LM2633, since an R-2R ladder network is used, R_1 and R_2 values change with the VID setting. For information regarding their values and ratios, refer to *Table 4*. For Channel 2, R_1 and R_2 are simply the external voltage divider resistors.

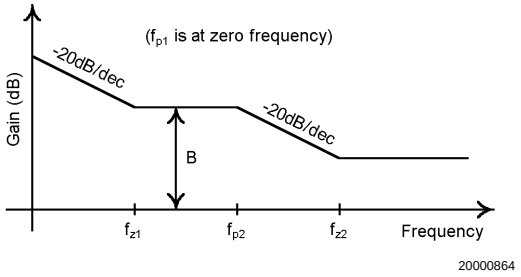


FIGURE 9. 2-Pole 2-Zero (lag-lag) Network Asymptotic Gain Plot

To achieve the gain shape in *Figure 9*, Z_c in *Figure 7* should take the form of two RC branches in parallel, as shown in *Figure 10*. In the scheme, C1 and R3 form the first zero f_{z1}, C2 and R3 form the second pole f_{p2}, and C2 and R4 form the second zero f_{z2}.

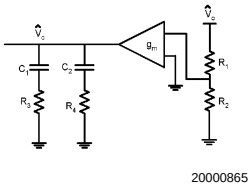


FIGURE 10. Compensation Network

The gain of the compensation network can be calculated as the following. If the ESR zero frequency f_z is higher than the low frequency pole f_p, then there should be a −20dB/decade section from f_p to f_z in the plant gain plot, such as shown in *Figure 8*. Find the frequency where this section (or the extension of this section) crosses 0dB by using the following equation:

$$f_{c\_o} = M \bullet f_p \quad (39)$$

If the desired loop transfer function cross-over frequency is f_{c_c}, then the gain of the compensation network at f_p should be:

$$K = \frac{f_{c\_c}}{f_{c\_o}} \quad (40)$$

To determine the component values in *Figure 10*, the following equations can be used:

$$R_3 = \frac{B}{g_m} \times \frac{R_1 + R_2}{R_2} \quad (41)$$

where B is the desired gain at f_{z1}, and g_m is the transconductance of the error amplifier.

$$C_1 = \frac{1}{2\pi f_{z1} \times R_3} \quad (42)$$

$$C_1 = \frac{1}{2\pi f_{p2} \times R_3} \quad (43)$$

Control Loop Design (Continued)

$$R_4 = \frac{1}{2\pi f_{z2} \times C_2} \quad (44)$$

Back to the example. Let B = K, $f_{z1} = f_p$, $f_{p2} = f_z$, $f_{z2} = f_n$, then:

$$f_{c\_o} = 5.1 \times 310Hz = 1581Hz$$

$$K = \frac{20kHz}{1.581kHz} = 12.7$$

$$R_3 = \frac{12.7}{670\ \mu mho} \times \frac{1}{0.49} = 38.7k\Omega \cong 39k\Omega$$

$$C_1 = \frac{1}{2\pi \times 310Hz \times 39k\Omega} = 13.2nF \cong 13nF$$

$$C_2 = \frac{1}{2\pi \times 8.8kHz \times 39k\Omega} = 464pF \cong 470pF$$

$$R_4 = \frac{1}{2\pi \times 125kHz \times 470pF} = 2.7k\Omega$$

The corresponding Bode plots of the compensation network and the loop transfer function are shown in *Figure 11* and *Figure 12* respectively.

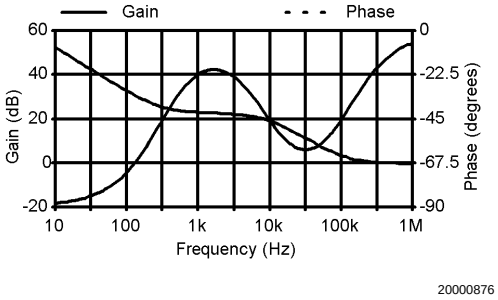


FIGURE 11. Example Compensation Transfer Function

It can be seen from *Figure 12* that the crossover frequency is 20kHz, and the phase margin is about 84 degrees.

One thing that should be pointed out is this Bode plot is only for the 0.4Ω load. That is, when load current is 4A. If load current is lower than 4A, the portion of the gain plot from fp to 310Hz will be −40dB/dec. If load current is higher than 4A, then the portion of the gain plot from 310Hz to fp will be flat. However, this usually does not have much effect on the cross-over frequency and phase margin because it happens at low frequencies.

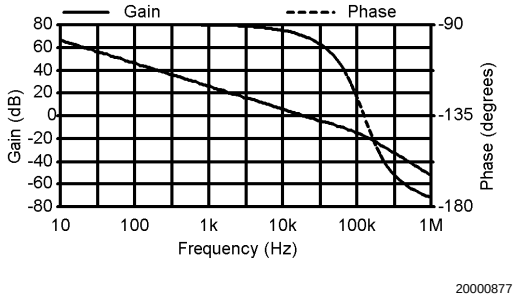


FIGURE 12. Example Loop Transfer Function

The power stage component selection can be significantly different from the example values. *Figure 13* shows how the two high frequency poles of a current-mode-control buck regulator change with the Q value.

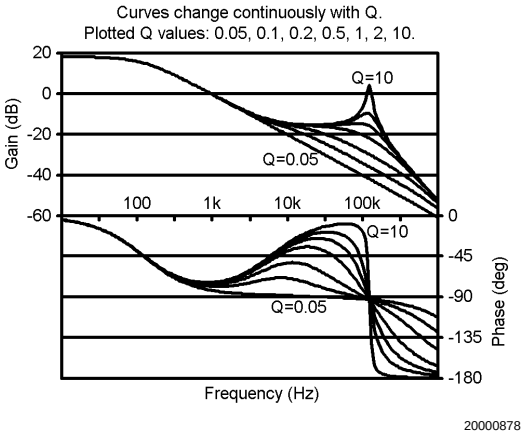


FIGURE 13. How Control Output Transfer Function Changes with Q Values

When Q is higher than 0.5, there will be a double-pole at half the switching frequency f_n. When Q is lower than 0.5, the double-pole is damped and becomes two separate poles. The lower the Q value is, the farther apart the two poles are. When Q is too low (such as Q = 0.05 or lower), one of the two high frequency poles may move well into the low frequency region. When Q is too high (such as Q = 5 or higher), there will be significant peaking at half the switching frequency and the phase will rapidly go to −180˚ near it. This typically results in a lower cross-over frequency so that the peaking in the loop gain is well below the 0dB line.

Q is a function of duty cycle and the deepness of the ramp compensation (m_c). See *Equation (32)*. The larger the duty cycle, the higher the Q value. The deeper the ramp compensation, the lower the Q value. When the inductor current ramp is too much smaller than the compensation ramp, one of the two high frequency poles will move far into the low frequency region and form a double-pole with the existing low frequency pole f_p. That makes a voltage-mode control.

The ramp compensation becomes deeper when inductance is increased, or input voltage is decreased, or sense resistance is decreased.

In the case of Channel 1 of LM2633, if L = 1 to 3µH, V_{in} = 5 to 24V, V_o = 0.925 to 2V, R_{ds} = 5 to 20mΩ, the Q value will be between 0.65 and 0.2.

Control Loop Design (Continued)

Audio Susceptibility

Audio susceptibility is the transfer function from input to output. In a typical power supply design, it is desirable to have as much attenuation in that transfer function as possible so that noise appearing at the input has little effect on the output. The open-loop audio susceptibility given by the model in *Figure 7* is:

$$A^o = \frac{\hat{V}_o}{\hat{V}_{in}} \cong \frac{D[m_c D' - (1-D/2)]}{\frac{Lf}{R} + (m_c D' - 0.5)} F_p(s) F_h(s) \quad (45)$$

The closed-loop audio susceptibility is simply:

$$A^c = \frac{A^o}{1+G(s)H(s)} \quad (46)$$

where H(s) is the compensation transfer function defined by:

$$H(s) = \frac{\hat{V}_c}{\hat{V}_o} \quad (47)$$

It can be seen from *Equation (45)* that if mc is equal to 1/(2D')+0.5, then the open-loop audio susceptibility is zero. Unfortunately, the transfer function is rather sensitive to the value of m_c around the critical value and thus this phenomenon is of little value.

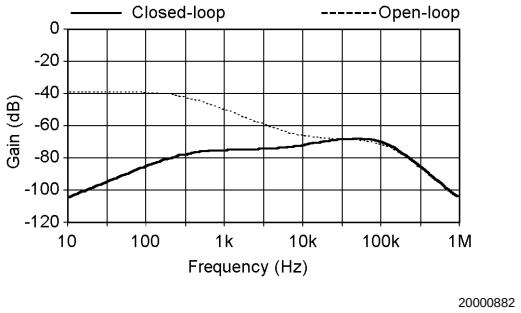


FIGURE 14. Example Audio Susceptibility Gain

The open-loop and closed-loop audio susceptibility of the previous example is shown in *Figure 14*. It can be told, both from the model and from *Equation (45)*, that open-loop gain of audio susceptibility is just a level shift of the loop gain. Closed-loop audio susceptibility starts to depart from its open-loop counterpart when frequency drops below the cross-over frequency.

PCB Layout Guidelines

It is extremely important to follow the guidelines below to ensure a clean and stable operation.

1. Use a four-layer PCB.
2. Keep the FETs as close to the IC as possible.
3. Keep the power components on the right side (pins 25 through 48) of the IC and small signal components on the left side.
4. Analog ground and power ground should be separate planes and should be connected at a single point.
5. The VDDx pin decoupling capacitor should be connected to the power ground plane.
6. Input ceramic capacitors should be placed very close to the FETs and their connections to the drain of the top FET and to the source of the bottom FET should be as short as possible and should not go through power plane or ground plane.
7. HDRVx, SWx traces should be as close to each other as possible to minimize noise emission. If these two traces are longer than 2 centimeters, they should be fairly wide, such as 50mil.
8. Keep KSx trace as short as possible. Otherwise, use a trace of 50mil or wider.
9. ILIMx trace should be kept away from noisy nodes such as the switch node.
10. It is preferable to have a shorter and wider FBx trace than a longer and narrower one.
11. VLIN5 pin decoupling capacitor should be connected to the local analog ground.
12. Compensation components should be placed close to the IC, within 1 to 2 centimeters.

An example of the power stage layout is shown in *Figure 15*.

PCB Layout Guidelines (Continued)

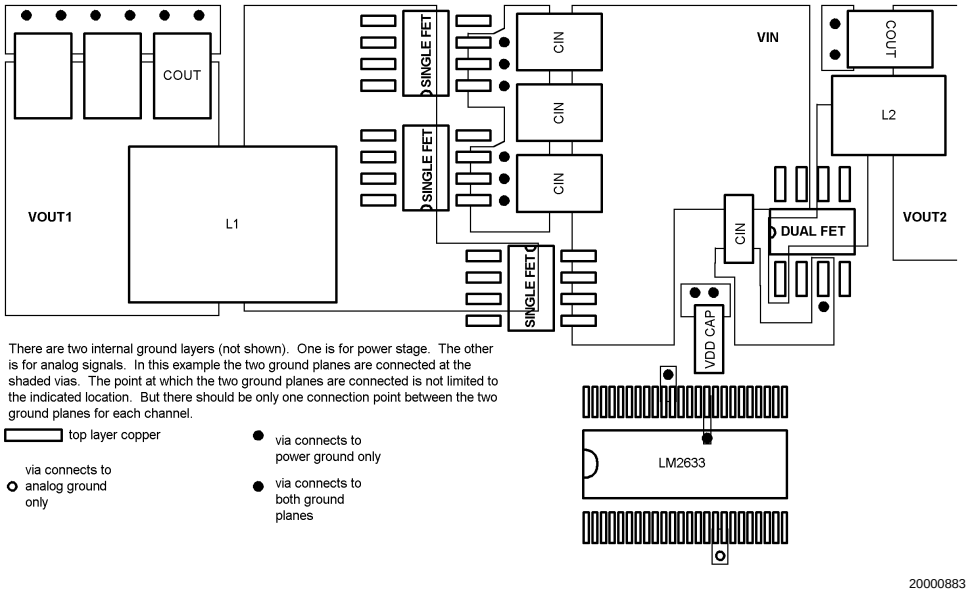
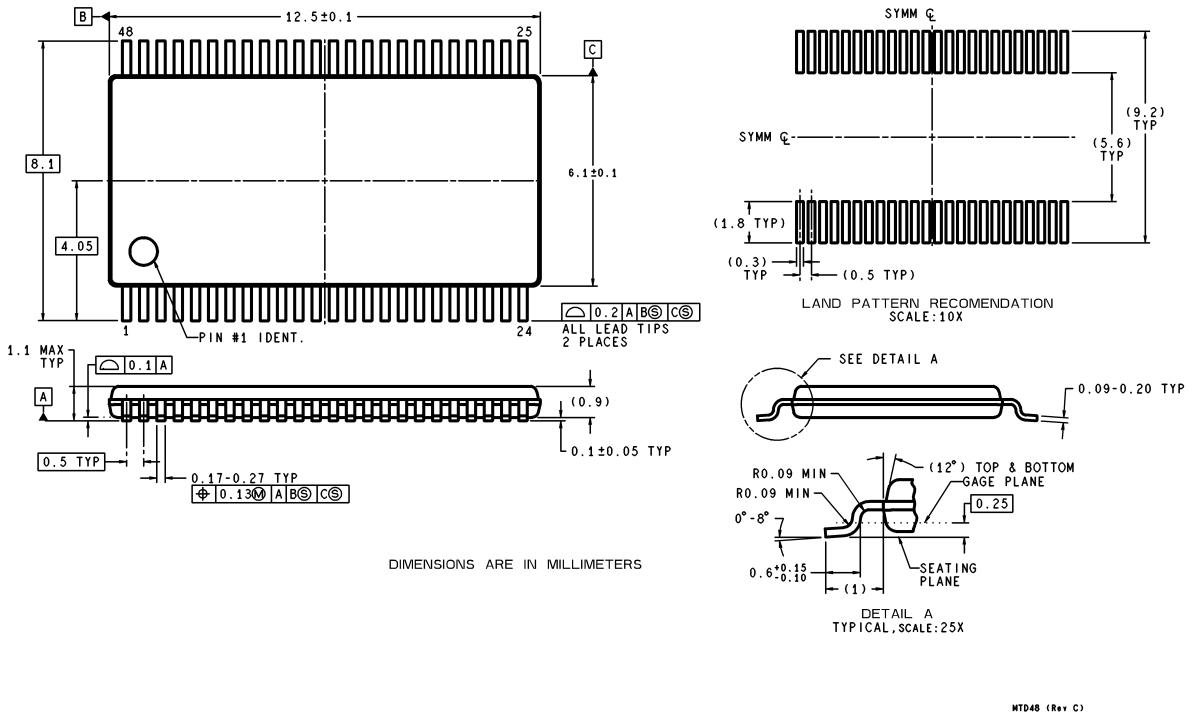


FIGURE 15. PCB Layout Example

Physical Dimensions inches (millimeters)
unless otherwise noted



48-Lead TSSOP Package
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