



# LB1976

## DC Fan Motor Driver

### Overview

The LB1976 is a three-phase brushless motor driver IC suited for use in direct PWM driving of DC fan motors for air conditioners, water heaters, and other similar equipment. Since a shunt regulator circuit is built in, single power supply operation sharing the same power supply for the motor is supported.

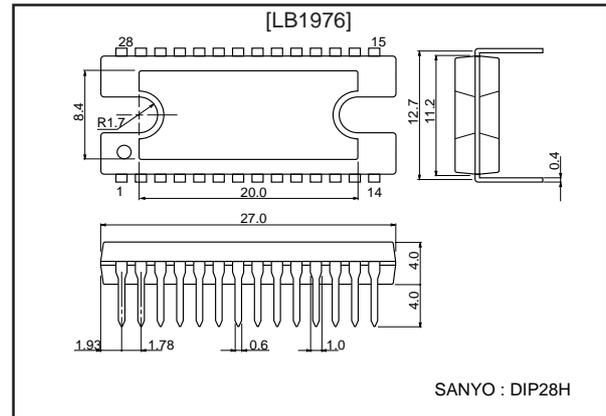
### Features

- Withstand voltage 60V, output current 2.5A
- Direct PWM drive output
- 3 built-in output top-side diodes
- Built-in current limiter
- Built-in FG output circuit

### Package Dimensions

unit: mm

#### 3147-DIP28H



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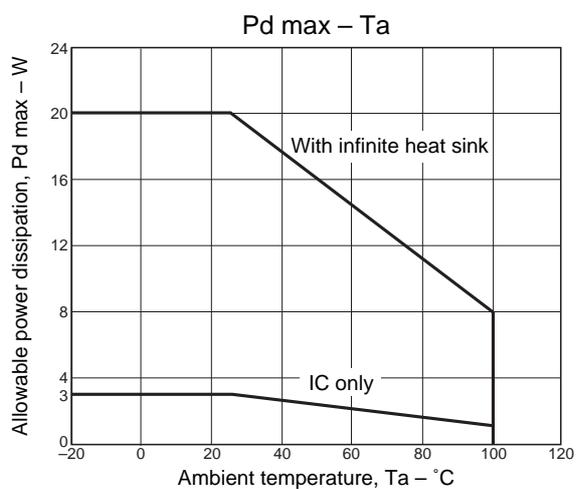
## Specifications

### Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	$V_{CC}$ max		7	V
	$V_M$ max		60	V
Output current	$I_O$ max		2.5	A
Maximum input current	$I_{REG}$ max	$V_{REG}$ pin	10	mA
Allowable power dissipation	$P_d$ max1	IC only	3	W
	$P_d$ max2	With infinite heat sink	20	W
Operating temperature	$T_{opr}$		-20 to +100	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

### Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	$V_{CC}$		4.5 to 6.7	V
	$V_M$		20 to 56	V
Input current range	$I_{REG}$	$V_{REG}$ pin	1 to 5	mA
FG pin applied voltage	$V_{FG}$		0 to $V_{CC}$	V
FG pin output current	$I_{FG}$		0 to 10	mA



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## Electrical Characteristics at Ta = 25°C, V<sub>CC</sub> = 5V, V<sub>M</sub> = 45V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply current	I <sub>CC</sub>		10	14	18	mA
[Output block]						
Output saturation voltage	V <sub>OSat1</sub> (L)	I <sub>O</sub> = 1.0A, V <sub>O</sub> (sink)		1.1	1.4	V
	V <sub>OSat1</sub> (H)	I <sub>O</sub> = 1.0A, V <sub>O</sub> (source)		0.9	1.3	V
	V <sub>OSat1</sub>	I <sub>O</sub> = 1.0A, V <sub>O</sub> (sink) + V <sub>O</sub> (source)		2.0	2.6	V
	V <sub>OSat2</sub> (L)	I <sub>O</sub> = 2.0A, V <sub>O</sub> (sink)		1.4	1.8	V
	V <sub>OSat2</sub> (H)	I <sub>O</sub> = 2.0A, V <sub>O</sub> (source)		1.2	1.7	V
	V <sub>OSat2</sub>	I <sub>O</sub> = 2.0A, V <sub>O</sub> (sink) + V <sub>O</sub> (source)		2.6	3.4	V
Output leak current	I <sub>O</sub> Leak (L)				100	μA
	I <sub>O</sub> Leak (H)		-100			μA
Top-side diode forward voltage	V <sub>FH1</sub>	I <sub>O</sub> = 1.0A		1.2	1.6	V
	V <sub>FH2</sub>	I <sub>O</sub> = 2.0A		2.1	2.6	V
[Hall amplifier]						
Input bias current	I <sub>HB</sub>		-4	-1		μA
Same-phase input voltage range	V <sub>ICM</sub>		1.5		V <sub>CC</sub> -1.5	V
Hall input sensitivity	V <sub>HIN</sub>		60			mVp-p
Hysteresis width	ΔV <sub>IN</sub> (HA)		23	32	39	mV
Input voltage [Low] -> [High]	V <sub>SLH</sub>		6	16	25	mV
Input voltage [High] -> [Low]	V <sub>SHL</sub>		-25	-16	-6	mV
[FG pin (speed pulse output)]						
Output low level voltage	V <sub>FGL</sub>	I <sub>FG</sub> = 5 mA			0.5	V
Pull-up resistor value	R <sub>FG</sub>		7.5	10	12.5	kΩ
[Current limiter]						
Limiter	V <sub>RF</sub>		0.45	0.50	0.55	V
[Thermal shutdown]						
Thermal shutdown trigger temperature	TSD	Design target Value (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target Value (junction temperature)		40		°C
[Low-voltage protection]						
Activation voltage	V <sub>LVSD</sub>		3.5	3.8	4.1	V
Deactivation voltage	V <sub>LVSD</sub> (OFF)			4.3	4.5	V
Hysteresis width	ΔV <sub>LVSD</sub>		0.4	0.5	0.6	V
[PWM oscillator]						
Output High level voltage	V <sub>OH</sub> (OSC)		2.95	3.10	3.25	V
Output Low level voltage	V <sub>OL</sub> (OSC)		1.38	1.45	1.59	V
Amplitude	V <sub>OSC</sub>		1.50	1.65	1.71	Vp-p
Ocillator frequency	f <sub>OSC</sub>	C = 2200 pF	19.6	23.0	27.6	kHz
Charge current	I <sub>CHG</sub>		-110	-94	-83	μA
Discharge resistance	R <sub>DCHG</sub>		1.6	2.1	2.6	kΩ
[V <sub>REG</sub> pin]						
Pin voltage	V <sub>REG</sub>	I <sub>REG</sub> = 1.5 mA	6.6	7.0	7.2	V
[V <sub>CTL</sub> pin]						
Input voltage	V <sub>CTL1</sub>	Output duty 0%	1.1	1.4	1.7	V
	V <sub>CTL2</sub>	Output duty 100%	3.2	3.5	3.8	V
Input bias current	I <sub>B1</sub> (CTL)	V <sub>CTL</sub> = 0V	-82			μA
	I <sub>B2</sub> (CTL)	V <sub>CTL</sub> = 5V			92	μA
[V <sub>CTL</sub> amplifier]						
Reference voltage	V <sub>CREF</sub>		2.23	2.35	2.46	V
Output voltage	V <sub>COU1</sub>	V <sub>CTL</sub> = 0V	3.90	4.20	4.40	V
	V <sub>COU2</sub>	V <sub>CTL</sub> = 5V	0.60	0.80	1.10	V
[Start/stop pin]						
High level input voltage range	V <sub>IH</sub> (S/S)		V <sub>CC</sub> -1.5		V <sub>CC</sub>	V
Low level input voltage range	V <sub>IL</sub> (S/S)		0		1.5	V
Input open voltage	V <sub>IO</sub> (S/S)		V <sub>CC</sub> -0.5		V <sub>CC</sub>	V
Hysteresis width	ΔV <sub>IN</sub> (S/S)		0.35	0.50	0.65	V
High level input current	I <sub>IH</sub> (S/S)	V (S/S) = V <sub>CC</sub>	-10	0	10	μA
Low level input current	I <sub>IL</sub> (S/S)	V (S/S) = 0V	-280	-210		μA

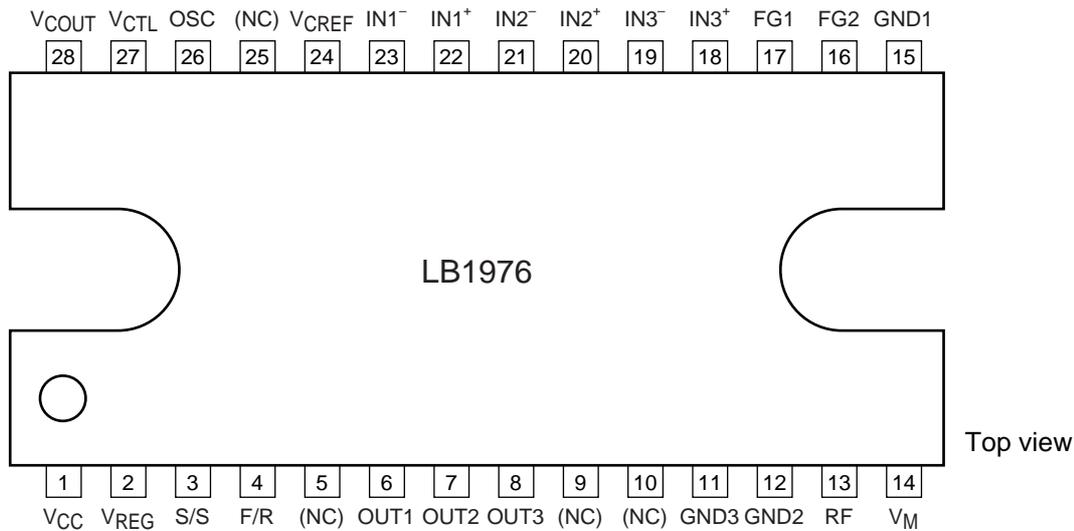
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Forward/reverse pin]						
High level input voltage range	$V_{IH}$ (F/R)		$V_{CC}-1.5$		$V_{CC}$	V
Low level input voltage range	$V_{IL}$ (F/R)		0		1.5	V
Input open voltage	$V_{IO}$ (F/R)		$V_{CC}-0.5$		$V_{CC}$	V
Hysteresis width	$\Delta V_{IN}$ (F/R)		0.35	0.50	0.65	V
High level input current	$I_{IH}$ (F/R)	$V$ (F/R) = $V_{CC}$	-10	0	10	$\mu A$
Low level input current	$I_{IL}$ (F/R)	$V$ (F/R) = 0V	-280	-210		$\mu A$

## Pin Assignment



A11963

## Truth Table

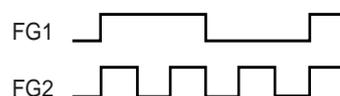
	Input			Forward/reverse control	Output	FG output	
	IN1	IN2	IN3	F/R	Source -> Sink	FG1	FG2
1	H	L	H	L	OUT2 -> OUT1	L	L
				H	OUT1 -> OUT2		
2	H	L	L	L	OUT3 -> OUT1	L	H
				H	OUT1 -> OUT3		
3	H	H	L	L	OUT3 -> OUT2	L	L
				H	OUT2 -> OUT3		
4	L	H	L	L	OUT1 -> OUT2	H	H
				H	OUT2 -> OUT1		
5	L	H	H	L	OUT1 -> OUT3	H	L
				H	OUT3 -> OUT1		
6	L	L	H	L	OUT2 -> OUT3	H	H
				H	OUT3 -> OUT2		

F/R

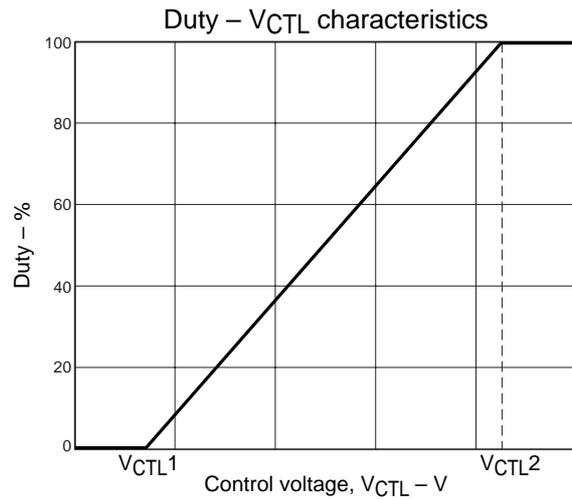
Forward rotation Low  
Reverse rotation High

0V to 1.5V  
 $V_{CC}-1.5V$  to  $V_{CC}$

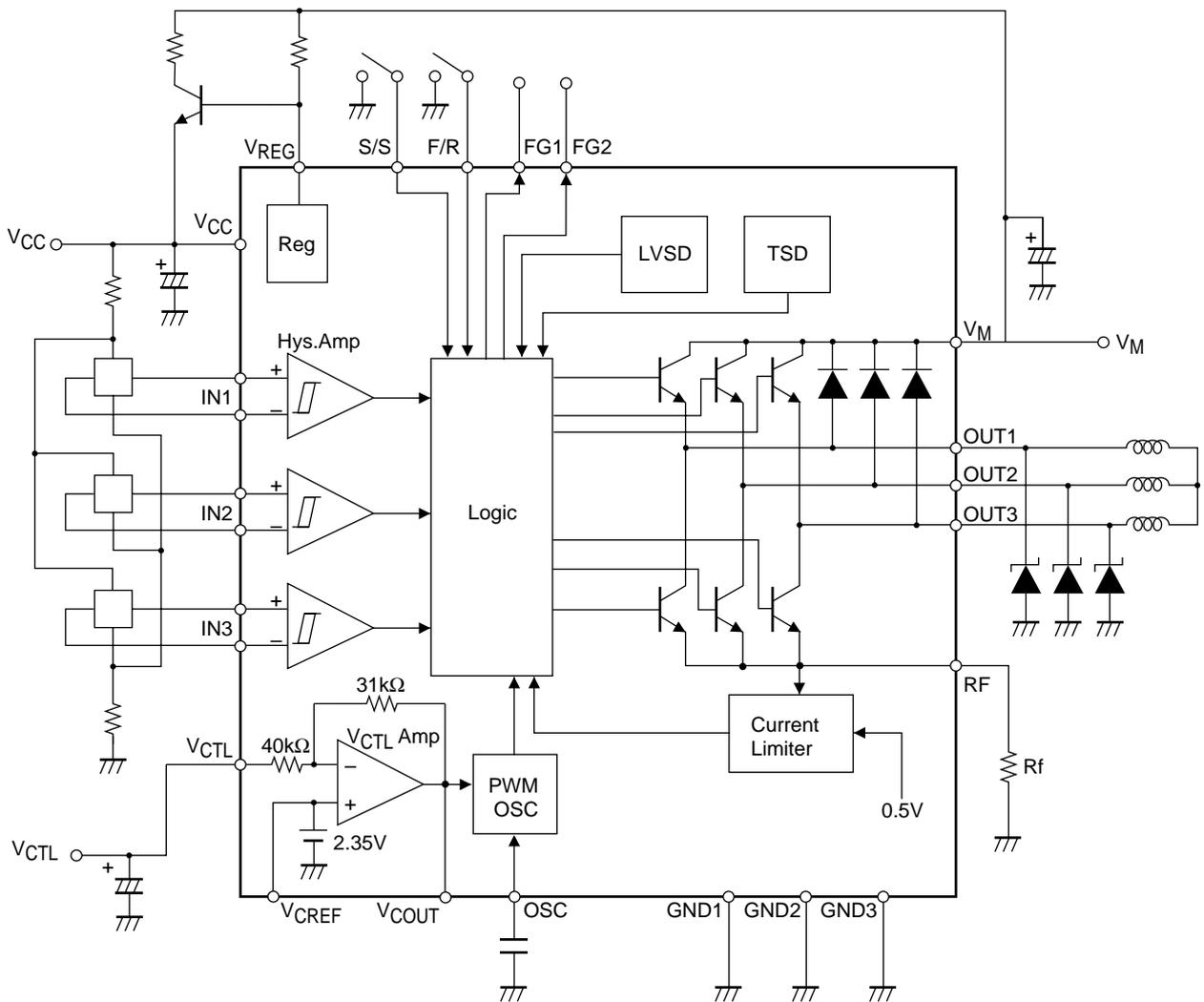
FG output



A11964



Block Diagram and Peripheral Circuitry



Pin Function

Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
1	V <sub>CC</sub>	4.5V to 6.7V		Power supply for blocks other than the output block
2	V <sub>REG</sub>	0.0V to 7.3V	<p>A11966</p>	Shunt regulator output pin (7V)
3	S/S	0.0V to V <sub>CC</sub>	<p>A11967</p>	Start/stop control pin Low: start High or Open: stop  Typical threshold voltage for V <sub>CC</sub> = 5V: approx. 2.8V (Low -> High) approx. 2.3V (High -> Low)
4	F/R	0.0V to V <sub>CC</sub>	<p>A11968</p>	Forward/reverse pin Low: forward High or Open: reverse  Typical threshold voltage for V <sub>CC</sub> = 5V: approx. 2.8V (Low -> High) approx. 2.3V (High -> Low)
6 7 8	OUT1 OUT2 OUT3		<p>A11969</p>	Output pin 1 Output pin 2 Output pin 3
13	RF	0.0V to V <sub>CC</sub>		Output current detect pin. Connect resistor RF between this pin and ground. Output current is limited to value set with V <sub>RF</sub> /R <sub>f</sub> . (Current limiter operation)
14	V <sub>M</sub>			Output block power supply
11	GND3			Output block ground

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
15 12	GND1 GND2			Ground for blocks other than the output block
17 16	FG1 FG2	0.0V to $V_{CC}$	<p style="text-align: right;">A11970</p>	Speed pulse output pin 1 with built-in pull-up resistor Speed pulse output pin 2 with built-in pull-up resistor
22 23 20 21 18 19	IN1+ IN1- IN2+ IN2- IN3+ IN3-	1.5V to $V_{CC}-1.5V$	<p style="text-align: right;">A11971</p>	Hall input pin IN+ > IN- : High input IN+ < IN- : Low input
26	OSC	1.0V to $V_{CC}$	<p style="text-align: right;">A11972</p>	This pin sets the PWM oscillation frequency. Connect a capacitor between this pin and ground.
27	$V_{CTL}$	0.0V to 6.7V	<p style="text-align: right;">A11973</p>	Output duty cycle control pin <ul style="list-style-type: none"> <li>• <math>V_{CTL} \leq V_{CTL1}</math> Duty cycle 0%</li> <li>• <math>V_{CTL1} &lt; V_{CTL} &lt; V_{CTL2}</math> Duty cycle is controlled by <math>V_{CTL}</math></li> <li>• <math>V_{CTL} \geq V_{CTL2}</math> Duty cycle 100%</li> </ul>

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
24	$V_{CREF}$	0.0V to $V_{CC}-2.0V$	<p style="text-align: right;">A11974</p>	VCTL amplifier internal reference voltage pin (2.35V)
28	$V_{COUT}$	0.7V to $V_{CC}-0.7V$	<p style="text-align: right;">A11975</p>	$V_{CTL}$ amplifier output pin

## IC Description

### 1. Direct PWM drive

This IC (LB1976) employs the direct PWM drive principle. Motor rotation speed is controlled by varying the output duty cycle according to an analog voltage input ( $V_{CTL}$ ). This eliminates the need to alter the motor power supply voltage. Compared to previous ICs using the PAM principle (such as the Sanyo LB1690), this allows simplification of the power supply circuitry. The  $V_{CTL}$  input can be directly supplied by a microcontroller, motor speed can, therefore, be controlled directly from the microcontroller.

For PWM, the source-side output transistors are switched on and off so that the ON duty tracks the  $V_{CTL}$  input. The output duty cycle can be controlled over the range of 0% to 100% by the  $V_{CTL}$  input.

### 2. PWM frequency

The PWM oscillator frequency  $f_{PWM}$  [Hz] is set by the capacitance  $C$  [pF] connected between the OSC pin and GND. The following equation applies:

$$f_{PWM} \cong 1 / (1.97 \times C) \times 10^8$$

Because output transistor on/off switching is subject to a delay, setting the PWM frequency to a very high value will cause the delay to become noticeable. The PWM frequency therefore should normally be kept below 40 kHz (typ.), which is achieved with a capacitance  $C$  of 1300 pF or higher. For reference, the source-side output transistor switching delay time is about 2  $\mu$ s for ON and about 4  $\mu$ s for OFF.

### 3. Output diodes

Because the PWM switching operation is carried out by the source-side output transistors, Schottky barrier diodes must be connected between the OUT pins and GND (OUT1 to OUT3). Use diodes with an average forward current rating in the range of 1.0 to 2.0 A, in accordance with the motor type and current limiting requirements.

If no Schottky barrier diodes are connected externally, or if Schottky barrier diodes with high forward voltage ( $V_F$ ) are used, the internal parasitic diode between OUT and GND becomes active. When this happens, the output logic circuit may malfunction, resulting in feedthrough current in the output which can destroy the output transistors. To prevent this possibility, Schottky barrier diodes must be used and dimensioned properly.

The larger the  $V_F$  of the externally connected Schottky barrier diodes, or the hotter the IC is, the more likely are the parasitic diodes between OUT and GND to become active and the more likely is malfunction to occur. The  $V_F$  of the Schottky barrier diodes must be determined so that output malfunction does not occur also when the IC becomes hot. If malfunction occurs, choose a Schottky barrier diode with lower  $V_F$ .

### 4. Protection circuits

#### 4.1. Low voltage protection circuit

When the  $V_{CC}$  voltage falls below a stipulated level ( $V_{LVSD}$ ), the low voltage protection circuit cuts off the source-side output transistors to prevent  $V_{CC}$  related malfunction.

#### 4.2. Thermal shutdown circuit (overheat protection circuit)

When the junction temperature rises above a stipulated value (TSD), the thermal shutdown circuit cuts off the source-side output transistors to prevent IC damage due to overheating. Design the application heat characteristics so that the protection circuit will not be triggered under normal circumstances.

#### 4.3. Current limiter

The current limiter cuts off the source-side output transistors when the output current reaches a preset value (limiter value). This interrupts the source current and thereby limits the output current peak value. By connecting the resistance  $R_f$  between the RF pin and ground, the output current can be detected as a voltage. When the RF pin voltage reaches 0.5V (typ.), the current limiter is activated. It performs on/off control of the source-side output transistors, thereby limiting the output current to the value determined by  $0.5 / R_f$ .

### 5. Hall input circuit

The Hall input circuit is a differential amplifier with a hysteresis of 32 mV (typ.). The operation DC level must be within the same-phase input voltage range ( $1.5V$  to  $V_{CC} - 1.5V$ ). To prevent noise and other adverse influences, the input level should be at least 3 times the hysteresis (120 to 160 mVp-p). If noise at the Hall input is a problem, a noise-canceling capacitor (about 0.01  $\mu$ F) should be connected across the Hall input  $IN^+$  and  $IN^-$  pins.

### 6. FG output circuit

The Hall input signal at  $IN1$ ,  $IN2$ , and  $IN3$  is combined and subject to waveform shaping before being output. The signal at  $FG1$  has the same frequency as the  $FG1$  Hall input, and the signal at  $FG2$  has a frequency that is three times higher.

### 7. Start/stop control circuit

The start/stop control circuit turns the source-side output transistors OFF (motor stop) when a High signal is input at the S/S pin or when the pin is Open. When a Low signal is input at the S/S pin, the source-side output transistors are turned ON, and the normal operation state is established (motor start).

### 8. Forward/Reverse switching

This IC is designed under the assumption that forward/reverse switching is not carried out while the motor is running. If switching is carried out while the motor is running, reverse torque braking occurs, leading to a high current flow. If the current limiter is triggered, the source-side output transistors are switched off, and the sink-side output transistors go into the short brake condition. However, because the current limiter of this IC cannot control the current flowing in the sink-side output transistors, these may be destroyed by the short brake current. Therefore F/R switching while the motor is running is permissible only if the output current ( $I_O$ ) is limited to a maximum of 2.5A using the motor coil resistance or other suitable means.

F/R switching should be carried out only while a High signal is input to the S/S pin or the pin is Open (stop condition), or while the  $V_{CTL}$  pin conforms to the following condition:  $V_{CTL} \leq V_{CTL1}$  (duty cycle 0%). In any other condition, F/R switching will result in feedthrough current. The F/R pin should therefore be fixed to Low (forward) or High or Open (reverse) during use.

### 9. $V_{CC}$ , $V_M$ power supplies

When the power supply voltage ( $V_{CC}$ ,  $V_M$ ) rises very quickly when a power is first applied, a feedthrough current may occur at the output. If the current remains below about 0.2A to 0.3A, it does not pose a problem, but such a possibility should still be prevented by slowing down the voltage rise at power-on. Especially if the F/R pin is set to High or Open (reverse), a quick rise in  $V_{CC}$  is likely to cause feedthrough current. This should be prevented by ensuring that  $\Delta V_{CC} / \Delta t = 0.2 V/\mu s$  or less. Feedthrough current can also be prevented by first switching on  $V_{CC}$  and then  $V_M$  during power-on.

The sequence at power-down should be as follows. Provide a stop input to the S/S pin or a duty ratio 0% input to the  $V_{CTL}$  pin. When the motor has come to a full stop, switch off  $V_M$  and then  $V_{CC}$ . If power is switched off while the motor is still rotating or a current is flowing in the motor coil (including motor restraint or inertia rotation), a counterelectromotive current or kickback current may flow on the  $V_M$  side, depending on the motor type and power-off procedure. If this current cannot be absorbed by the  $V_M$  power supply or a capacitor,  $V_M$  voltage may rise and exceed the absolute maximum  $V_M$  rating for the IC. Ensure that this does not happen through proper design of the  $V_M$  power supply or through use of a capacitor.

Because the IC (LB1976) incorporates a shunt regulator, it can be used on a single power supply. In this case, supply  $V_{CC}$  (6.3 typ.) to the  $V_{REG}$  pin via an external NPN transistor and resistor. When not using the regulator, leave the  $V_{REG}$  pin open.

#### 10. Power supply stabilizing capacitors

If the  $V_{CC}$  line fluctuates drastically, the low-voltage protection circuit may be activated by mistake, or other malfunctions may occur. The  $V_{CC}$  line must therefore be stabilized by connecting a capacitor of at least several  $\mu\text{F}$  between  $V_{CC}$  and GND. Because a large switching current flows in the  $V_M$  line, wiring inductance and other factors can lead to  $V_M$  voltage fluctuations. As the GND line also fluctuates, the  $V_M$  line must be stabilized by connecting a capacitor of at least several  $\mu\text{F}$  between  $V_M$  and GND, to prevent exceeding  $V_{M\text{max}}$  or other problems. Especially when long wiring runs ( $V_M$ ,  $V_{CC}$ , GND) are used, sufficient capacitance should be provided to ensure power supply stability.

#### 11. $V_{\text{CREF}}$ pin, $V_{\text{COUT}}$ pin

These pins are always used in the Open condition. If chattering occurs in the PWM switching output, connect a capacitor (about 0.1  $\mu\text{F}$ ) between  $V_{\text{CREF}}$  and ground or between  $V_{\text{COUT}}$  and GND.

#### 12. IC heat dissipation fins

A heat sink may be mounted to the heat dissipation fins of this IC, but it may not be connected to GND. The sink should be electrically open.

#### 13. Sample calculation for internal power dissipation (approximate)

The calculation assumes the following parameters:

$$V_{CC} = 5\text{V}$$

$$V_M = 30\text{V}$$

Source-side output transistor ON duty cycle 80% (PWM control)

Output current  $I_O = 1\text{A}$  (RF pin average current)

(1)  $I_{CC}$  power dissipation P1

$$P1 = V_{CC} \times I_{CC} = 5\text{V} \times 14\text{mA} = 0.07\text{W}$$

(2) Output drive current power dissipation P2

$$P2 = V_M \times 11\text{mA} = 30\text{V} \times 11\text{mA} = 0.33\text{W}$$

(3) Source-side output transistor power dissipation P3

$$P3 = V_O(\text{source}) \times I_O \times \text{Duty}(\text{on}) = 0.9\text{V} \times 1\text{A} \times 0.8 = 0.72\text{W}$$

(4) Sink-side output transistor power dissipation P4

$$P4 = V_O(\text{sink}) \times I_O = 1.1\text{V} \times 1\text{A} = 1.10\text{W}$$

(5) Total internal power dissipation P

$$P = P1 + P2 + P3 + P4 = 2.22\text{W}$$

#### 14. IC temperature rise measurement

Because the chip temperature of the IC cannot be measured directly, measurement according to one of the following procedures should always be carried out.

##### 14.1. Thermocouple measurement

A thermocouple element is mounted to the IC heat dissipation fin. This measurement method is easy to implement, but it will be subject to measurement errors if the temperature is not stable.

##### 14.2. Measurement using internal diode characteristics of IC

This is the recommended measurement method. It makes use of the parasitic diode incorporated in the IC between FG1 and GND. Set FG1 to High and measure the voltage  $V_F$  of the parasitic diode to calculate the temperature.

(Sanyo data: for  $I_F = -1\text{mA}$ ,  $V_F$  temperature characteristics are about  $-2\text{mV}/^\circ\text{C}$ )

#### 15. NC pins

Because NC pins are electrically open, they may be used for wiring purpose etc.

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