

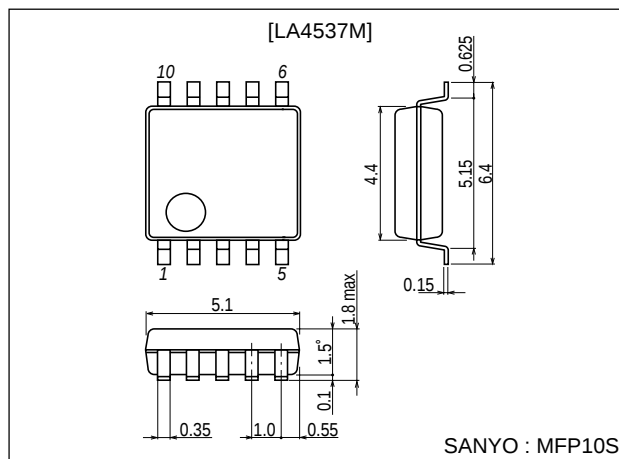
**LA4537M****Power Amplifier for 1.5V Headphone Stereos****Features**

- Low current drain.
- 16Ω load drive capability.
- Excellent reduced voltage characteristics.
- Excellent power supply ripple rejection.
- Minimum number of external parts required (no input capacitor, feedback capacitor required).
- Less harmonic interference in radio band.
- On-chip power switch function, muting function.

Package Dimensions

unit:mm

3086A-MFP10S

**Specifications****Absolute Maximum Ratings** at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max	Quiescent	4.5	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-40 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		1.5	V
Operating voltage range	V _{CC} op		0.9 to 4.0	V
Recommended load resistance	R _L		16 to 32	Ω

Operating Characteristics at Ta = 25°C, R_L=16Ω, R_g=600Ω, See specified Test Circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I _{cco1}	V _{CC} =1.2V, quiescent		3.5	6.0	mA
	I _{cco2}	V _{CC} =2.5V, pin 10 → GND		1.4	2.5	mA
	I _{cco3}	V _{CC} =2.5V, pin 1 → GND			1.0	μA
Voltage gain	V _G	V _{CC} =1.2V, f=1kHz, V _O =-20dBm	28.5	30.0	31.5	dB
Voltage gain difference	ΔV _G	V _{CC} =1.2V, f=1kHz, V _O =-20dBm			1.0	dB

Continued on next page.

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Continued from preceding page.

Note) The quiescent current is respresented by the current flowing into pin 6. The respective maximum currents flowing into pin 1 and pin 10 are calculated by (pin voltage -0.5) / 16 [V/k Ω] and the total current increases by these current values.

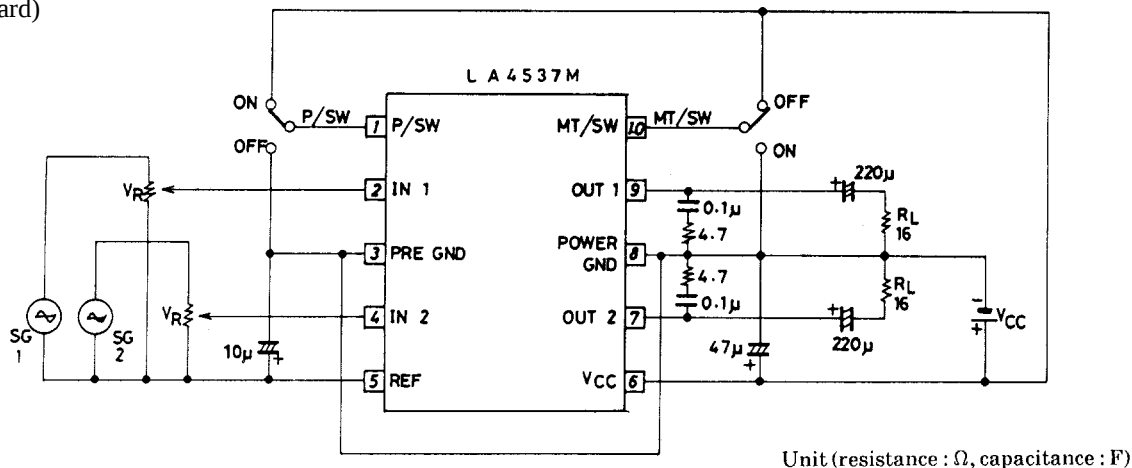
The block diagram illustrates the internal architecture of the 14-pin package. It features a central vertical line representing the signal path. At the top, a 'POWER SWITCH' block is connected to pin 1 (POWER SWITCH) and pin 2 (IN 1). Below it, a 'BIAS' block is connected to pin 5 (REF) and the central signal line. The signal line then splits into two paths, each passing through an amplifier block ('Amp 1' and 'Amp 2') before reaching the output pins (pin 9: OUT 1 and pin 7: OUT 2). A 'MUTE CIRCUIT' block is connected to pin 10 (MUTE SWITCH) and the central signal line. Pin 3 (PRE GND) and pin 8 (POWER GND) are connected to ground symbols. Pin 6 (VCC) is connected to the bottom of the central signal line.

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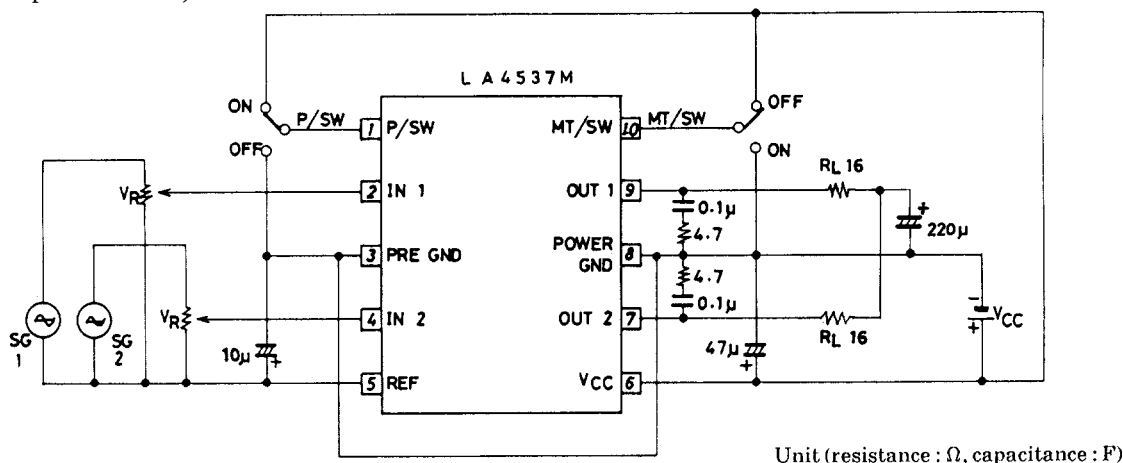
Sample Application Circuit 1

(Standard)



Sample Application Circuit 2

(Output capacitor shared)



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