

INTRODUCTION

The KS0090i is an LCD driver and controller LSI for liquid crystal dot matrix character display systems. It can display 2 or 3 lines of 12 characters with the 5×8 dots format. It is capable of interfacing with the I²C serial mode. Voltage converter (2 or 3 times), voltage regulator, divider resistor and voltage follower OP AMP are built-in to the IC, and a low operation current of 50 μ A is achieved. The slim shape of the chip makes it suitable for the COG module application and TCP. The KS0090i is an ideal solution for display on portable equipment such as hand-held phones.

FEATURES

- **Driver Outputs**

- Common output: 26 common
- Segment output: 64 segment
- Icons: 128 horizontal icons, 24×4 vertical icons, 5 static icons

- **Applicable Panel Size**

Display Size	Duty	Output Content
2 line $\times$ 12 char	1/18	(12 characters + 4 segments for signal) $\times$ 2 + 128 icons + 5 static icons
3 line $\times$ 12 char	1/26	(12 characters + 4 segments for signal) $\times$ 3 + 128 icons + 5 static icons

- **Internal Memory**

- Character generator ROM (CGROM): 10,240 bits (256 characters $\times$ 5×8 dots)
- Character generator RAM (CGRAM): 160 bits (4 characters $\times$ 5×8 dots)
- Display data RAM (DDRAM): 288 bits (12 characters $\times$ 3 lines $\times$ 8 bits)
- Segment icon RAM (ICONRAM): 224 bits ($12 \times 2 \times 5$ bits + 2×4 bits + 24×4 bits)

- **MPU Interface**

- Serial interface mode: I²C serial interface

- **Function Set**

- Various instruction set: display control, power save, power control, function set... etc.
- COM/SEG bidirectional function (4 type LCD application available)
- Hardware reset (RES pin)

- **Built-in Analog Circuit**

- On-chip oscillator with an Internal resistor or external clock input
- Electronic volume for contrast control (32 or 64 steps)
- Voltage converter (2 or 3 times) / voltage regulator / voltage follower and bias circuit

- **Low Power Consumption**
 - 80 μ A Max.: In normal mode for normal display operation
 - 10 μ A Max.: In standby mode for displaying static icon
 - 5 μ A Max.: In sleep mode when display is turned off
- **Operating Voltage Range**
 - Power supply voltage (V_{DD}): 2.4 to 5.5 V
 - LCD driving voltage ($V_{LCD} = V_0 - V_{SS}$): 11.0 V (positive process)
- **Package Type**
 - Bumped chip or TCP available

BLOCK DIAGRAM

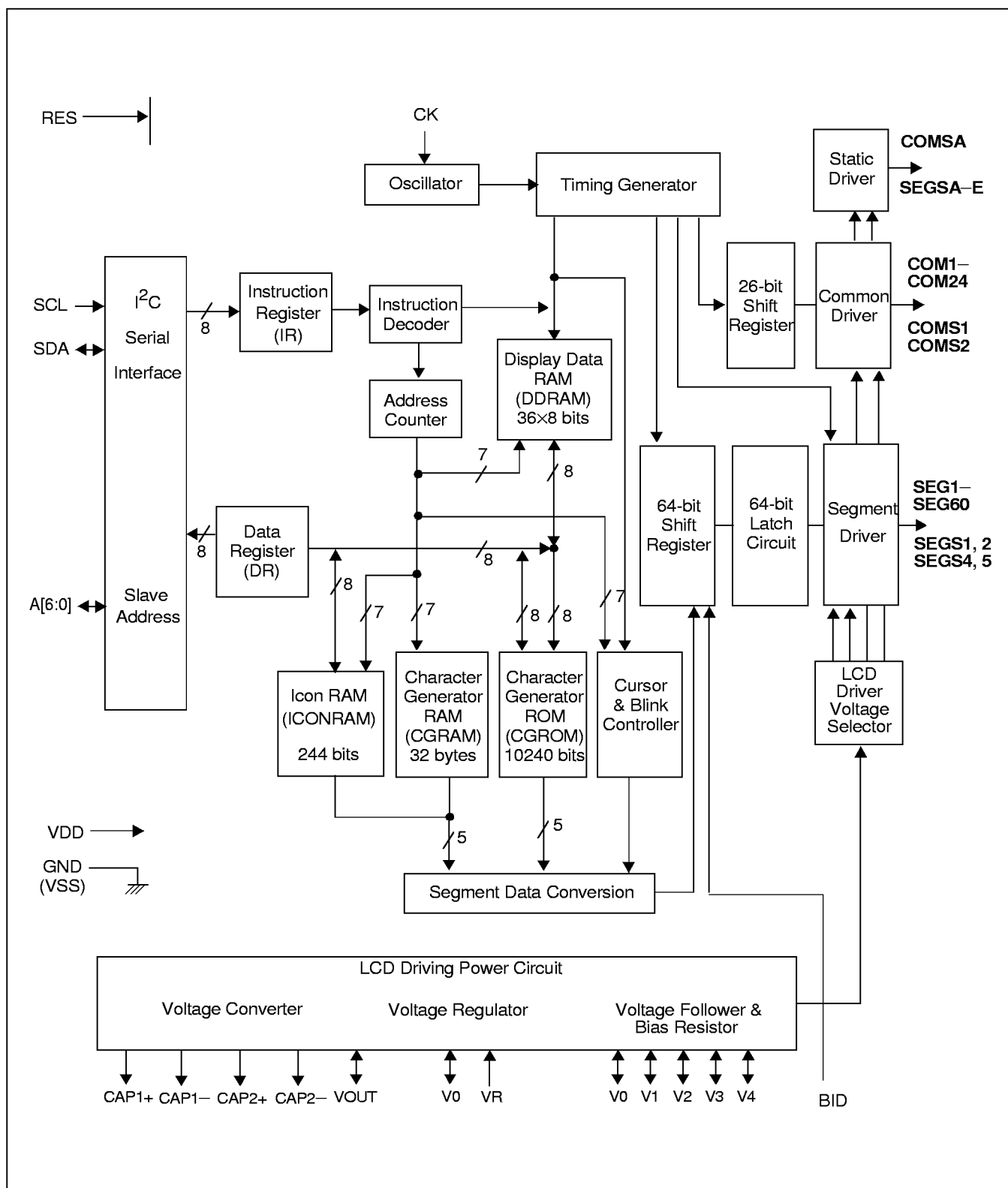
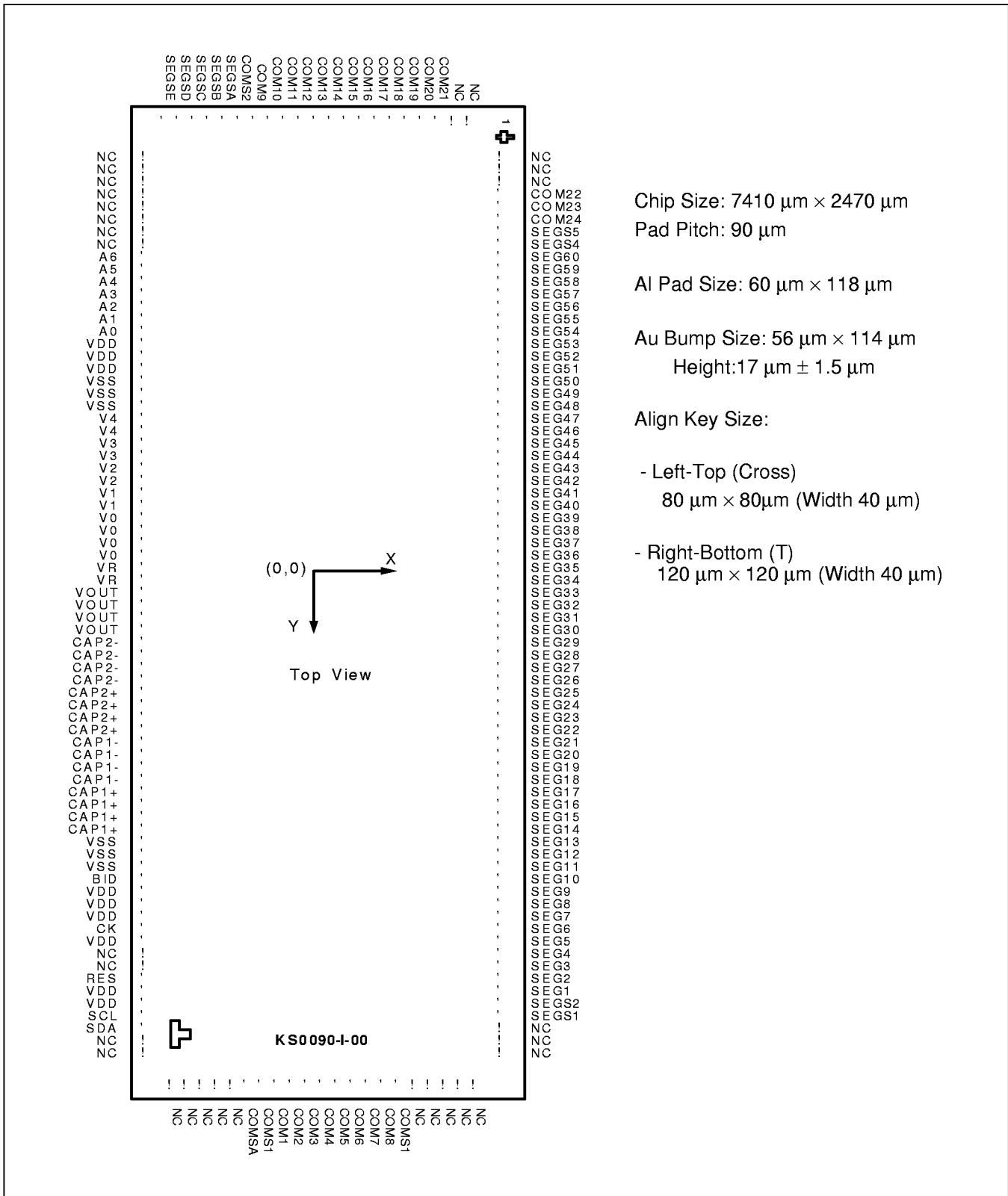


Figure 1. KS0090i Block Diagram

PAD CONFIGURATION



PAD LOCATION

[UNIT: nm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	NC1	-3540	880	31	A5	-2430	-1111	61	CAP2-	270	-1111
2	NC2	-3540	790	32	A4	-2340	-1111	62	CAP2-	360	-1111
3	COM21	-3540	700	33	A3	-2250	-1111	63	CAP2-	450	-1111
4	COM20	-3540	610	34	A2	-2160	-1111	64	CAP2-	540	-1111
5	COM19	-3540	520	35	A1	-2070	-1111	65	CAP2+	630	-1111
6	COM18	-3540	430	36	A0	-1980	-1111	66	CAP2+	720	-1111
7	COM17	-3540	340	37	V _{DD}	-1890	-1111	67	CAP2+	810	-1111
8	COM16	-3540	250	38	V _{DD}	-1800	-1111	68	CAP2+	900	-1111
9	COM15	-3540	160	39	V _{DD}	-1710	-1111	69	CAP1-	990	-1111
10	COM14	-3540	70	40	V _{SS}	-1620	-1111	70	CAP1-	1080	-1111
11	COM13	-3540	-20	41	V _{SS}	-1530	-1111	71	CAP1-	1170	-1111
12	COM12	-3540	-110	42	V _{SS}	-1440	-1111	72	CAP1-	1260	-1111
13	COM11	-3540	-200	43	V4	-1350	-1111	73	CAP1+	1350	-1111
14	COM10	-3540	-290	44	V4	-1260	-1111	74	CAP1+	1440	-1111
15	COM9	-3540	-380	45	V3	-1170	-1111	75	CAP1+	1530	-1111
16	COMS2	-3540	-470	46	V3	-1080	-1111	76	CAP1+	1620	-1111
17	SEGSA	-3540	-560	47	V2	-990	-1111	77	V _{SS}	1710	-1111
18	SEGSB	-3540	-650	48	V2	-900	-1111	78	V _{SS}	1800	-1111
19	SEGSC	-3540	-740	49	V1	-810	-1111	79	V _{SS}	1890	-1111
20	SEGSD	-3540	-830	50	V1	-720	-1111	80	BID	1980	-1111
21	SEGSE	-3540	-920	51	V0	-630	-1111	81	V _{DD}	2070	-1111
22	NC3	-3240	-1111	52	V0	-540	-1111	82	V _{DD}	2160	-1111
23	NC4	-3150	-1111	53	V0	-450	-1111	83	V _{DD}	2250	-1111
24	NC5	-3060	-1111	54	V0	-360	-1111	84	CK	2340	-1111
25	NC6	-2970	-1111	55	VR	-270	-1111	85	V _{DD}	2430	-1111
26	NC7	-2880	-1111	56	VR	-180	-1111	86	NC11	2520	-1111
27	NC8	-2790	-1111	57	VOUT	-90	-1111	87	NC12	2610	-1111
28	NC9	-2700	-1111	58	VOUT	0	-1111	88	RES	2700	-1111
29	NC10	-2610	-1111	59	VOUT	90	-1111	89	V _{DD}	2790	-1111
30	A6	-2520	-1111	60	VOUT	180	-1111	90	V _{DD}	2880	-1111

[Unit: nm]

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
91	SCL	2970	-1111	124	SEG4	2520	1070	157	SEG37	-450	1070
92	SDA	3060	-1111	125	SEG5	2430	1070	158	SEG38	-540	1070
93	NC13	3150	-1111	126	SEG6	2340	1070	159	SEG39	-630	1070
94	NC14	3240	-1111	127	SEG7	2250	1070	160	SEG40	-720	1070
95	NC15	3540	-920	128	SEG8	2160	1070	161	SEG41	-810	1070
96	NC16	3540	-830	129	SEG9	2070	1070	162	SEG42	-900	1070
97	NC17	3540	-740	130	SEG10	1980	1070	163	SEG43	-990	1070
98	NC18	3540	-650	131	SEG11	1890	1070	164	SEG44	-1080	1070
99	NC19	3540	-560	132	SEG12	1800	1070	165	SEG45	-1170	1070
100	COMSA	3540	-470	133	SEG13	1710	1070	166	SEG46	-1260	1070
101	COMS1	3540	-380	134	SEG14	1620	1070	167	SEG47	-1350	1070
102	COM1	3540	-290	135	SEG15	1530	1070	168	SEG48	-1440	1070
103	COM2	3540	-200	136	SEG16	1440	1070	169	SEG49	-1530	1070
104	COM3	3540	-110	137	SEG17	1350	1070	170	SEG50	-1620	1070
105	COM4	3540	-20	138	SEG18	1260	1070	171	SEG51	-1710	1070
106	COM5	3540	70	139	SEG19	1170	1070	172	SEG52	-1800	1070
107	COM6	3540	160	140	SEG20	1080	1070	173	SEG53	-1890	1070
108	COM7	3540	250	141	SEG21	990	1070	174	SEG54	-1980	1070
109	COM8	3540	340	142	SEG22	900	1070	175	SEG55	-2070	1070
110	COMS1*	3540	430	143	SEG23	810	1070	176	SEG56	-2160	1070
111	NC20	3540	520	144	SEG24	720	1070	177	SEG57	-2250	1070
112	NC21	3540	610	145	SEG25	630	1070	178	SEG58	-2340	1070
113	NC22	3540	700	146	SEG26	540	1070	179	SEG59	-2430	1070
114	NC23	3540	790	147	SEG27	450	1070	180	SEG60	-2520	1070
115	NC24	3540	880	148	SEG28	360	1070	181	SEGS4	-2610	1070
116	NC25	3240	1070	149	SEG29	270	1070	182	SEGS5	-2700	1070
117	NC26	3150	1070	150	SEG30	180	1070	183	COM24	-2790	1070
118	NC27	3060	1070	151	SEG31	90	1070	184	COM23	-2880	1070
119	SEGS1	2970	1070	152	SEG32	0	1070	185	COM22	-2970	1070
120	SEGS2	2880	1070	153	SEG33	-90	1070	186	NC28	-3060	1070
121	SEG1	2790	1070	154	SEG34	-180	1070	187	NC29	-3150	1070
122	SEG2	2700	1070	155	SEG35	-270	1070	188	NC30	-3240	1070
123	SEG3	2610	1070	156	SEG36	-360	1070				

NOTE: The COMS1 has two terminals (#101, #110), and these two COMS1 are the same signal at the same time.

PIN DESCRIPTION

Table 1. Pin Description

Name	I/O	Description										
Power Supply												
VDD	Power	Power supply. Connect to MPU power supply pin.										
VSS		0 V (GND)										
V0 V1 V2 V3 V4	I/O	Bias voltage level for LCD driving. Voltages have the following relationship; $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq Vss$ When the built-in power circuit is on, the following voltages are given to pin V1 to V4 using internal 1/5 bias resistors. <table><tr><td>LCD Bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr><tr><td>(1/5) Bias</td><td>(4/5) V0</td><td>(3/5) V0</td><td>(2/5) V0</td><td>(1/5) V0</td></tr></table>	LCD Bias	V1	V2	V3	V4	(1/5) Bias	(4/5) V0	(3/5) V0	(2/5) V0	(1/5) V0
LCD Bias	V1	V2	V3	V4								
(1/5) Bias	(4/5) V0	(3/5) V0	(2/5) V0	(1/5) V0								
LCD Driver Supply												
CAP1+	O	Capacitor1+ connecting pin for the internal voltage converter. This pin connects the capacitor with CAP1−.										
CAP1−		Capacitor1− connecting pin for the internal voltage converter. This pin connects the capacitor with CAP+.										
CAP2+		Capacitor2+ connecting pin for the internal voltage converter. When VOUT is 2 times boosting, this pin connects the capacitor with VDD. When 3 times boosting, this pin connects the capacitor with CAP2−.										
CAP2−		Capacitor2− connecting pin for the internal voltage converter. When VOUT is 2 times boosting, this pin is not used. When 3 times boosting, this pin connects the capacitor with CAP2+.										
VOUT	I/O	2 or 3 times DC/DC voltage converter output. This pin connects a capacitor with VDD pin.										
VR	I	Voltage adjust pin. This pin gives a voltage between V0 and Vss by resistance-division of voltage.										

Table 1. Pin Description (Continued)

Name	I/O	Description
System Control		
CK	I	External clock input pin. It must be fixed to "High" when the internal oscillation circuit is used. In the external clock mode, it is used as an external clock input pin.
BID	I	SEG direction selection pin When BID = "Low", SEGS1 → SEGS2 → SEG1 → → SEG60 → SEGS4 → SEGS5 When BID = "High", SEGS5 → SEGS4 → SEG60 → → SEG1 → SEGS2 → SEGS1
MPU Interface		
RES	I	Initialization is performed by edge sensing of the RES signal. When RES = "Low":  When RES = "High": 
SCL	I	I ² C clock input
SDA	I/O	I ² C data signal
A6 – A0	I	Used as slave address for I ² C interface. This must be fixed to "High" or "Low". This can be set arbitrary from 00h to 7Fh and the setting address is used as the slave address (identification code) in KS0090i.
LCD Driver Outputs (Dynamic)		
COM1 to COM24	O	Common signal output for character display.
COMS1, COMS2	O	Common signal output for icon display. The COMS1 has two terminals, and these two COMS1 are the same signal at the same time.
SEG1 to SEG60	O	Segment signal output for character display.
SEGS1, SEGS2 SEGS4, SEGS5	O	Segment signal output for vertical icon display.
LCD Driver Outputs (Static)		
COMSA	O	Static common signal output for static icon display.
SEGSA, B, C, D, E	O	Static segment signal output for static icon display.

FUNCTION DESCRIPTION

SYSTEM INTERFACE

KS0090i has I²C serial interface mode. KS0090i is selected when the higher 7-bit of first byte, which is transferred from the MPU after the start procedure, matches the 7-bit slave address assigned to A6~A0 pin.

During writing operation, two 8-bit registers, data register (DR) and instruction register (IR), are used. DR or IR register is selected by setting the RS flag of control bit. The data register(DR) is used as temporary data storage place for being written into DDRAM/CGRAM/ICONRAM, and one of these RAMs is selected by RAM address setting instruction. The Instruction register(IR) is used to store instruction code transferred from MPU.

Table 2. I²C Serial Interface

RES	A6 ~ A0	SCL	SDA
RESET	A6 ~ A0	I ² C clock	I ² C data

RES: MPU reset

SCL: I²C serial clock input

SDA: I²C serial data input/output

A6 ~ A0: I²C slave address input

I²C SERIAL MODE

Allows serial data transfer conforming to the I²C serial interface protocol over the serial data line (SDA) and serial transfer clock line (SCL). Here, KS0090i operates write mode only.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must be remain stable during the high period of the clock pulse. If SDA data line changes at this time, the I²C serial interface will be transferred to start or stop condition.

Start and Stop Conditions

KS0090i initiates serial data transfer with a high-to-low transition of the data line when the clock is high. This is defined as the start condition. On the contrary, KS0090i finishes serial data transfer with a low-to-high transition of the data line when the clock is high, which is defined as the stop condition.

Acknowledge

From the start to the stop condition, the number of data bytes transferred from MPU to KS0090i is unlimited. Each byte formatted with eight bits is followed by an acknowledge bit (ACK). After receiving each 8-bit data, KS0090i pulls down SDA pin to a low level. At this time the MPU must be generates an extra clock pulse for acknowledge bit transferred from KS0090i to MPU.

Therefore, if ACK is not returned, the data must be transferred again. A series of data bytes can be transferred so long as KS0090i does not meet the stop condition.

I²C Protocol

KS0090i is selected when the higher 7-bit of first byte, which transferred from the MPU after the start procedure, matches the 7-bit slave address assigned to A6~A0 pin. After being selected, KS0090i receives the subsequent data strings.

The I²C bus configuration for KS0090i write mode is shown in following.

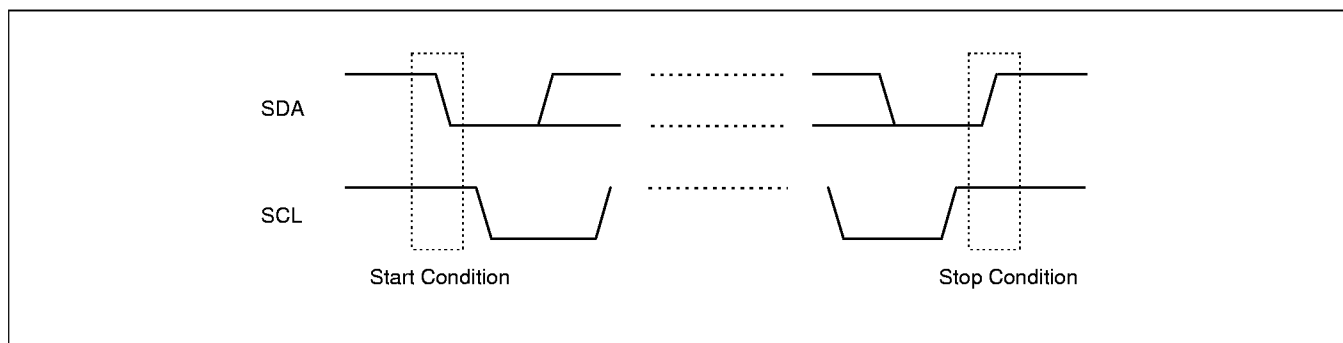


Figure 2. Definition of Start and Stop Conditions

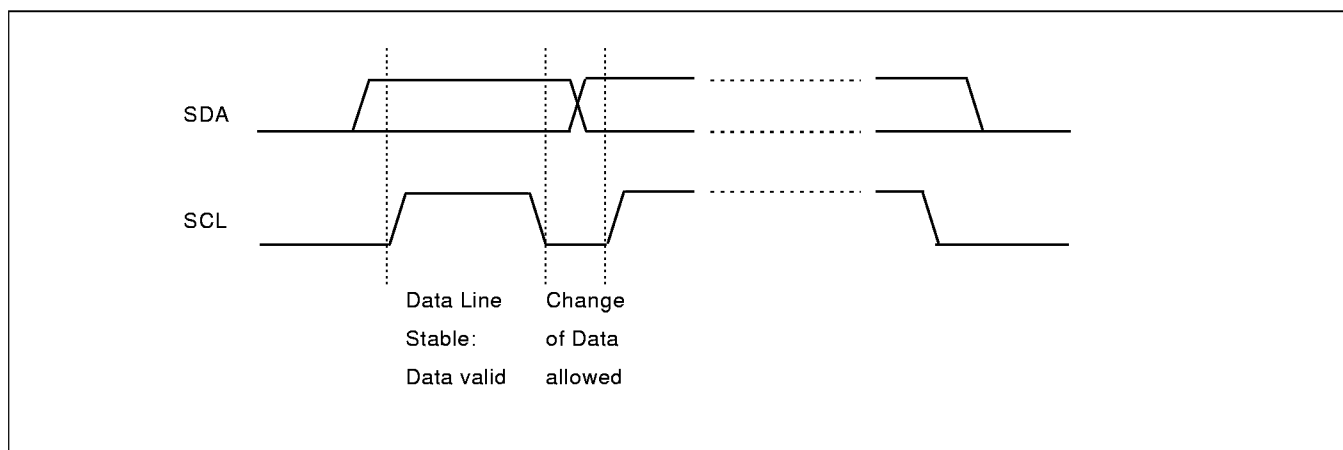


Figure 3. Bit Transfer

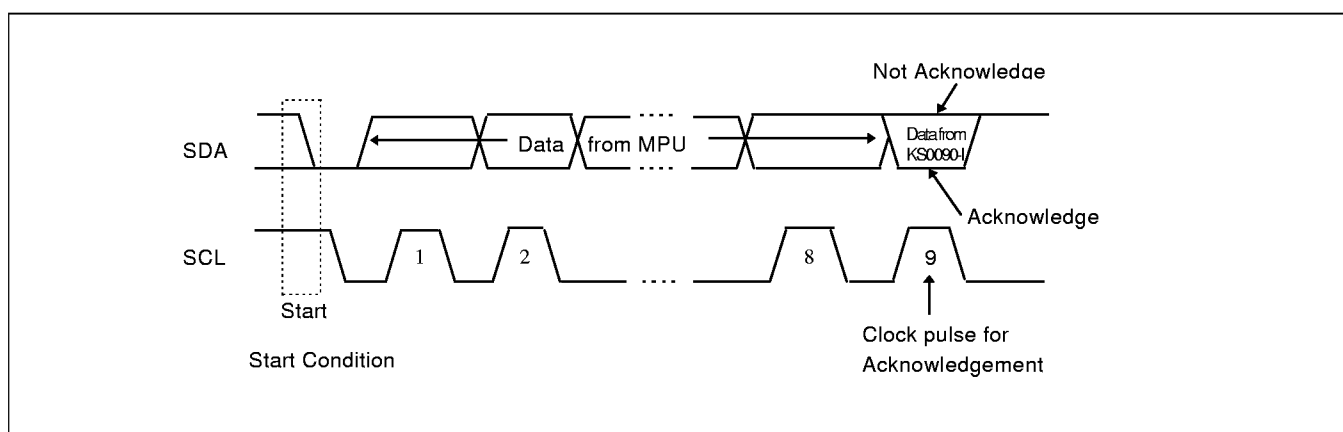


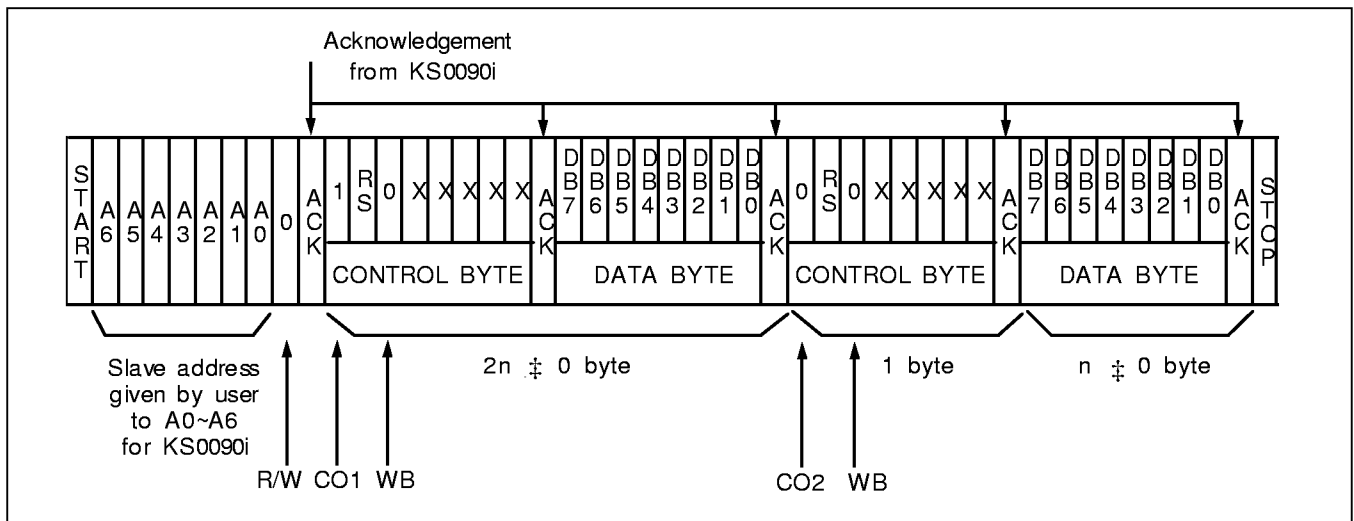
Figure 4. Acknowledgment on the I²C Interface

DATA TRANSFERRING SEQUENCE

1. Control Byte Format

Control Byte Format	CO	RS	WB	.	.	.	.	.	" . ": Don't care
CO = "0": Last control byte,									
RS = "0": Set Instruction register,									
WB = "0": Normal write operation,									
CO = "1": More control byte will follow									
RS = "1": Set data register									
WB = "1": Unexpected read mode									
KS0090i provides write-only mode of I ² C interface. So if unexpected read happen, KS0090i makes SDA floated. ACK occur after passing 8 cycle of SCL.									

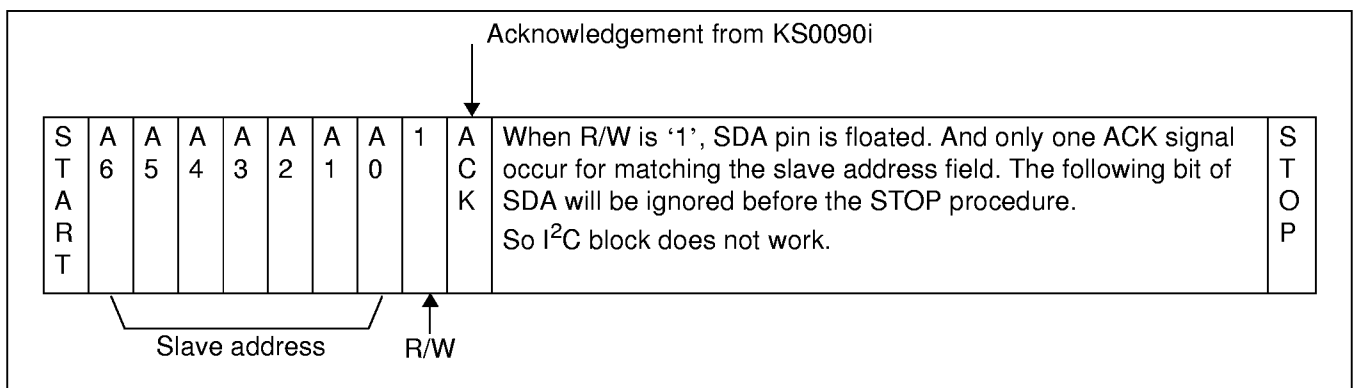
2. Normal write operation



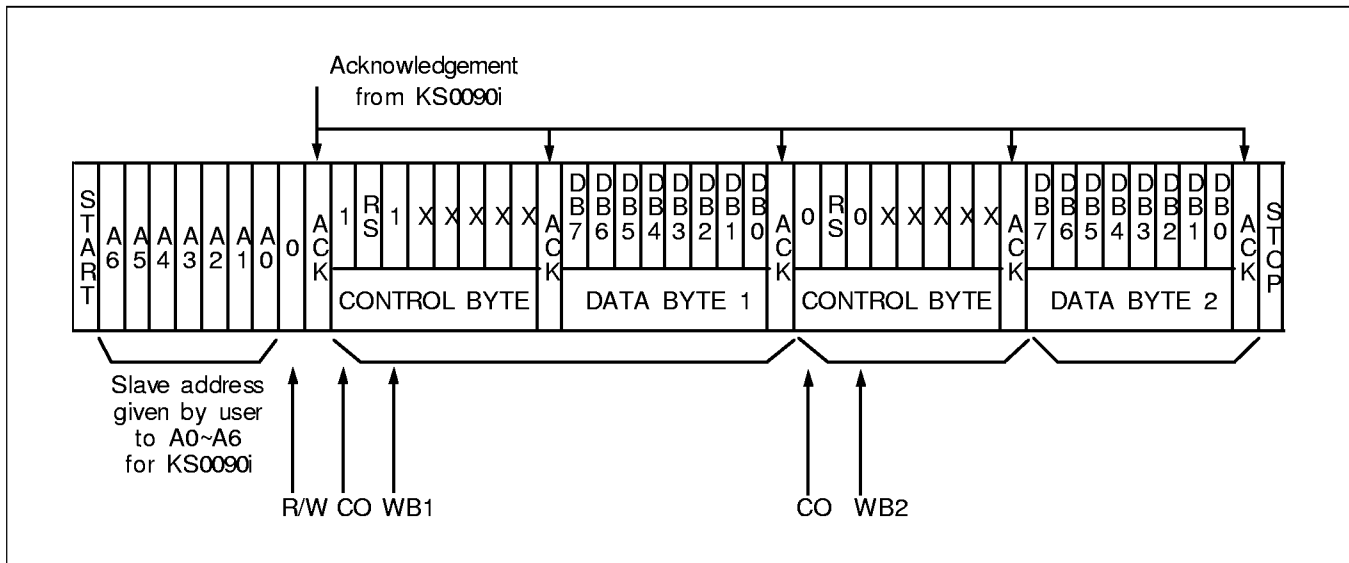
CO1: The following byte will be a data byte. After data byte, KS0090i will look upon the next 8-bit as a control byte

CO2: After this control byte, all the following bytes will be considered as a data byte before the stop procedure.

3. Unexpected read by setting R/W as 1



4. Unexpected read mode by setting WB as 1 after R/W is set as 0



WB1: The following data byte will be ignored. And I²C block makes only ACK signal.

WB2: After this, the following data bytes will be written into data register(DR) as normal operation.

S T A R T	Slave Address	0	A C K	100xxxxx Control Byte	A C K	Command Byte (Instruction)	A C K	010xxxxx Control Byte	A C K	Command Byte (Data)	A C K		Command Byte (Data)	A C K	S T O P
	Start byte			RAM address setting			Data write			Next data write continuously					

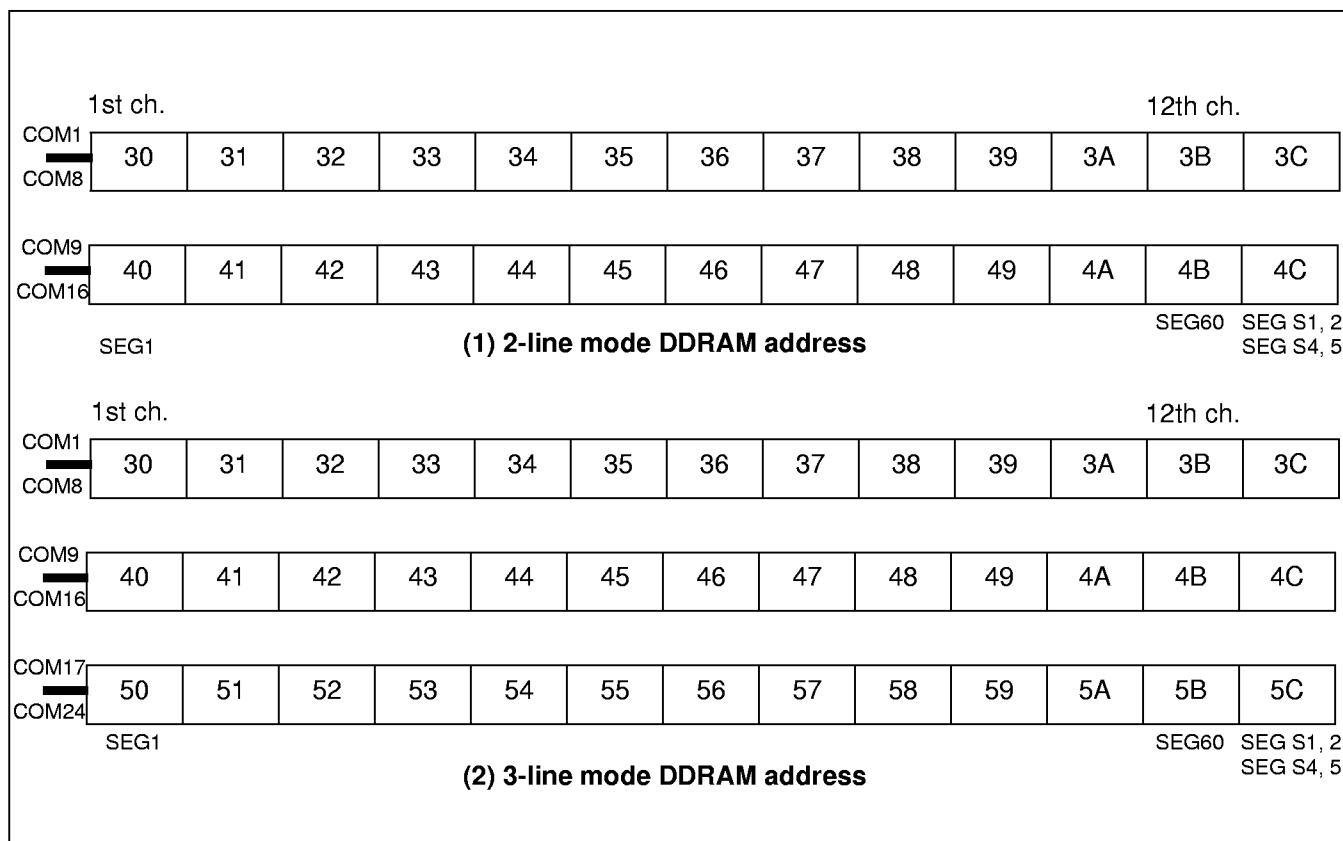
Figure 5. MPU Write Data after Set RAM Address; Write Address, Write Data

ADDRESS COUNTER (AC)

The address counter (AC) in KS0090i stores the CGRAM / DDRAM / ICONRAM address, which is transferred from IR. After writing into CGRAM / DDRAM / ICONRAM, AC is automatically increased by 1.

DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 36×8 bits (Max. 36 characters).
DDRAM address is set in the address counter (AC) as a hexadecimal number.

**Figure 6. DDRAM Address**

CHARACTER GENERATOR ROM (CGROM)

KS0090i has the character generator ROM (CGROM) consisting of up to 256 types of characters. Character size is 5×8 dots. The CG bit of the instruction table selects the 4 characters (00h to 03h) of CGROM or CGRAM. KS0090i CGROM is contact mask option ROM and compatible with customized ROM font.

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F
70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF
B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF
F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF

Figure 7. CGROM Character Code Table (F00)

CHARACTER GENERATOR RAM (CGRAM)

CGRAM contained in KS0090i enables the user to program the character pattern to display signals. When using CGRAM, the CG bit should be selected to “High”. CGRAM has up to four 5×8 -dot characters. By writing font data to CGRAM, the user defined character can be used.

Table 3. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM Data)	CGRAM Address	CGRAM Data (Character Pattern)	Pattern Number
D7 D6 D5 D4 D3 D2 D1 D0	A7 A6 A5 A4 A3 A2 A1 A0	P7 P6 P5 P4 P3 P2 P1 P0	
0 0 0 0 0 0 0 0 (00h)	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 0 0 1 1 0 0 0 0 0 1 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 1 1 0 0 0 0 0 0 1 1 1	– – – 0 1 0 1 0 – – – 1 0 1 0 1 – – – 0 1 0 1 0 – – – 1 0 1 0 1 – – – 0 1 0 1 0 – – – 1 0 1 0 1 – – – 0 1 0 1 0 – – – 1 0 1 0 1	Pattern 1
0 0 0 0 0 0 0 1 (01h)	0 0 0 0 1 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 1 0 1 0 0 0 0 0 1 0 1 1 0 0 0 0 1 1 0 0 0 0 0 0 1 1 0 1 0 0 0 0 1 1 1 0 0 0 0 0 1 1 1 1	– – – 0 0 0 0 0 0 – – – 1 1 1 1 1 1 – – – 0 0 0 0 0 0 – – – 1 1 1 1 1 1 – – – 0 0 0 0 0 0 – – – 1 1 1 1 1 1 – – – 0 0 0 0 0 0 – – – 1 1 1 1 1 1	Pattern 2
0 0 0 0 0 0 1 0 (02h)	0 0 0 1 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 1 0 0 1 0 0 0 0 1 0 0 1 1 0 0 0 1 0 1 0 0 0 0 0 1 0 1 0 1 0 0 0 1 0 1 1 0 0 0 0 1 0 1 1 1	– – – 0 1 0 1 0 – – – 0 1 0 1 0 – – – 0 1 0 1 0 – – – 0 1 0 1 0 – – – 0 1 0 1 0 – – – 0 1 0 1 0 – – – 0 1 0 1 0 – – – 0 1 0 1 0	Pattern 3
0 0 0 0 0 0 1 1 (03h)	0 0 0 1 1 0 0 0 0 0 0 1 1 0 0 1 0 0 0 1 1 0 1 0 0 0 0 1 1 0 1 1 0 0 0 1 1 1 0 0 0 0 0 1 1 1 0 1 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 1	– – – 0 1 0 1 0 – – – 0 1 0 1 0 – – – 1 0 1 0 1 – – – 1 0 1 0 1 – – – 0 1 0 1 0 – – – 0 1 0 1 0 – – – 1 0 1 0 1 – – – 1 0 1 0 1	Pattern 4

(“–”: Don't care)

SEGMENT ICON RAM (ICONRAM)

ICONRAM has segment control data and segment pattern data.

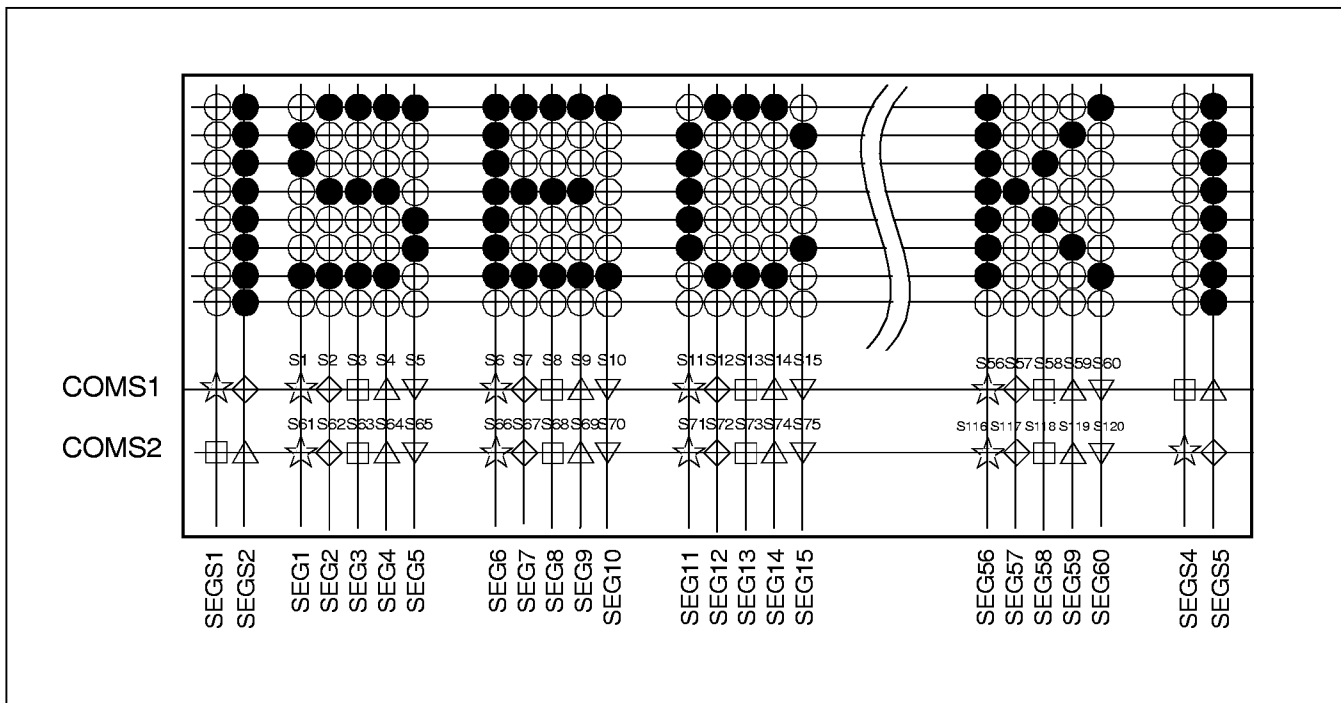


Figure 8. Relationship between ICONRAM and Icon Display

Table 4. Relationship between ICONRAM Address and Display Pattern

ICONRAM Address		ICONRAM Bits							
High Order	Low Order	D7	D6	D5	D4	D3	D2	D1	D0
6	0	—	—	—	S1	S2	S3	S4	S5
	1	—	—	—	S6	S7	S8	S9	S10
	:	:	:	:	:	:	:	:	:
	A	—	—	—	S51	S52	S53	S54	S55
	B	—	—	—	S56	S57	S58	S59	S60
	C	—	—	—	SEGS1	SEGS2	—	SEGS4	SEGS5
7	0	—	—	—	S61	S62	S63	S64	S65
	1	—	—	—	S66	S67	S68	S69	S70
	:	:	:	:	:	:	:	:	:
	A	—	—	—	S111	S112	S113	S114	S115
	B	—	—	—	S116	S117	S118	S119	S120
	C	—	—	—	SEGS1	SEGS2	—	SEGS4	SEGS5

("—": Don't care)

STATIC ICON RAM (SI)

KS0090i contains the static icon RAM to display the static icons in addition to the dynamic icons. Capacity of static icon RAM is 10 bits and is capable of displaying up to 5 icons.

The following table shows the relationship between the static icon functions, static icon RAM address and written data (Blink frequency: 1 to 2 Hz).

Table 5. Relationship between static icon RAM address and display pattern

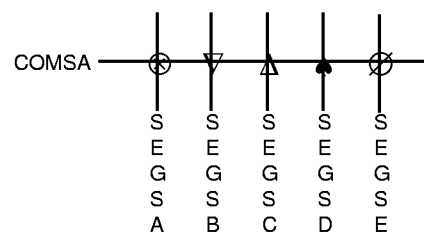
Function	RAM Address	Static Icon Data								Static Icon				
		D7	D6	D5	D4 (A)	D3 (B)	D2 (C)	D1 (D)	D0 (E)	SEGS -A	B	C	D	E
Display On/Off	20h	—	—	—	0	1	0	1	0	□	■	□	■	□
Blink On/Off	21h	—	—	—	1	1	1	0	0	■	□	■	■	□

20h = "0": Static icon off

"1": Static icon on

21h = "0": Blink off

"1": Blink on (20h data are inverted)

**SEGMENTS FOR SIGNAL DISPLAY (FS)**

When DDRAM address is 3Ch: COM1 to COM8, 1 line

4Ch: COM9 to COM16, 2 line

5Ch: COM17 to COM24, 3 line

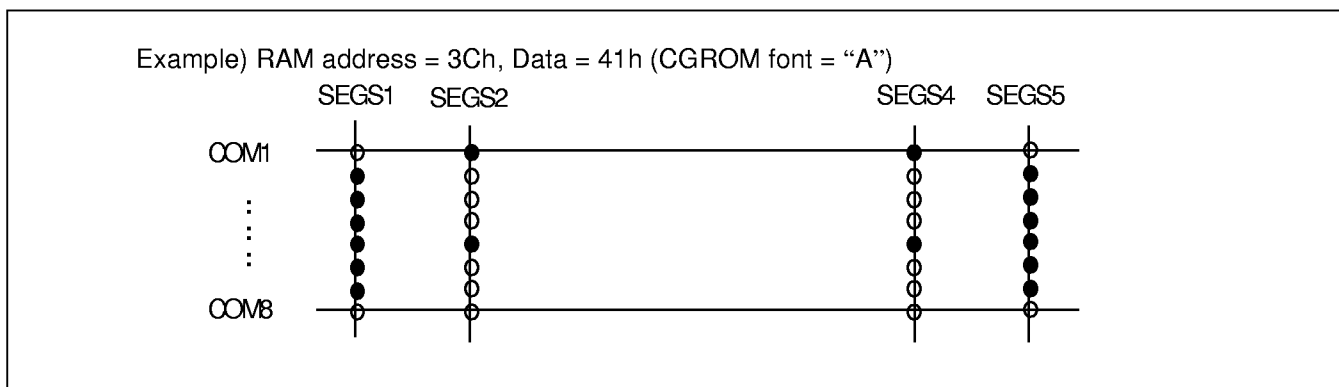
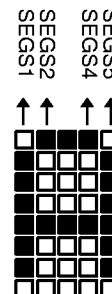
SEGS1: Font 1st bit display

SEGS2: Font 2nd bit display

SEGS4: Font 4th bit display

SEGS5: Font 5th bit display

(Font 3rd bit is not displayed.)

**Figure 9. Segment for Signal Display**

LOW POWER CONSUMPTION MODE

KS0090i provides a “standby mode” and “sleep mode” to reduce power consumption during the standby period.

Standby Mode (Power save bit on, Oscillation bit on)

The standby mode can be switched on and off by the power save command.

In the standby mode, only the static icon is displayed.

1. Liquid crystal display output

COM1 to COM24, COMS1, COMS2: V_{SS} level

SEG1 to SEG60, SEGS1, 2, 4, 5: V_{SS} level

SEGSA, B, C, D, E, COMSA: V_{DD} or V_{SS} level (Can be turned on/off by static drivers)

Use the static icon RAM for controlling the static icon display done with SEGSA, B, C, D, E, COMSA.

2. Written data in DDRAM, CGRAM, ICONRAM and registers remain at its previous value.

3. Operation mode is retained the same as it was prior to execution of the standby mode.

The internal circuit for the dynamic display output is stopped.

4. The oscillation circuit for the static display must remain “on”.

Sleep Mode (Power save on, Oscillation off)

To enter the sleep mode, the power circuit and oscillation circuit should be turned off by the power save command and power control command. This mode helps reduce power consumption by reducing current to reset level.

1. Liquid crystal display output

COM1 to COM24, COMS1, COMS2: V_{SS} level

SEG1 to SEG60, SEGS1, 2, 4, 5: V_{SS} level

SEGSA, B, C, D, E, COMSA: V_{SS} level

2. Written data in DDRAM, CGRAM, ICONRAM and registers remain at its previous value.

3. Operation mode is retained as it was prior to execution of the sleep mode.

All internal circuits are stopped.

4. Power circuit and oscillation circuit

The built-in power supply circuit and oscillation circuit are turned off by the power save command and power control command.

LCD DRIVER CIRCUIT

LCD driver circuit has 26 common and 64 segment signals for driving LCD. Data from ICONRAM/CGRAM/CGROM are transferred to 64-bit segment register serially, and then they are stored to 64-bit latch. For 2-line display mode, COM1 to COM16, COMS1, and COMS2 have 1/18 duty, and in 3-line mode, COM1 to COM 24, COMS1, and COMS2 have 1/26 duty ratio.

SEG bidirectional function is selected by the BID input pin, and COM shift direction is selected by the function set instruction “S” bit.

Table 6. SEG Data Shift Direction

BID pin	SEG Data Shift Direction
Low	SEGS1 → SEGS2 → SEG1 → → SEG60 → SEGS4 → SEGS5
High	SEGS5 → SEGS4 → SEG60 → → SEG1 → SEGS2 → SEGS1

INSTRUCTION DESCRIPTION

Table 7. Instruction Table

Instruction	Instruction Code									Description
	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Return Home	0	0	0	0	1	—	—	—	—	DDRAM address is set to “30h” from AC and cursor returns to “30h” position if shifted. The contents of DDRAM are not changed.
Display Control	0	0	0	1	1	C	B	—	D	Cursor/blink /display on/off C = 0: cursor off (default), C = 1: cursor on B = 0: blink off (default), B = 1: blink on D = 0: display off (default), D = 1: display on
Power Save	0	0	1	0	0	—	—	OS	PS	Power save/oscillation circuit. OS = 0: oscillator off (default), OS = 1: oscillator on PS = 0: power save off (default), PS = 1: power save on
Power Control	0	0	1	0	1	0	VR	VF	VC	LCD power control VR = 0: voltage regulator off (default), 1: voltage regulator on VF = 0: voltage follower off (default), 1: voltage follower on VC = 0: voltage converter off (default), 1: voltage converter on
Function Set	0	0	1	1	0	N2	N1	S	CG	Display line mode. N2, N1 = 0, 0: 2 line display mode (default), 0, 1: 3 line display mode Set shifting direction of COM S = 0: COM left shift (COM1 → COM24) (default), 1: COM right shift (COM24 → COM1) Select CGRAM or CGROM CG = 0: use CGROM (default), 1: use CGRAM
RAM Address Set	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	DDRAM/CGRAM/ICONRAM or register address.
Write Data	1	D7	D6	D5	D4	D3	D2	D1	D0	Write DDRAM/CGRAM/ICONRAM or register data.
EV Mode	0	0	0	0	0	0	0	0	EV	Electronic volume step EV = 0: 32 contrast-step (default), 1: 64 contrast-step
Test Mode	0	0	0	0	0	*	*	*	*	Instruction for IC chip test. Don't use this instruction.

NOTES:

(“—”: Don't Care, “*”: Don't Use)

- For the NOP instruction,
when EV mode is “0” (32 contrast-step), the NOP instruction set is (000000000), and
when EV mode is “1” (64 contrast-step), the NOP instruction set is (000000001).
- Instruction execution time depends on the internal process time of KS0090i, therefore it is necessary to provide a time larger than one MPU interface cycle time (tc) between execution of two successive instructions.

RETURN HOME

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	-	-	-	-

(“-”: Don't Care)

Return home instruction field makes the cursor return home.

DDRAM address is set to “30h” into the address counter. Return cursor to first digit of the first line. The contents of DDRAM are not changed.

DISPLAY CONTROL

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	C	B	-	D

(“-”: Don't Care)

Display control instruction field controls cursor / blink / display on / off.

C Cursor on / off control bit

H	Cursor is turned on.
L	Cursor is disappeared in current display and can't blink (default).

B Cursor blink on / off control bit

H	When C = “H”, KS0090i makes LCD alternate between inverting display character and normal display character at the cursor position with about a half second. On the contrary, if C = “Low”, only a normal character is displayed regardless of the B flag.
L	Blink is off (default).

D Display on / off control bit

H	Display is turned on
L	Display is turned off, but display data remain in DDRAM (default).

NOTE: Static icons driven by COMSA and SEGSA/B/C/D/E must be controlled by the static icon RAM.

POWER SAVE

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	-	-	OS	PS

(“-”: Don't Care)

Power save instruction field is used to control the oscillator and power save mode.

OS**Oscillator on / off control bit**

H	Oscillator is turned on.
L	Oscillator is turned off (default).

PS**Power save on / off control bit**

H	Power save mode is turned on.
L	Power save mode is turned off. (default)

POWER CONTROL

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	VR	VF	VC

Power control instruction field sets voltage regulator / follower / converter on / off.

VR**Voltage regulator circuit control bit**

H	Voltage regulator is turned on.
L	Voltage regulator is turned off (default).

VF**Voltage follower circuit control bit**

H	Voltage follower is turned on.
L	Voltage follower is turned off (default).

VC**Voltage converter circuit control bit**

H	Voltage converter is turned on.
L	Voltage converter is turned off (default).

NOTE: The oscillator circuit must be turned on for the voltage converter circuit to be active.

FUNCTION SET

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	N2	N1	S	CG

N2, N1

Display line mode instruction field selects 2-line or 3-line display mode

L	L	2-Line display mode (default)
L	H	3-Line display mode

S

Data shift direction of common

H	COM right shift (default)
L	COM left shift

Table 8. COM Data Shift Direction

Line Mode	S	COM Data Shift Direction
2 Line Mode	0 (Left)	COM1 → → COM15 → COM16 → COMS1 → COMS2 → COM1
	1 (Right)	COM16 → COM15 → → COM1 → COMS1 → COMS2 → COM16
3 Line Mode	0 (Left)	COM1 → → COM23 → COM24 → COMS1 → COMS2 → COM1
	1 (Right)	COM24 → COM23 → → COM1 → COMS1 → COMS2 → COM24

CG

CGRAM enable bit

H	CGRAM can be accessed and you can use this RAM as a four special character area. (00h – 03h = CGRAM font display)
L	CGRAM is disabled. CGROM (00h to 03h) can be accessed and the additional current consumption is saved by using this mode (default). (00h – 03h = CGROM font display)

RAM ADDRESS SET

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

RAM address set instruction field sets CGRAM / DDRAM / ICONRAM or register address.
 Each RAM is distinguished by a RAM address.
 Before writing data into the RAM, set the address by RAM address set instruction.
 Next, when data are written in succession, the address is automatically increased by 1.

Table 9. RAM Address Mapping

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00h	CGRAM (00h)									CGRAM (01h)						
10h	CGRAM (02h)									CGRAM (03h)						
20h	SI		Unused							EV	TE	Unused				
30h	DDRAM line 1 (30h to 3Bh)												FS		Unused	
40h	DDRAM line 2 (40h to 4Bh)												FS			
50h	DDRAM line 3 (50h to 5Bh)												FS			
60h	ICONRAM COMS1 Icon (60h – 6Ch)													Unused		
70h	ICONRAM COMS2 Icon (70h – 7Ch)															

NOTE:

SI: Static icon register (20h, 21h). It is used for SEGs/B/C/D/E

EV: Electronic volume register (28h)

TE: Test register (29h) (Do not use.)

FS: For signals: 1 line (3Ch), 2 line (4Ch), 3 line (5Ch). It is used for SEGs1/2/4/5.

WRITE DATA

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	D7	D6	D5	D4	D3	D2	D1	D0

This instruction field makes KS0090i write binary 8-bit data to DDRAM / CGRAM / ICONRAM or register. The RAM address to be written into is determined by the previous RAM Address Set instruction. After writing operation, the address is automatically increased by 1.

EV MODE

RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	EV

This instruction field selects between 2 electronic volume steps: 32 and 64 contrast-step.

When the EV = “Low”, KS0090i selects 32 contrast-step (default), and when

Electronic volume register (28h)=

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
-	-	-	C4	C3	C2	C1	C0

When the EV = “High”, KS0090i selects 64 contrast-step. (“-”: Don’t Care)

Electronic volume register (28h)=

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
-	-	C5	C4	C3	C2	C1	C0

(“-”: Don’t Care)

INITIALIZING & POWER SAVE MODE SETUP

HARDWARE RESET

After reset by RES pin, KS0090i can be initialized the following state.

1. Control Display on/off instruction

C=0: Cursor off
B=0: Blink off
D=0: Display off

2. Power Save Set instruction

OS=0: Oscillator off
PS=0: Power save off

3. Power Control Set instruction

VR=0: Voltage regulator off
VF=0: Voltage follower off
VC=0: Voltage converter off

4. Function Set instruction

N2=0, N1=0: 2 line display mode
S=0: COM left shift
CG=0: CGRAM is not used

5. Return Home

Address counter = 30h

6. Static icon RAM & electronic contrast control register

Static icon RAM: 20h = (0, 0, 0, 0, 0), static icon off
21h = (0, 0, 0, 0, 0), blink off
EV = 0: 32 contrast-step
Electronic contrast control register: 28h = ((0),0, 0, 0, 0, 0), contrast high

NOTE: If initialization is not done by the RES pin at application, an unknown condition may result, in which case you can initialize by instruction.

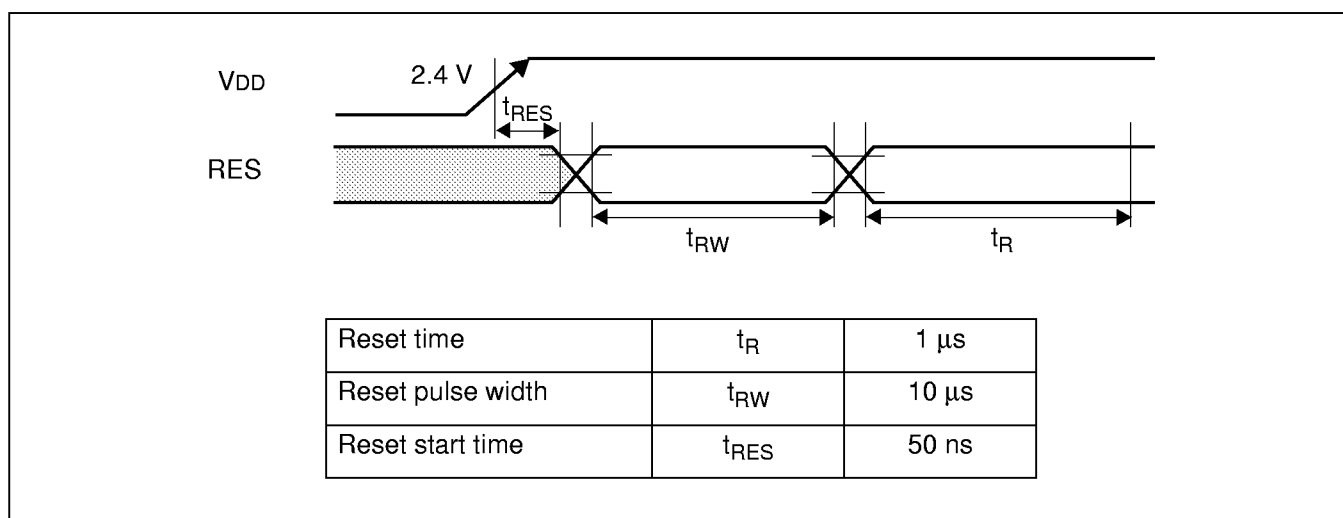
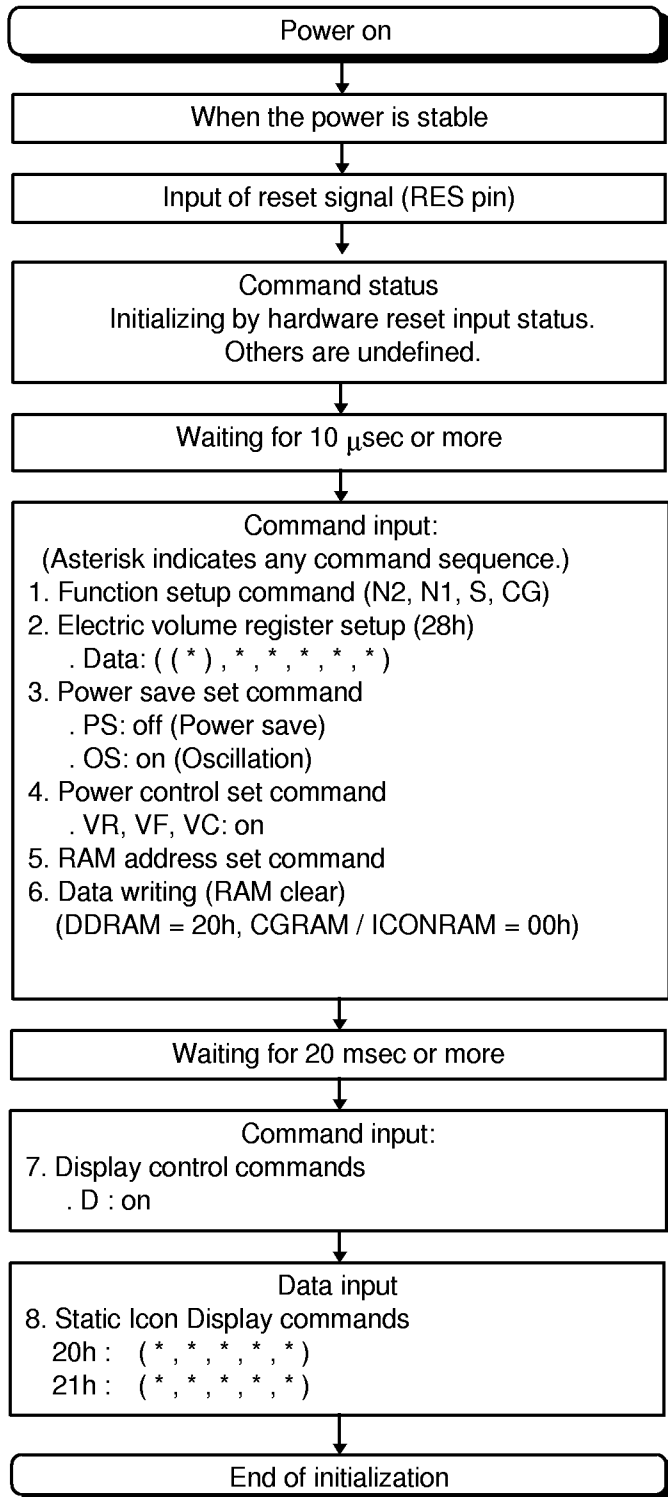


Figure 10. RESET Timing

INITIALIZING AND POWER SAVE MODE SETUP

Initializing by Instruction



NOTES:

At command (5) and (6), the internal RAM should be cleared.

To clear DDRAM and FS (segment for signal)

- Set address at 30h (first DDRAM) and then write 20h (space character code) 13 times
- Set address at 40h and write 20h for 13 times
- Set address at 50h and write 20h for 13 times

To clear CGRAM,

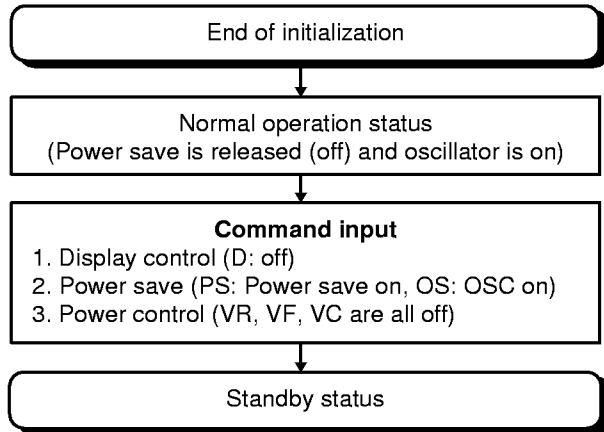
- Set address at 00h (first CGRAM) and then write 00h (null data) 32 times

To clear ICONRAM,

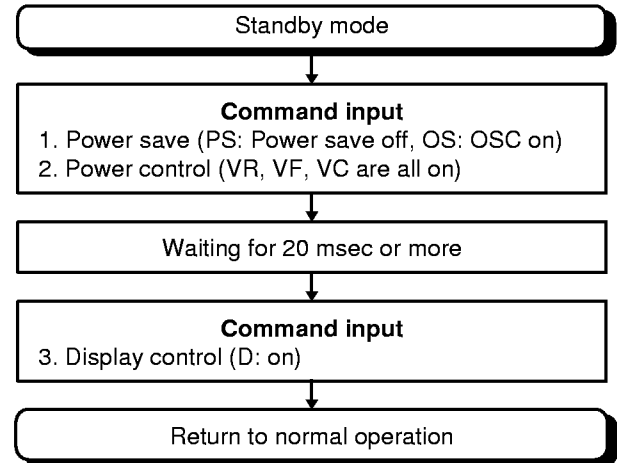
- Set address at 60h (first ICONRAM) and then write 00h (null data) 13 times
- Set address at 70h and write 00h for 13 times

Standby Mode Set or Release by Instruction

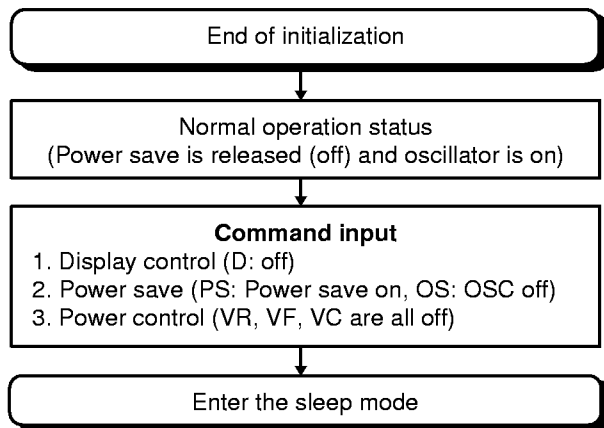
(a) Standby mode set



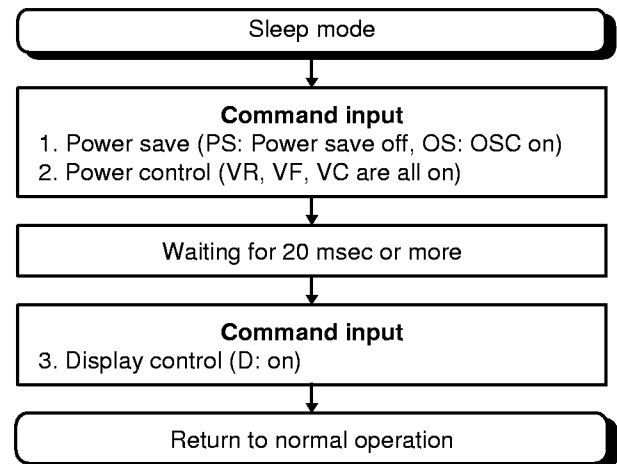
(b) Standby mode release

**Sleep Mode Set or Release by Instruction**

(a) Sleep mode set



(b) Sleep mode release



LCD DRIVING POWER SUPPLY CIRCUIT

The power supply circuit produces LCD panel driving voltage at low power consumption. The LCD driving power supply circuit consists of voltage converter (2 times or 3 times), voltage regulator, and voltage follower. It is controlled by power control instruction. Table 10. shows how the LCD driving power supply circuit works by power control instruction sets.

Table 10. Power Supply Control Mode Set

VR	VF	VC	Voltage Regulator	Voltage Follower	Voltage Converter	VOUT Pin	VR Pin	V0, V1, V2, V3, V4 Pin
1	1	1	Enable	Enable	Enable	Internal voltage output	Used for voltage adjustment	Internal voltage output
1	1	0	Enable	Enable	Disable	External voltage input	Used for voltage adjustment	Internal voltage output
0	1	0	Disable	Enable	Disable	Open	Open	V1 – V4: Internal voltage output V0: External voltage input
0	0	0	Disable	Disable	Disable	Open	Open	V0 – V4: External voltage input

NOTE: Any other case which is not written in this table is prohibited.

VOLTAGE CONVERTER

If capacitors are connected between CAP1+ and CAP1-, CAP2+ and CAP2-, VDD and VOUT, VDD- VSS voltage is positively tripled and generated at VOUT terminal. When the voltage is doubled, open CAP2- and connect CAP2+ to VOUT terminal.

This boosted voltage is used in the built-in voltage regulator circuit.

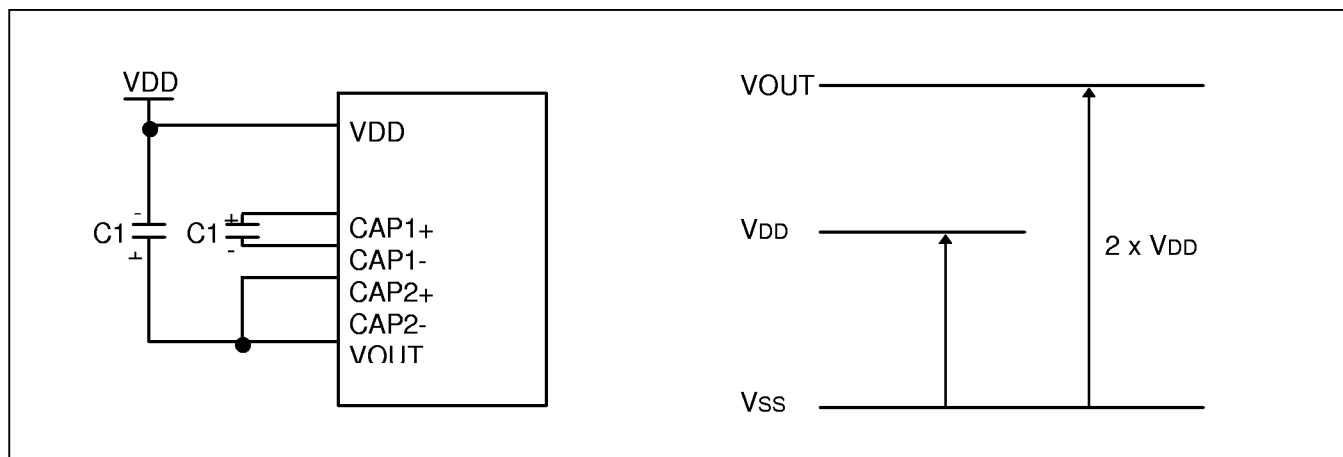


Figure 11. Two Times Boosting

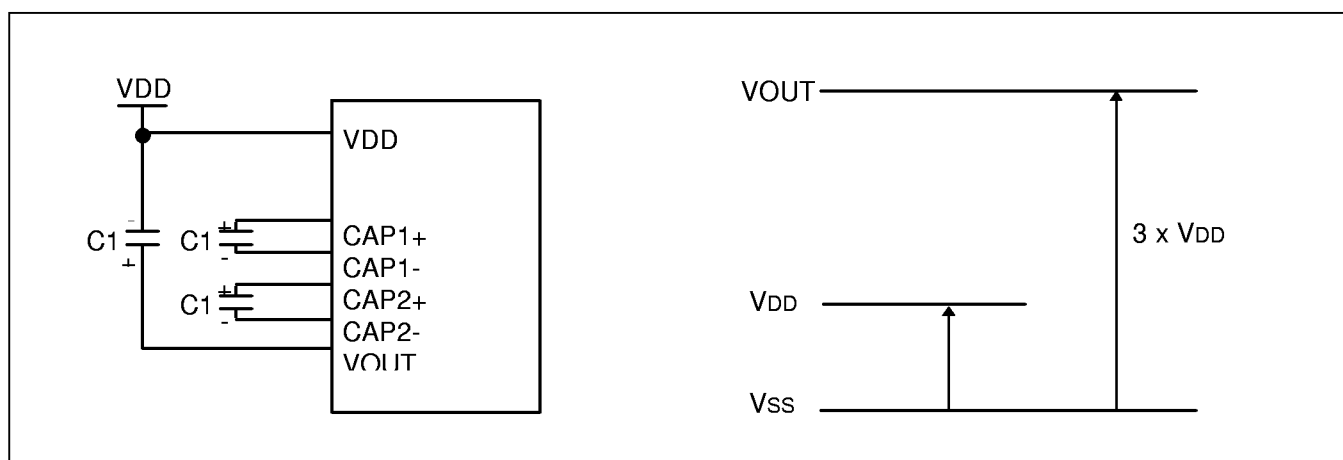


Figure 12. Three Times Boosting

VOLTAGE REGULATOR

The voltage regulator circuit is used to obtain an appropriate LCD panel driving voltage. This voltage is obtained by adjusting resistors R_a and R_b as shown in equation (1), and by setting electronic contrast control data bits. See equation (2) or (3).

The potential of V_0 pin can be adjusted within V_{REF} to V_{OUT} . V_{REF} is the internal constant voltage source of the chip and this value is 2.0V in the condition $V_{DD} \geq 2.4V$.

Voltage regulation by adjusting resistors R_a , R_b

$$V_0 = \left(1 + \frac{R_b}{R_a}\right) \times V_{REF} \quad \text{..... (1)}$$

The internal V_{REF} of voltage regulator has the temperature compensation function, and the temperature coefficient is approximately $-0.05\%/^{\circ}C$ at range $-20^{\circ}C$ to $+50^{\circ}C$.

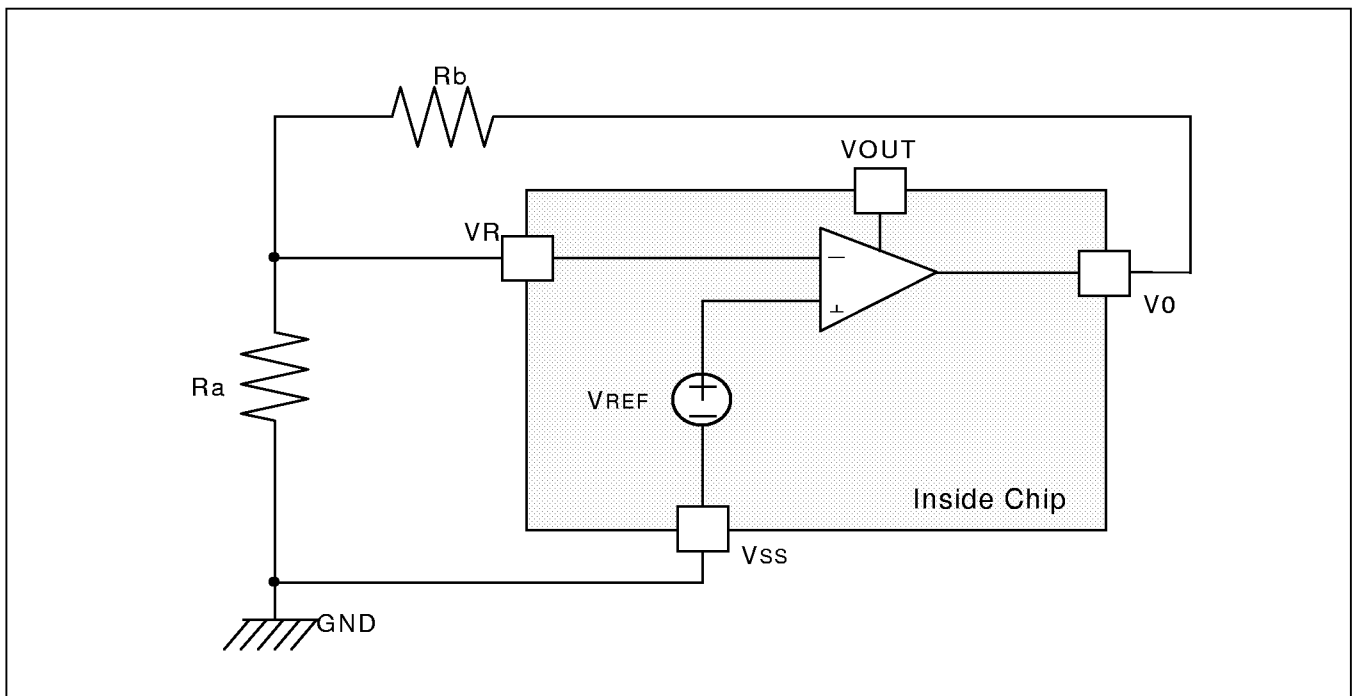


Figure 13. Voltage Regulator Circuit

ELECTRONIC CONTRAST CONTROL (EV=0, 32 STEPS)

For 32 contrast-step, EV flag of EV set mode instruction field should be set to “Low”. Then, electronic contrast control data bits 28h = (C4, C3, C2, C1, C0) can be valid. Voltage regulation is adjusted as 32-contrast step according to the value of Electronic Contrast Control data bits. LCD drive voltage V0 has one of 32 voltage values if 5-bit data is set to the electronic contrast control register (RAM address 28h). When using the electronic contrast control function, you need to turn on the voltage regulator using power control instruction.

$$V_0 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV} \quad \text{..... (2)}$$

$$V_{EV} = V_{REF} - n\alpha \quad (n = 0, 1, 2, \dots, 30, 31)$$

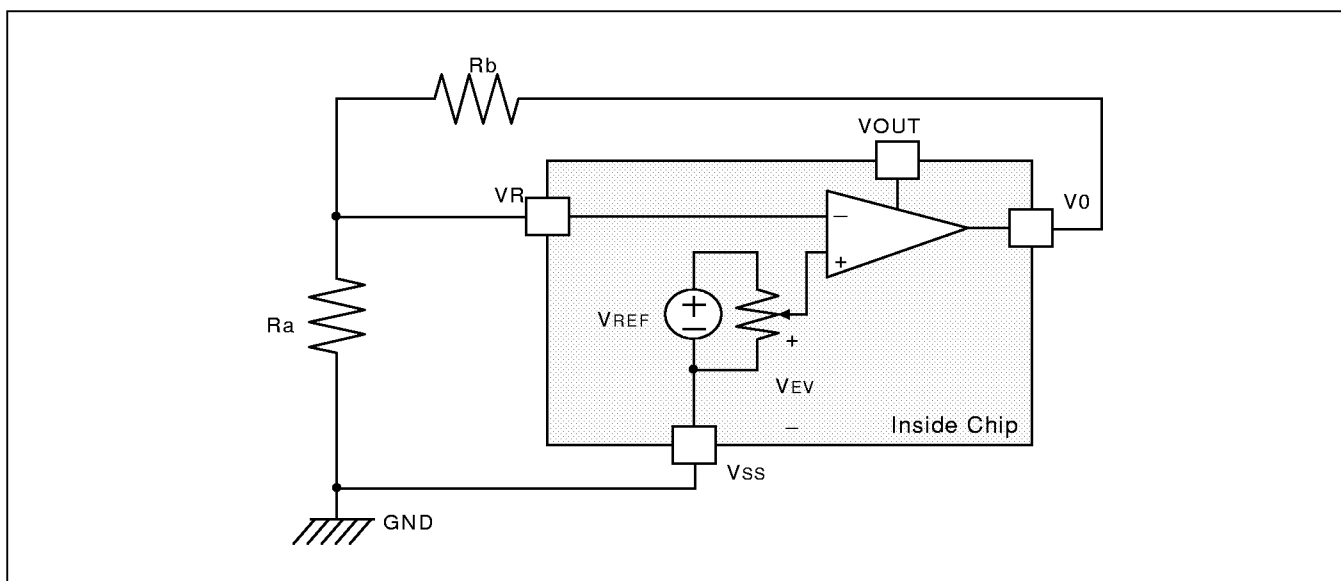
$$\alpha = V_{REF} / 150$$

For example $R_a = 1 \text{ M}\Omega$, $R_b = 2 \text{ M}\Omega$, $n = 0$ then $V_0 = 6 \text{ V}$

Table 11. Electronic Contrast Control Register (32 Steps)

No.	C7	C6	C5	C4	C3	C2	C1	C0	$n\alpha$	V0	Contrast
0	—	—	—	0	0	0	0	0	0 (default)	Maximum	High
1	—	—	—	0	0	0	0	1	1α	:	:
2	—	—	—	0	0	0	1	0	2α	:	:
3	—	—	—	0	0	0	1	1	3α	:	:
:	:	:	:	:	:	:	:	:	:	:	:
30	—	—	—	1	1	1	1	0	30α	:	:
31	—	—	—	1	1	1	1	1	31α	Minimum	Low

(“—”: Don’t Care)

**Figure 14. Electronic Contrast Control Circuit**

ELECTRONIC CONTRAST CONTROL (EV=1, 64 STEPS)

For 64 contrast-step, EV flag of EV set mode instruction field should be set to “High”. After this, electronic contrast control data bits 28h = (C5, C4, C3, C2, C1, C0) can be valid. Voltage regulation is adjusted as 64-contrast step according to the value of Electronic Contrast Control data bits. LCD drive voltage V0 has one of 64 voltage values if 6-bit data is set to the electronic contrast control register (RAM address 28h). When using the electronic contrast control function, you must turn on the voltage regulator using power control instruction.

$$V_0 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV} \quad \text{..... (3)}$$

$$V_{EV} = V_{REF} - n\alpha \quad (n = 0, 1, 2, \dots, 62, 63)$$

$$\alpha = V_{REF} / 300$$

Table 12. Electronic Contrast Control Register (64 Steps)

No.	C7	C6	C5	C4	C3	C2	C1	C0	nα	V0	Contrast
0	—	—	0	0	0	0	0	0	0 (default)	Maximum	High
1	—	—	0	0	0	0	0	1	1 α	:	:
2	—	—	0	0	0	0	1	0	2 α	:	:
3	—	—	0	0	0	0	1	1	3 α	:	:
:	:	:	:	:	:	:	:	:	:	:	:
62	—	—	1	1	1	1	1	0	62 α	:	:
63	—	—	1	1	1	1	1	1	63 α	Minimum	Low

(“—”: Don’t Care)

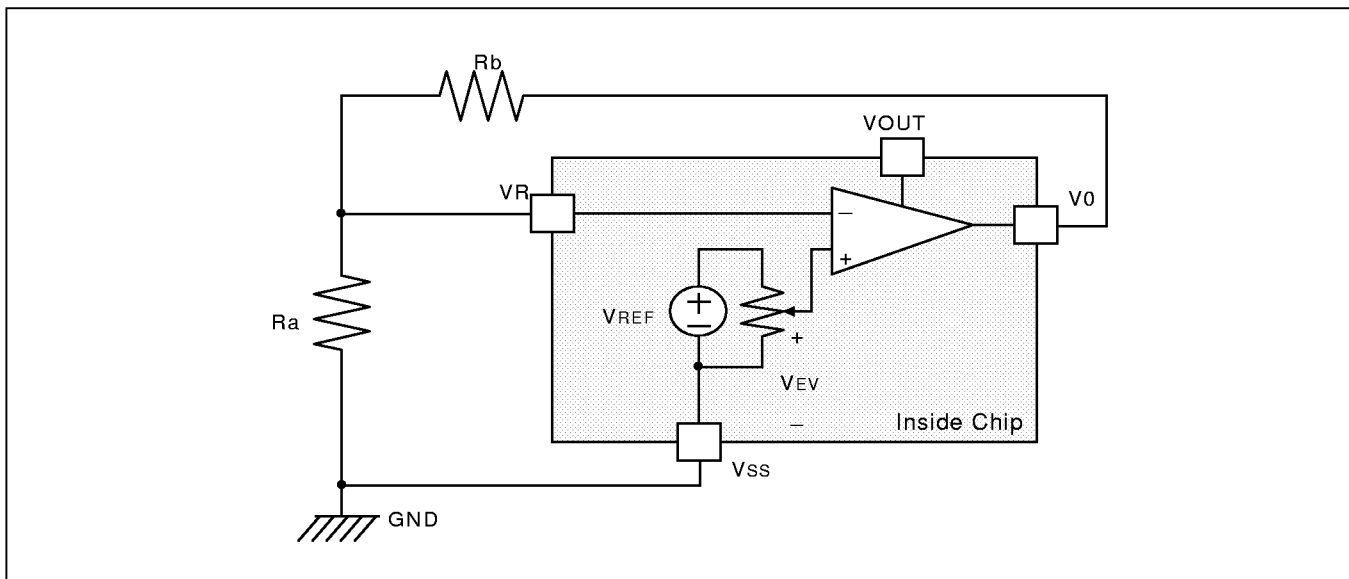


Figure 15. Electronic Contrast Control Circuit

VOLTAGE GENERATOR CIRCUIT

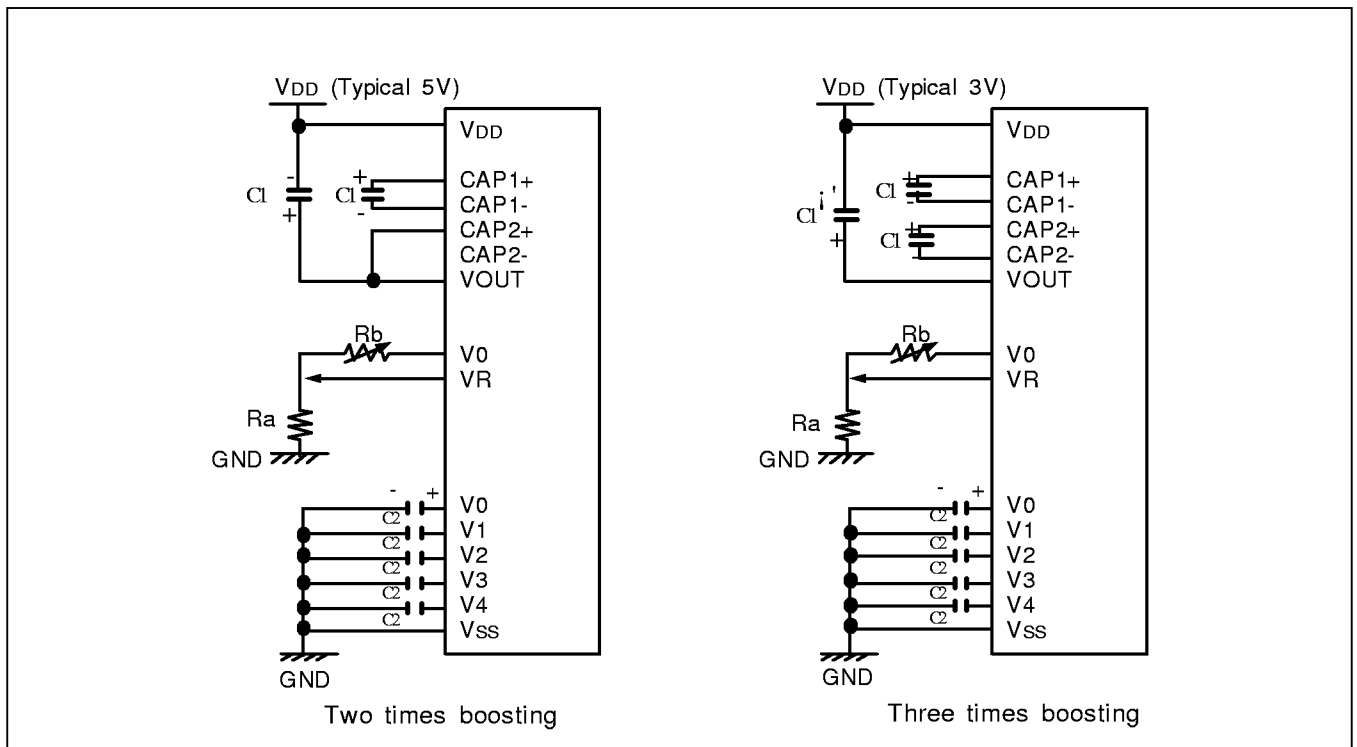
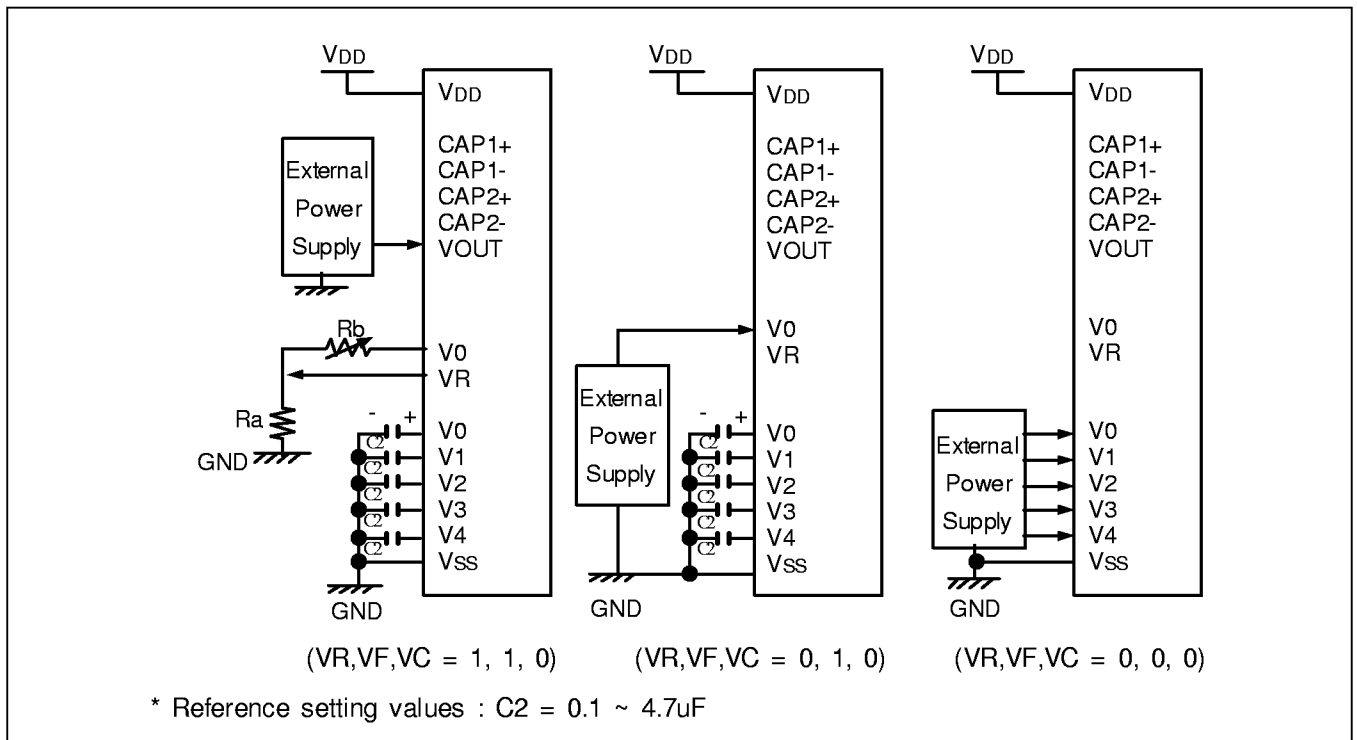
Figure 16. When Built-in Power Supply is Used ($VR, VF, VC = 1, 1, 1$)

Figure 17. When External Power Supply is Used

MPU INTERFACE

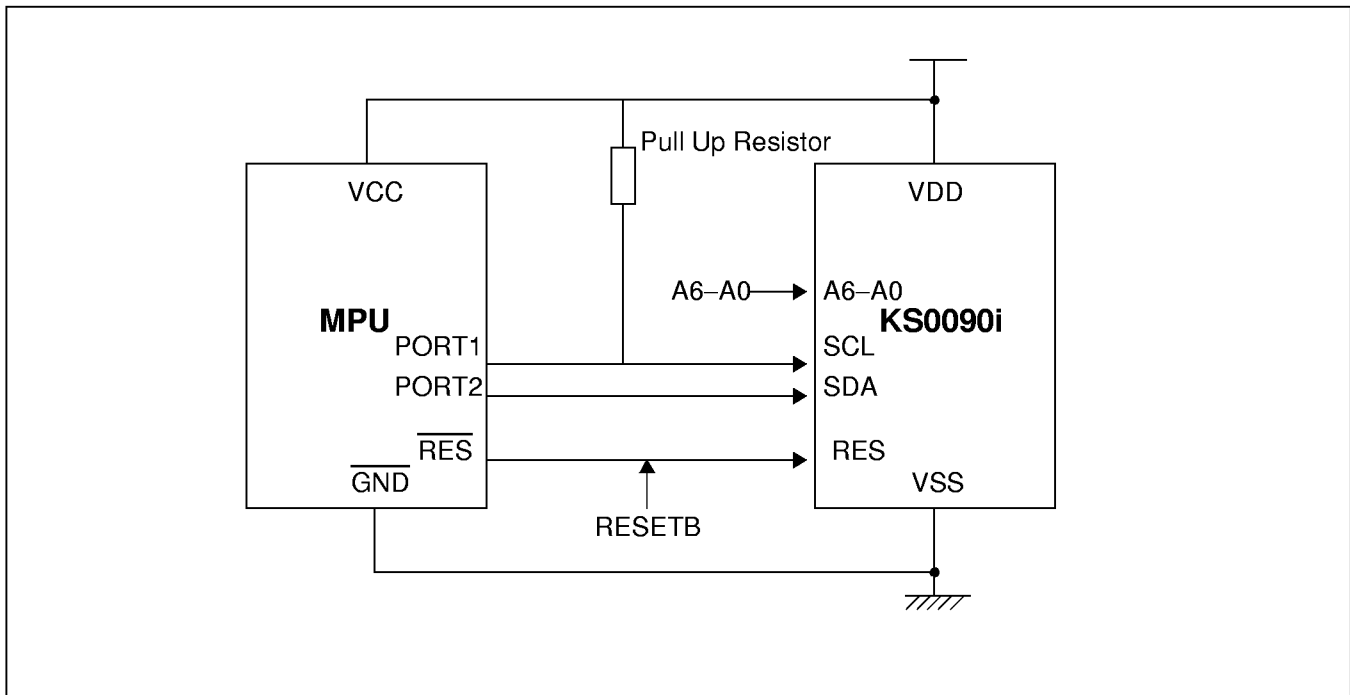


Figure 18. I²C Serial Interfacing with Any Microprocessors.

Example of I²C operation: 2 line display

Step	Operation	Display	I²C Byte
1	Reset by using RES pin		KS0090i reset
2	I²C start		I²C initialized. No display appears.
3	Acknowledge (During the acknowledge cycle SDA will be pulled-down by the KS0090i)		Slave address for write A6 A5 A4 A3 A2 A1 A0 R/W Ack A6 A5 A4 A3 A2 A1 A0 0 0
4	Send a control byte for function set (Control byte sets RS High for instruction)		C0 RS WB Ack 1 0 0 × × × × × 0
5	Function set (2-line display, COM left shift and don't use CGRAM)		DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 1 0 0 0 0 0 0
6	Send a control byte for function set (Control byte sets RS High for instruction)		C0 RS WB Ack 1 0 0 × × × × × 0
7	Address set (for EV register (28H))		DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 1 0 1 0 1 0 0 0 0
8	Send a control byte for write data (Control byte sets RS High for EV register)		C0 RS WB Ack 1 1 0 × × × × × 0
9	Set EV register to DB0–DB7		DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0

10	Send a control byte for power save set (Control byte sets RS Low for instruction)		C0 RS WB 0 0 0 × × × × × 0	Ack
11	Power save set (OS: On , PS: off)		DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 × × 1 0	Ack 0
12	Power control set (VR, VF, VC: On)		DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 × × 1 0	Ack 0
13	RAM address set (ADDR = 30H)		DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 × × 1 0	Ack 0
14	I ² C start		For writing data to DDRAM (RAM Clear: DDRAM=20H) Therefore a control byte is needed.	
15	Slave address for write (During the acknowledge cycle SDA will be pulled-down by the KS0090i)		Slave address for write A6 A5 A4 A3 A2 A1 A0 R/W A6 A5 A4 A3 A2 A1 A0 0	Ack 0
16	Send a control byte for write data (Control byte sets RS High for RAM Clear)		C0 RS WB 0 1 0 × × × × × 0	Ack 0
17	Write null character to DDRAM (ADDR=30H, DB[7:0]=20H)		DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 0 0 0 0 0	Ack 0
18	Repeat 32 times of step 16 for 2-line RAM data			
19	I ² C start		For writing display instruction, a control byte is needed.	
20	Slave address for write (During the acknowledge cycle SDA will be pulled-down by the KS0090i)		Slave address for write A6 A5 A4 A3 A2 A1 A0 R/W A6 A5 A4 A3 A2 A1 A0 0	Ack 0
21	Send a control byte for write instruction (Control byte sets RS Low for display instruction)		C0 RS WB 1 0 0 × × × × × 0	Ack 0
22	Return Home		DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 1 0 0 0 0 0	Ack 0
23	Send a control byte for write instruction (Control byte sets RS Low for display instruction)		C0 RS WB 1 0 0 × × × × × 0	Ack 0
24	Display Control	–	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 1 1 1 1 × 1	Ack 0
25	Send a control byte for write data (Control byte sets RS High for display instruction)	–	C0 RS WB 1 1 0 × × × × × 0	Ack 0
26	Write data A	A_	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 1 0 0 0 0 0 1	Ack 0
27	I ² C stop	A_		

APPLICATION INFORMATION FOR LCD PANEL

CHIP BOTTOM AND LOWER VIEW (S (COM) = "0", BID (SEG) = "0")

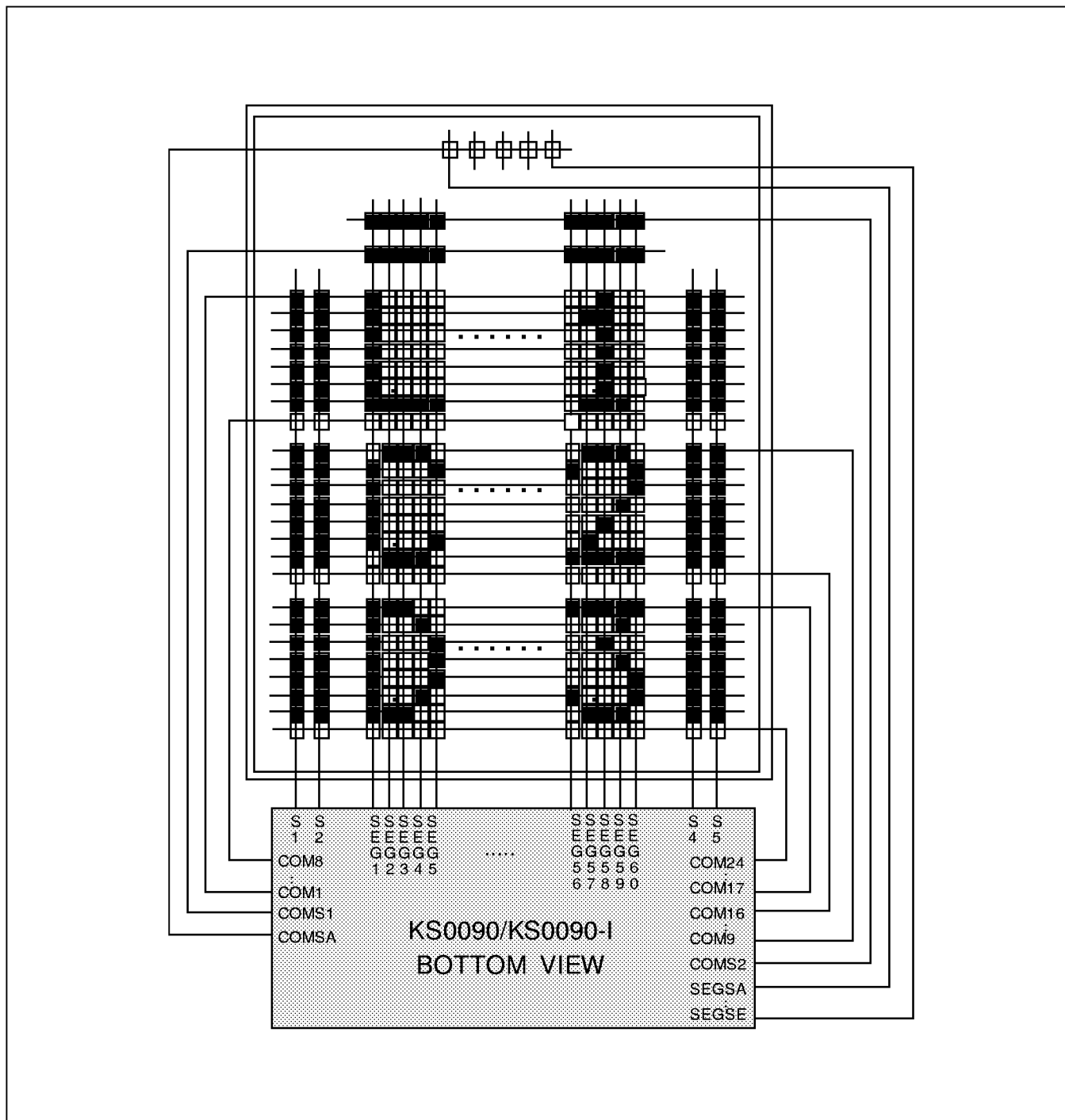


Figure 19.

CHIP BOTTOM & UPPER VIEW (S (COM) = "1", BID (SEG) = "1")

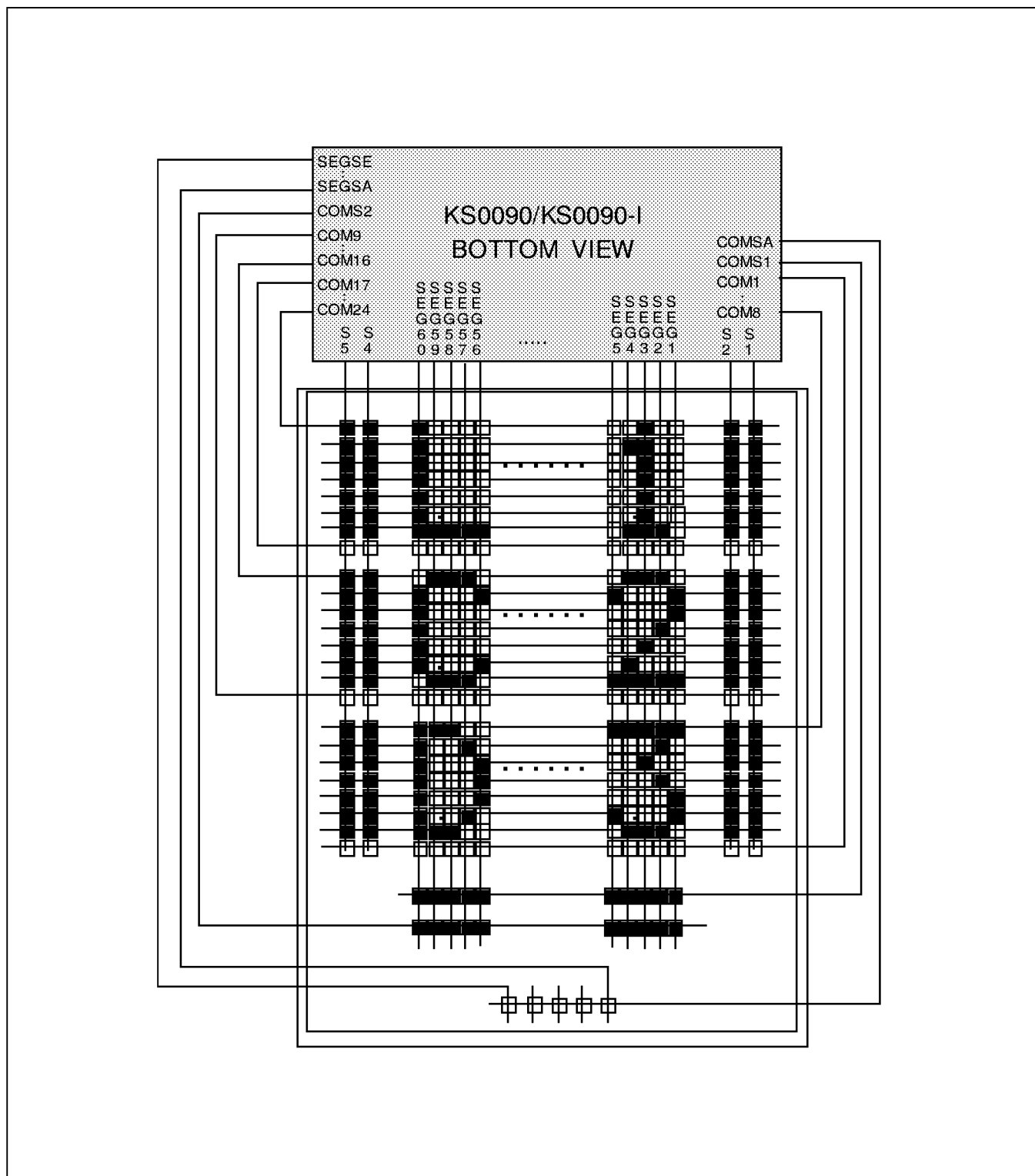


Figure 20.

CHIP TOP & LOWER VIEW (S (COM) = "0", BID (SEG) = "1")

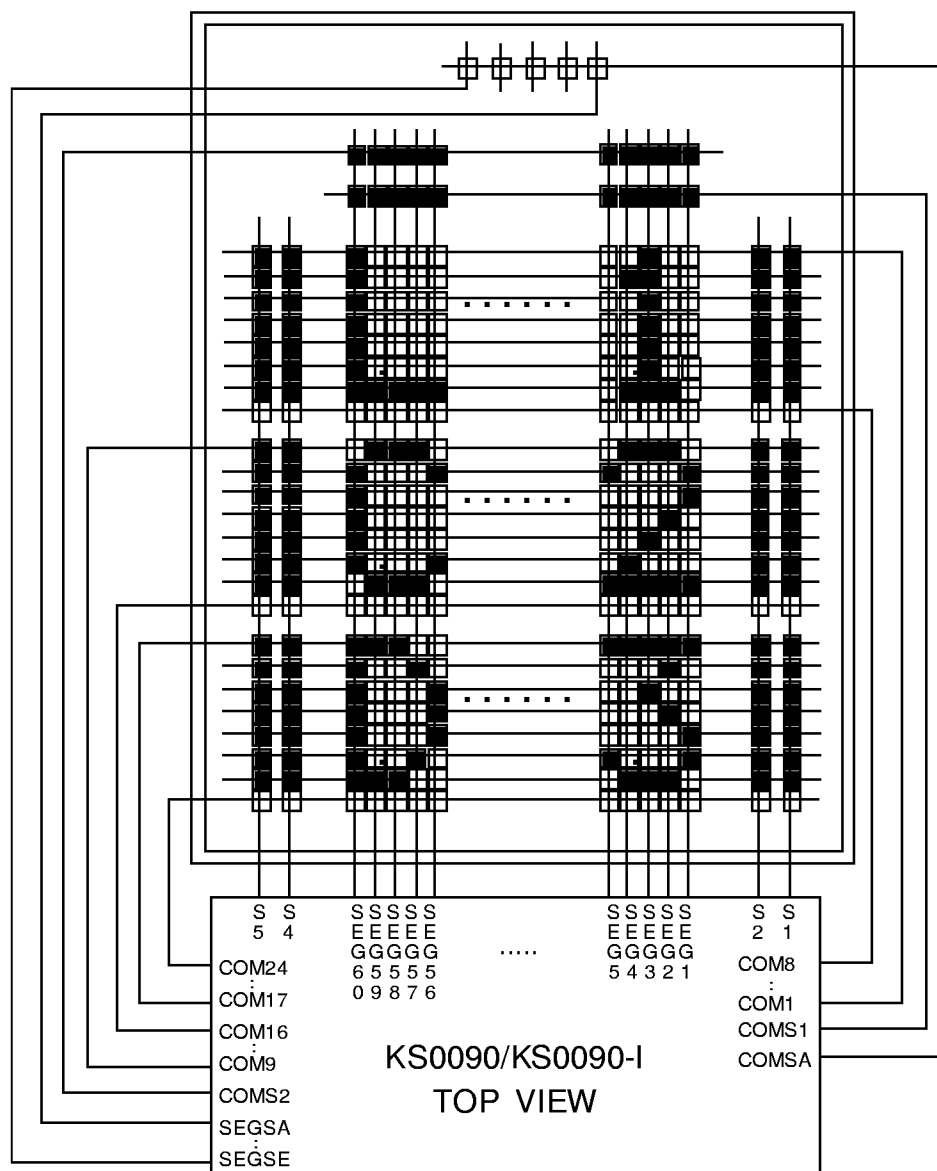


Figure 21.

CHIP TOP & UPPER VIEW (S (COM) = "1", BID (SEG) = "0")

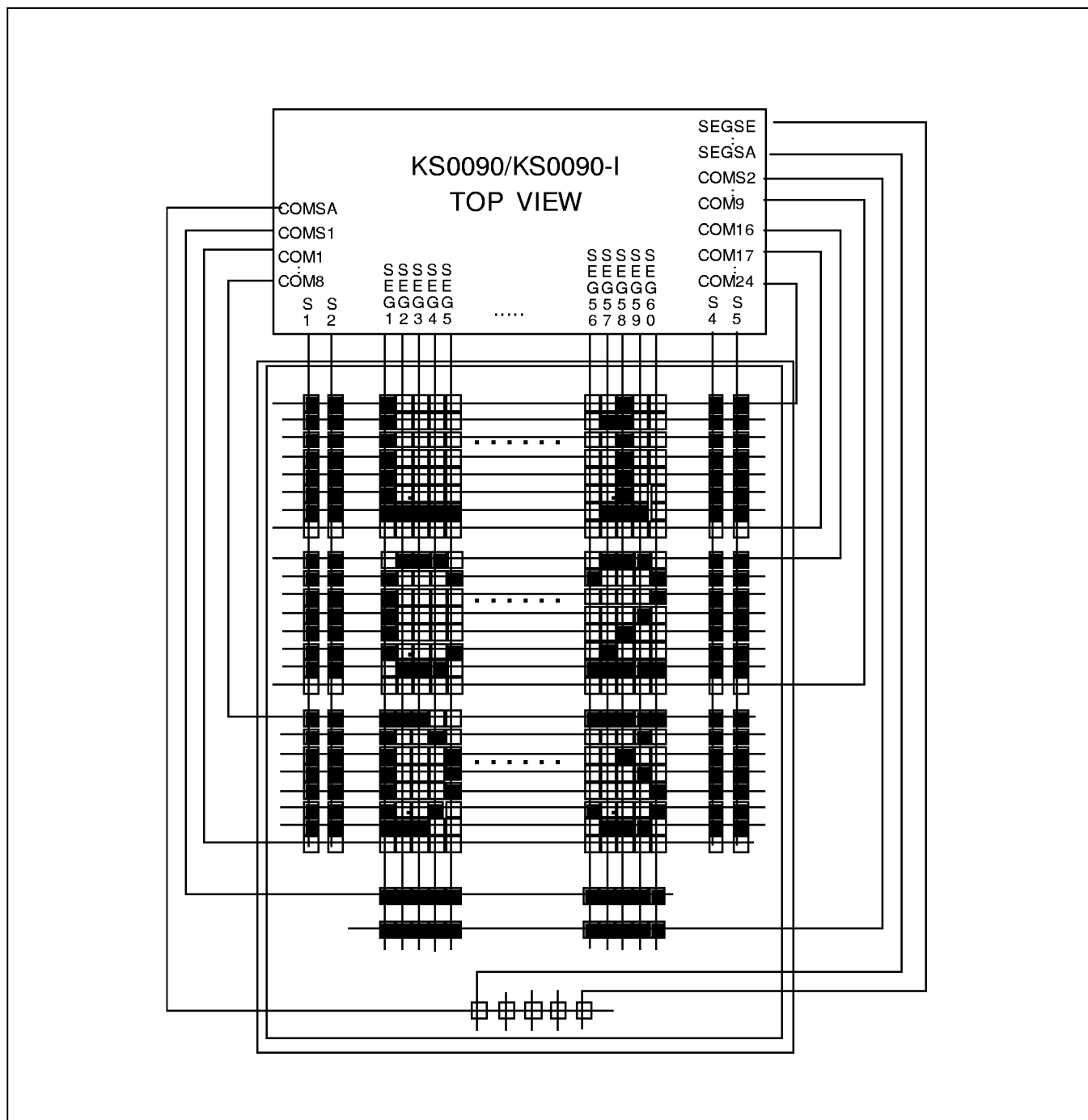
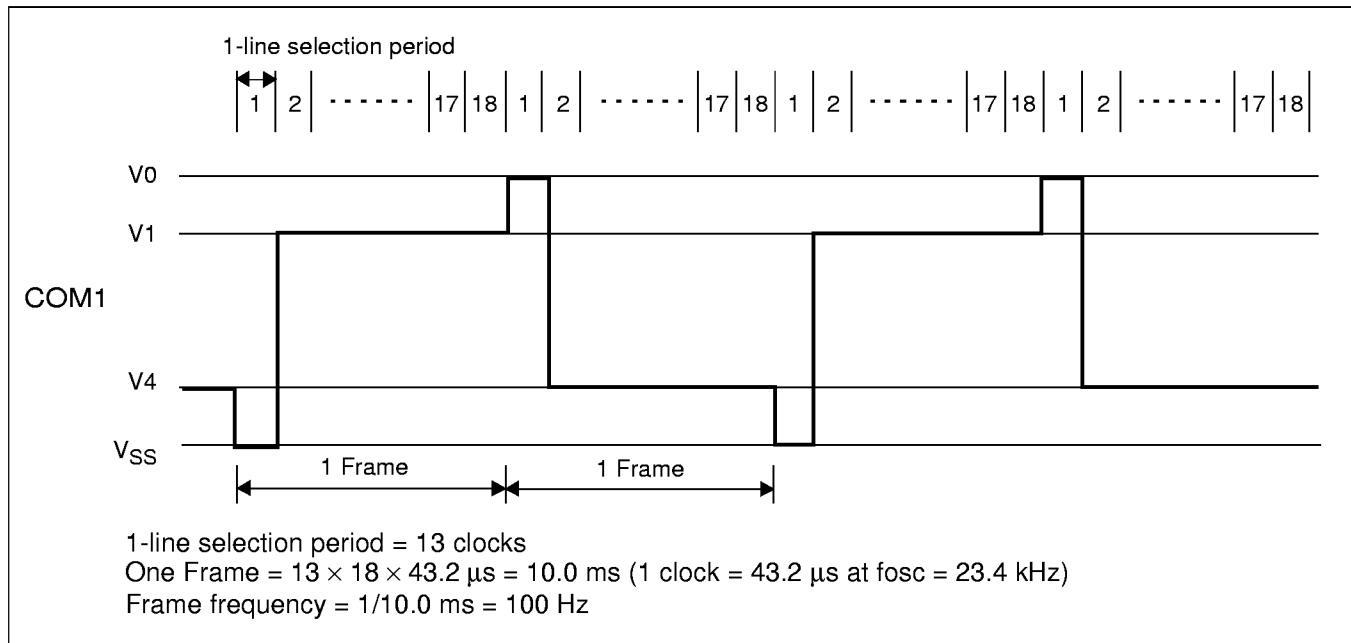


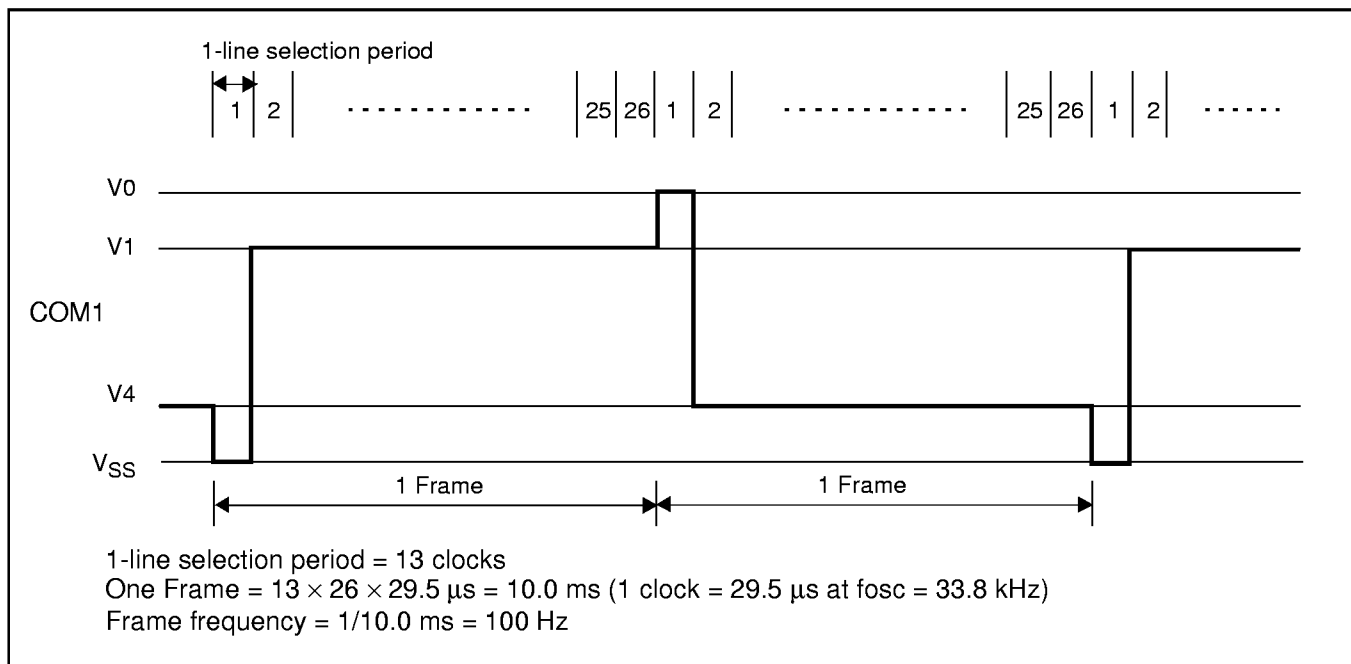
Figure 22.

FRAME FREQUENCY

1/18 DUTY (2-LINE MODE)



1/26 DUTY (3-LINE MODE)



ABSOLUTE MAXIMUM RATINGS**Table 13. Absolute Maximum Ratings**

Characteristics	Symbol	Value	Unit
Power supply voltage ⁽¹⁾	V _{DD}	– 0.3 to + 7.0	V
Power supply voltage ⁽²⁾	V ₀ , V _{OUT}	– 0.3 to + 13.0	V
Power supply voltage ⁽³⁾	V ₁ , V ₂ , V ₃ , V ₄	– 0.3 to V ₀	V
Operating temperature	T _{OPR}	– 30 to + 85	°C
Storage temperature	T _{STG}	– 55 to + 125	°C

NOTES:

1. Voltage greater than above may damage the circuit
2. All the voltage levels are based on V_{SS} = 0V
3. Voltage level: V_{OUT} ≥ V₀ ≥ V_{DD} ≥ V_{SS}
V₀ ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V_{SS}

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Table 14. DC Characteristics

($V_{DD} = 2.4V$ to $3.6V$, $T_a = -30$ to $+85^\circ C$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD}	—	2.4	—	3.6	V
Supply current ($V_{DD} = 3V$, $T_a = 25^\circ C$)	I_{DD1}	Display operation, $V_{LCD} = 6V$ without load No access from MPU	—	—	80	μA
	I_{DD2}	Standby operation, without load, Oscillation on, Power off	—	—	10	
	I_{DD3}	Sleep operation, without load, Oscillation off, Power off	—	—	5	
	I_{DD4}	Access operation from MPU $F_{cyc} = 200\text{ kHz}$	—	—	500	
Input voltage	V_{IH}	—	$0.8V_{DD}$	—	V_{DD}	V
	V_{IL}	—	V_{SS}	—	$0.2V_{DD}$	
Input leakage current	I_{IL}	$V_{IN} = 0V$ to V_{DD}	—1	—	1	μA
R_{ON} resistance	R_{COM}	$I_O = \pm 50\text{ }\mu A$	—	—	5	$k\Omega$
	R_{SEG}	$I_O = \pm 50\text{ }\mu A$	—	—	10	
Frame frequency	f_{FR}	$V_{DD} = 3V$, $T_a = 25^\circ C$	70	100	130	Hz
External clock frequency	f_{CK}	Display of 2-line mode	—	23.4	—	kHz
		Display of 3-line mode	—	33.8	—	
Voltage converter V_{DD} 2 or 3 times	$V_{OUT2/3}$	$T_a = 25^\circ C$, $C1 = 1\text{ }\mu F$ Without load	95	99	—	%
Voltage regulator reference voltage	V_{REF}	$T_a = 25^\circ C$	1.94	2.0	2.06	V
LCD driving voltage	V_{LCD}	$V_{LCD} = V_O - V_{SS}$	4.0	—	11.0	

Table 15. DC Characteristics

(V_{DD} = 3.6V to 5.5V, Ta = – 30 to + 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V _{DD}	–	3.6	–	5.5	V
Supply current (V _{DD} = 5V, Ta = 25°C)	I _{DD1}	Display operation, V _{LCD} = 6 V without load No access from MPU	–	–	100	μA
	I _{DD2}	Standby operation, without load, Oscillation on, Power off	–	–	20	
	I _{DD3}	Sleep operation, without load, Oscillation off, Power off	–	–	10	
	I _{DD4}	Access operation from MPU Fcyc=200 kHz	–	–	1000	
Input voltage	V _{IH}	–	0.8V _{DD}	–	V _{DD}	V
	V _{IL}	–	V _{SS}	–	0.2V _{DD}	
Input leakage current	I _{IL}	V _{IN} = 0V to V _{DD}	–1	–	1	μA
R _{ON} resistance	R _{COM}	I _O = ± 50 μA	–	–	5	kΩ
	R _{SEG}	I _O = ± 50 μA	–	–	10	
Frame frequency	f _{FR}	V _{DD} = 5 V, Ta = 25°C	70	100	130	Hz
External clock frequency	f _{CK}	Display of 2-line mode	–	23.4	–	kHz
		Display of 3-line mode	–	33.8	–	
Voltage converter V _{DD} 2 times	V _{OUT2}	Ta = 25°C, C1 = 1 μF Without load	95	99	–	%
Voltage regulator reference voltage	V _{REF}	Ta = 25°C	1.94	2.0	2.06	V
LCD driving voltage	V _{LCD}	V _{LCD} = V _O – V _{SS}	4.0	–	11.0	

NOTE: When power supply (V_{DD}) range is 3.6 V to 5.5 V, the boosting of the voltage converter is only available 2 times.

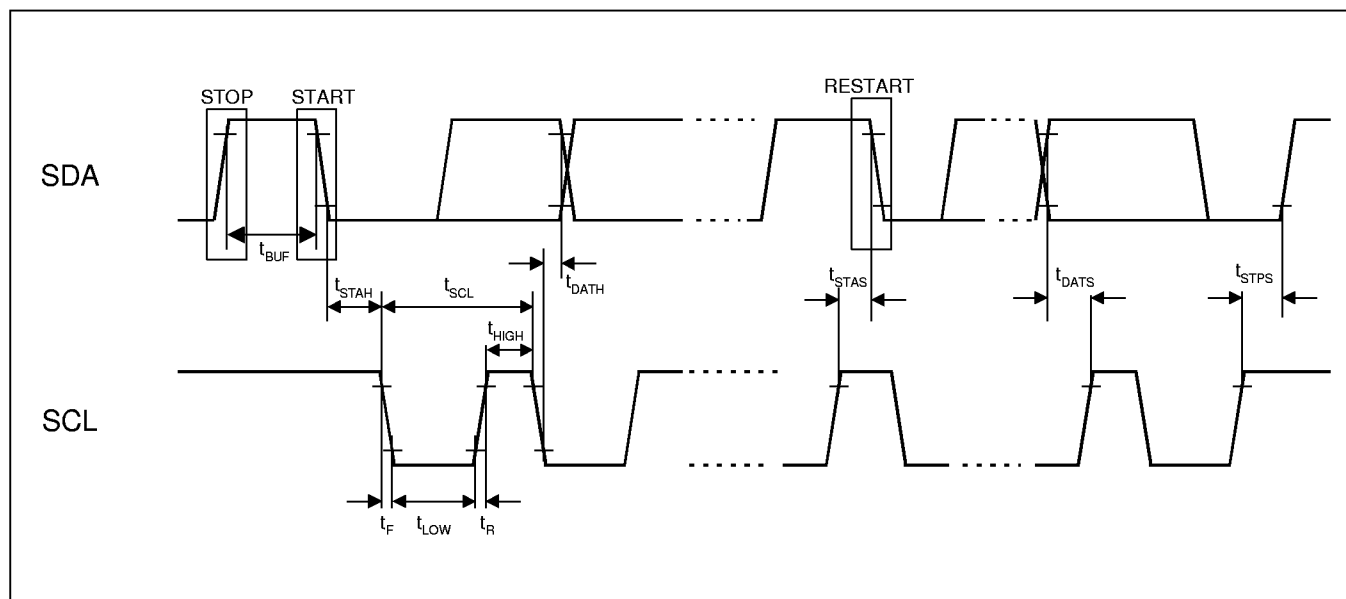
AC CHARACTERISTICS

($V_{DD} = 2.4V$ to $3.6V$, $T_a = -30$ to $+85^{\circ}C$)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
I ² C Serial Interface Mode	SCL clock cycle time	t_{SCL}	2	–	20	μs
	SCL clock high level width	t_{HIGH}	500	–	–	ns
	SCL clock low level width	t_{LOW}	1000	–	–	
	SCL/SDA rise / fall time (CL=60pF)	t_R, t_F	–	–	300	
	Bus free time	t_{BUF}	1000	–	–	
	START hold time	t_{STAH}	500	–	–	
	START setup time	t_{STAS}	500	–	–	
	SDA data setup time	t_{DATS}	140	–	–	
	SDA data hold time	t_{DATH}	0	–	–	
	STOP setup time	t_{STPS}	500	–	–	

($V_{DD} = 3.6V$ to $5.5V$, $T_a = -30$ to $+85^{\circ}C$)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
I ² C Serial Interface Mode	SCL clock cycle time	t_{SCL}	2	–	20	μs
	SCL clock high level width	t_{HIGH}	500	–	-	ns
	SCL clock low level width	t_{LOW}	1000	–	-	
	SCL/SDA rise / fall time (CL=60pF)	t_R, t_F	-	–	300	
	Bus free time	t_{BUF}	1000	–	–	
	START hold time	t_{STAH}	500	–	–	
	START setup time	t_{STAS}	500	–	–	
	SDA data setup time	t_{DATS}	100	–	–	
	SDA data hold time	t_{DATH}	0	–	–	
	STOP setup time	t_{STPS}	500	–	–	

Figure 23. I²C Serial Interface Mode Timing