

KS0063B

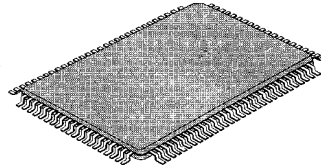
80CH SEGMENT DRIVER FOR DOT MATRIX LCD

INTRODUCTION

The KS0063B is a LCD driver LSI which is fabricated by low power CMOS technology. Basically this LSI consists of 40×2 bit bidirectional shift register, 40×2 bit data latch and 40×2 bit LCD driver (refer to Fig 1). This LSI can be used segment driver.

FUNCTION

- Dot matrix LCD driver with 80 channel output.
- Input/Output signal
 - Output : 40×2channel waveform for LCD driving
 - Input : - Serial display data and control pulse from the controller LSI.
 - Bias voltage ($V_1 - V_4$)



FEATURES

- Display driving bias ; static-1/5
- Power supply voltage ; 2.7V ~ 5.5V
- Supply voltage for display : 0 ~ - 5V(V_{EE})
- interface

driver (cascade connection)	controller
KS0065B, KS0063, Other KS0063B	KS0066/U

- CMOS Process
- I00QFP and bare chip available

BLOCK DIAGRAM

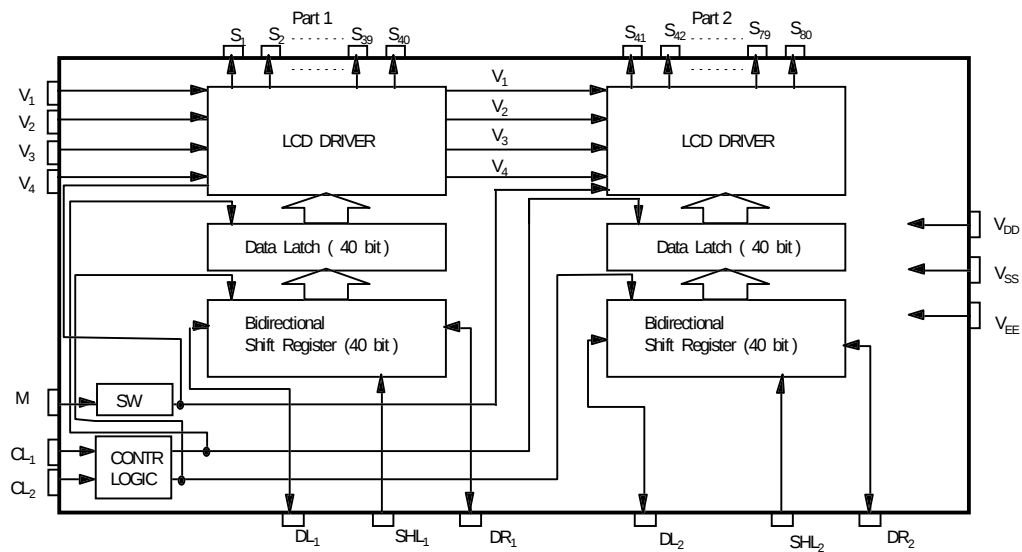


Fig. 1. KS0063 functional block diagram

80CH SEGMENT DRIVER FOR DOT MATRIX LCD

PIN CONFIGURATION

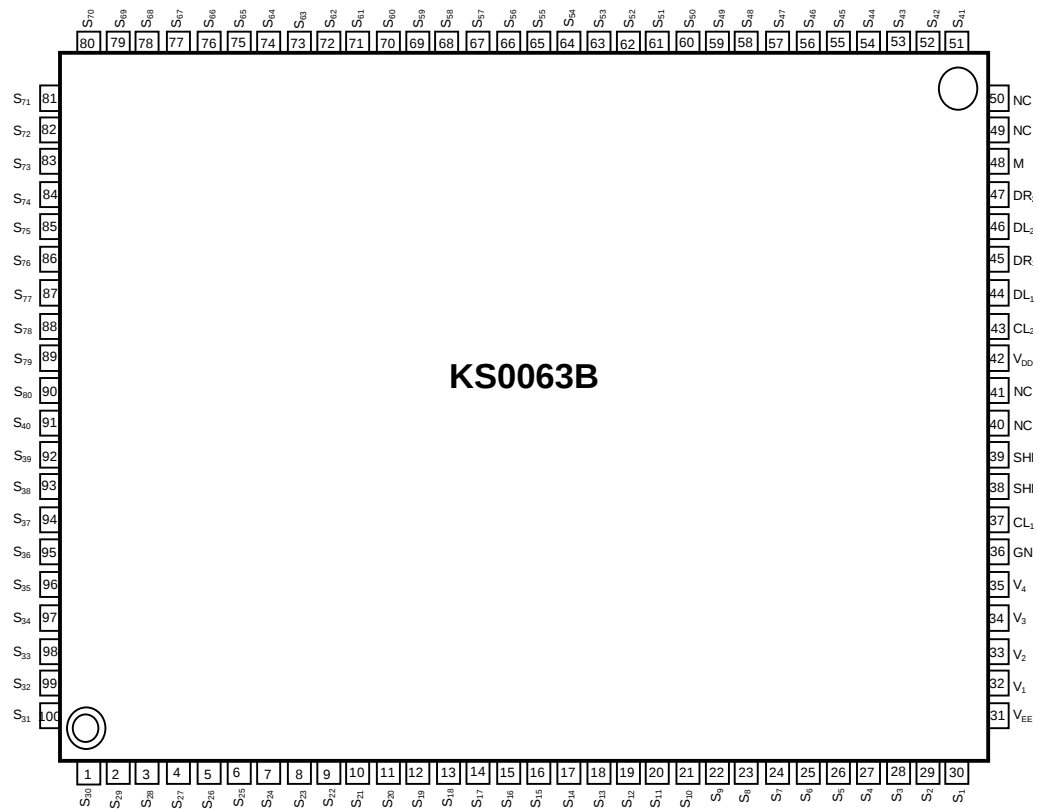


Fig. 2.100QFP Top View

KS0063B**80CH SEGMENT DRIVER FOR DOT MATRIX LCD****PIN DESCRIPTION**

PIN (NO.)	INPUT OUTPUT	NAME		DESCRIPTION	INTERFACE
V _{DD} (42)	Power	Operating Voltage		For logical circuit (2.7V ~ 5.5V)	Power Supply
V _{SS} (GND)(36)				0V (GND)	
V _{EE} (31)		Negative Supply Voltage		For LCD driver circuit (- 5V)	
V1, V2 (32,33)	Input	LCD driver output voltage level		Bias voltage level for LCD drive (Select level)	Power
V3, V4 (34,35)	Input			Bias voltage level for LCD drive (Nonselect level)	
S1 - S40	Output	Part 1	LCD driver	LCD driver output	LCD
SHL1(38)	Input		Data Interface	Selection of the shift direction of shift register	V _{DD} or V _{SS}
DL1, DR1 (44,45)	Input Output			Data Input/output of shift register (part 1)	Controller or KS0063B
S41 - S80	Output	Part 2	LCD driver	LCD driver output	LCD
SHL2 (39)	Input		Data Interface	Selection of the shift direction of shift register	V _{DD} or V _{SS}
DL2, DR2 (46,47)	Input Output			Data Input/output of shift register (part 2)	Controller or KS0063
M(48)	Input	Alternated signal for LCD driver output		The alternating signal to convert LCD drive waveform to AC	Controller
CL1, CL2 (37,43)	Input	Data shift/latch clock		CL1 : Data latch clock CL2 : Data shift clock	
NC (40, 41, 49, 50)				No connection	NC

KS0063B**80CH SEGMENT DRIVER FOR DOT MATRIX LCD****MAXIMUM ABSOLUTE LIMIT** ($T_a=25\text{ }^{\circ}\text{C}$)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	-0.3~+7.0	V
Driver Supply Voltage	V_{LCD}	$V_{DD}-13.5\sim V_{DD}+0.3$	V
Input Voltage 1	V_{IN1}	-0.3~ $V_{DD}+0.3$	V
Input Voltage 2 ($V_1\sim V_4$)	V_{IN2}	$V_{DD}+0.3\sim V_{EE}-0.3$	V
Operating Temperature	T_{OPR}	-30~+85	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55~+125	$^{\circ}\text{C}$

* Voltage greater than above may damage to the circuit

* V_{EE} : connect a protection resistor ($220\Omega \pm 5\%$)

ELECTRICAL CHARACTERISTICS**DC CHARACTERISTICS** ($V_{DD}=2.7\text{V}\sim 5.5\text{V}$, $V_{EE}=3\sim 13\text{V}$, $V_{SS}=0\text{V}$, $T_a=-30\sim +85\text{ }^{\circ}\text{C}$)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current	I _{DD}	f _{CL2} = 400KHz	-	1	mA	V _{DD} , V _{EE}
Supply Current	I _{EE}	f _{CL1} = 1KHz	-	10	μA	
Input High Voltage	V _{IH}	-	0.7V _{DD}	V _{DD}	V	CL1, CL2,DL1, DL2, DR1, DR2, SHL1, SHL2, M
Input Low Voltage	V _{IL}		0	0.3V _{DD}		
Input Leakage Current	I _{LKG}	V _{IN} = 0 ~ V _{DD}	-5	5	μA	
Output High Voltage	V _{OH}	I _{OH} = -0.4mA	V _{DD} -0.4	-	V	DL1, DL2, DR1, DR2 V(V ₁ -V ₄)-S(S ₁ -S ₈₀)
Output Low Voltage	V _{OL}	I _{OL} = +0.4mA		0.4		
Voltage Descending	V _{D1}	I _{ON} = 0.1mA for one of S ₁ - S ₈₀	-	1.1		
	V _{D2}	I _{ON} = 0.05mA for each S ₁ - S ₈₀	-	1.5		
Leakage Current	I _V	V _{IN} = V _{DD} ~ V _{EE} (Output S ₁ ~ S ₈₀ ; floating)	-10	10	μA	V ₁ - V ₄

AC CHARACTERISTICS ($V_{DD}=2.7\text{V}\sim 5.5\text{V}$, $V_{EE}=3\sim 13\text{V}$, $V_{SS}=0\text{V}$, $T_a=-30\sim +85\text{ }^{\circ}\text{C}$)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f_{CL}	-	-	400	KHz	CL2
Clock High Level Width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	-	800	-		CL2
Clock Set-up Time	t_{SL}	from CL2 to CL1	500	-		CL1, CL2
	t_{LS}	from CL1 to CL2	500	-		
Clock Rise/Fall Time	t_R/t_F	-	-	200		DL1, DL2, DR1, DR2 DL1, DL2, DR1, DR2 DL1, DL2, DR1, DR2
Data Set-up Time	t_{SU}	-	300	-		
Data Hold Time	t_{DH}	-	300	-		
Data Delay Time	t_D	$C_L = 15\text{pF}$	-	500		

TIMING CHARACTERISTICS

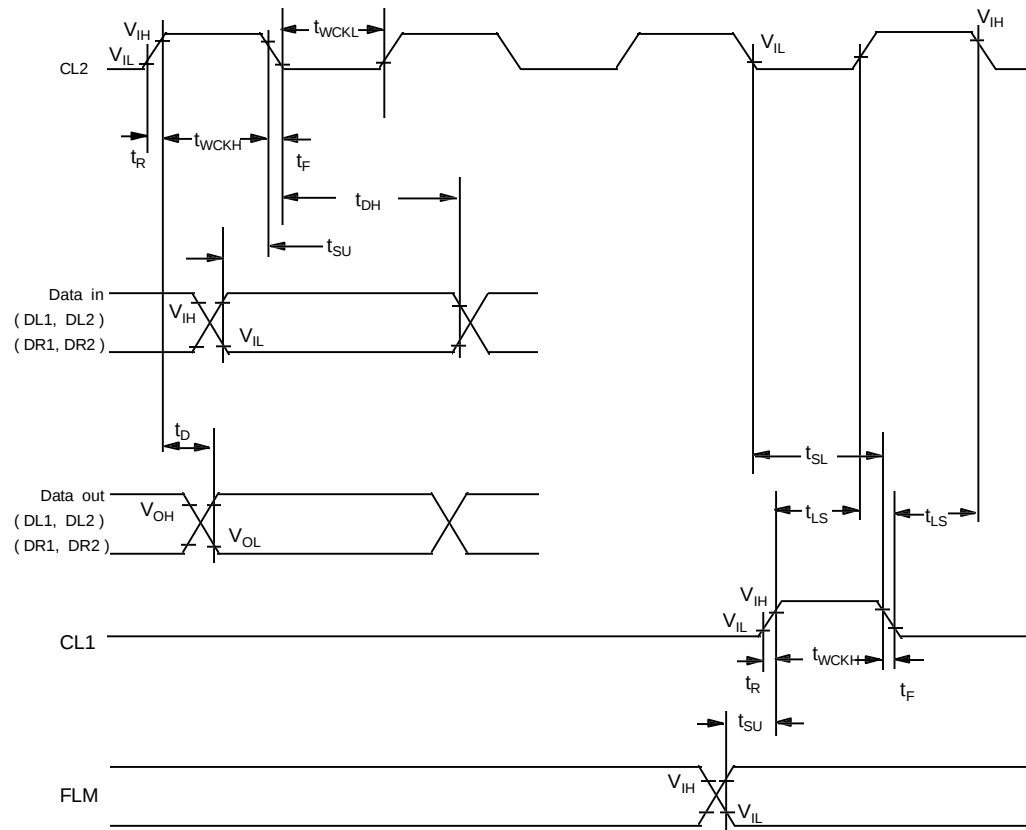
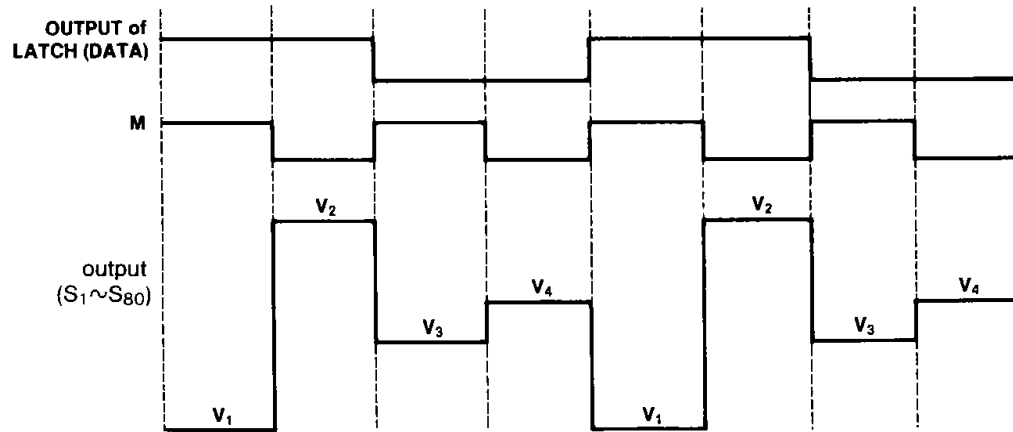


Fig. 3. AV characteristics

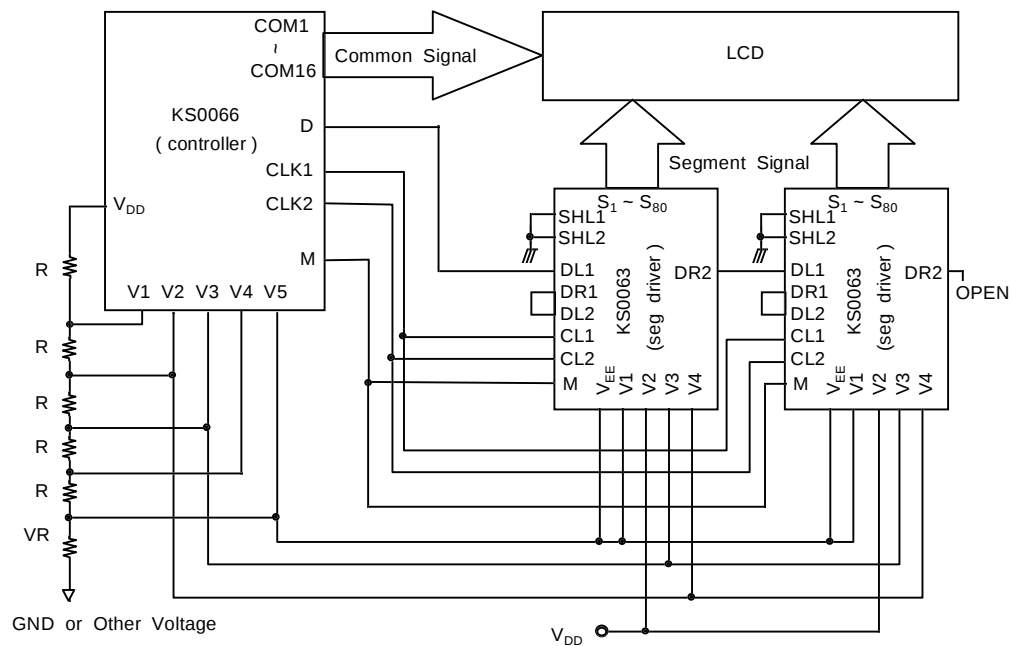
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LCD OUTPUT WAVEFORMS



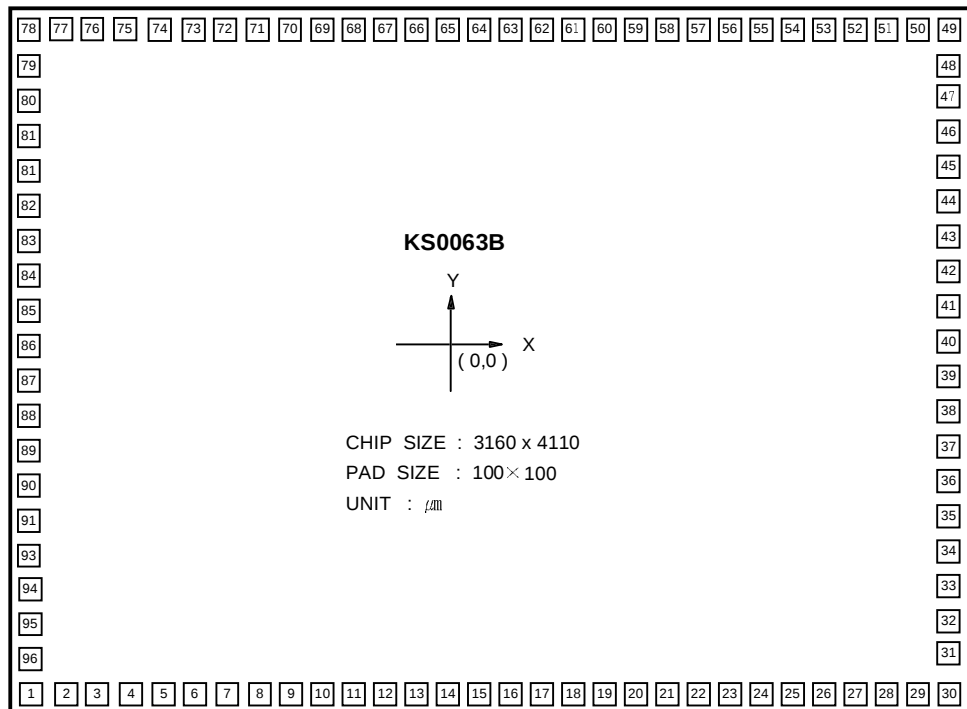
APPLICATION CIRCUIT



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PAD DIAGRAM



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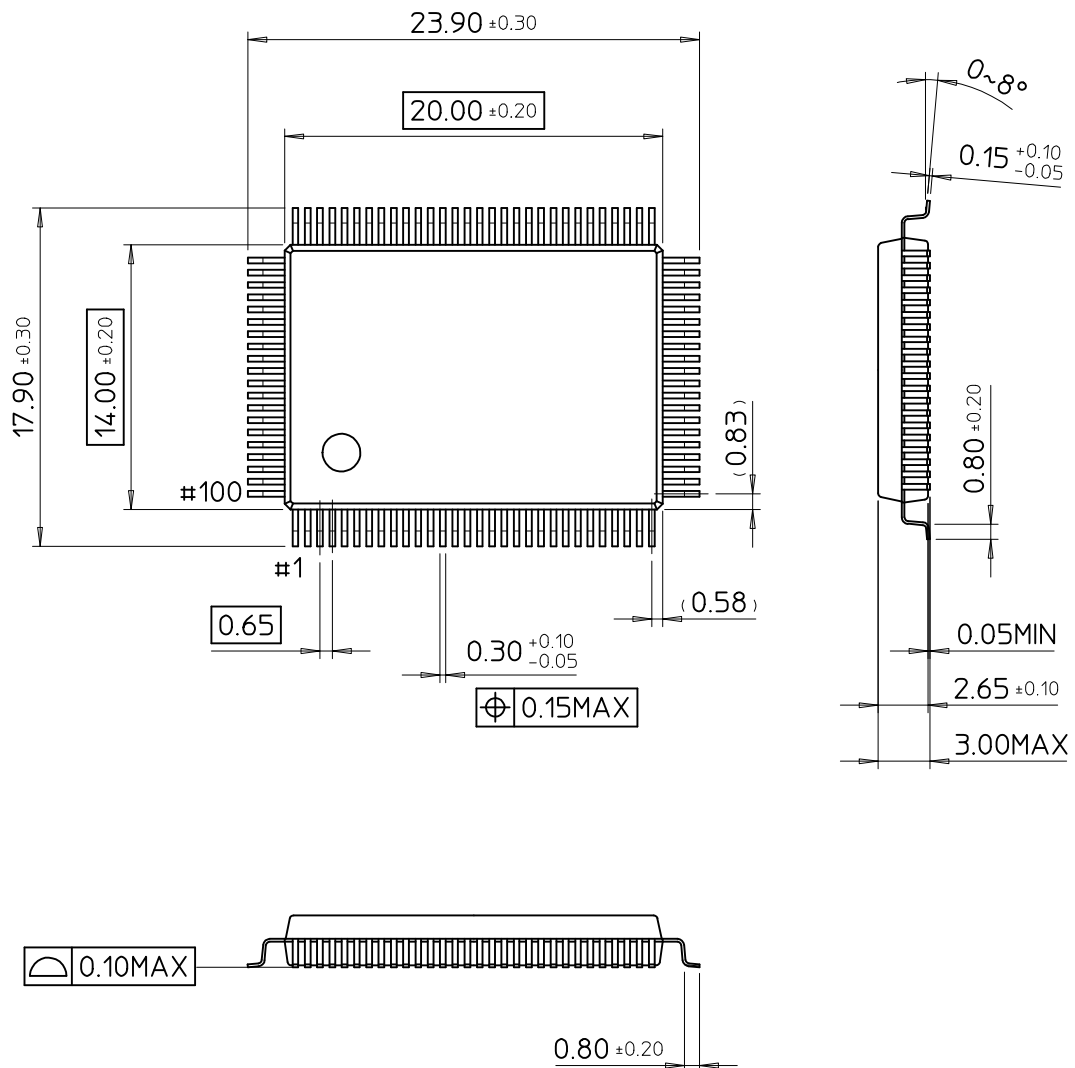
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PAD LOCATION

PAD NUMBER	PAD NAME	COORDINATE X Y		PAD NUMBER	PAD NAME	COORDINATE X Y		PAD NUMBER	PAD NAME	COORDINATE X Y	
1	S42	-1813	-1352	33	S74	1827	-812	65	S15	-188	1352
2	S43	-1688	-1352	34	S75	1827	-687	66	S14	-313	1352
3	S44	-1563	-1352	35	S76	1827	-562	67	S13	-438	1352
4	S45	-1438	-1352	36	S77	1827	-437	68	S12	-563	1352
5	S46	-1313	-1352	37	S78	1827	-312	69	S11	-688	1352
6	S47	-1188	-1352	38	S79	1827	-187	70	S10	-813	1352
7	S48	-1063	-1352	39	S80	1827	-62	71	S9	-938	1352
8	S49	-938	-1352	40	S40	1827	63	72	S8	-1063	1352
9	S50	-813	-1352	41	S39	1827	188	73	S7	-1188	1352
10	S51	-688	-1352	42	S38	1827	313	74	S6	-1313	1352
11	S52	-563	-1352	43	S37	1827	438	75	S5	-1438	1352
12	S53	-438	-1352	44	S36	1827	563	76	S4	-1563	1352
13	S54	-313	-1352	45	S35	1827	688	77	S3	-1688	1352
14	S55	-188	-1352	46	S34	1827	813	78	S2	-1813	1352
15	S56	-63	-1352	47	S33	1827	938	79	S1	-1827	1087
16	S57	62	-1352	48	S32	1827	1063	80	VFF	-1827	962
17	S58	187	-1352	49	S31	1827	1352	81	V1	-1827	837
18	S59	312	-1352	50	S30	1687	1352	82	V2	-1827	712
19	S60	437	-1352	51	S29	1562	1352	83	V3	-1827	587
20	S61	562	-1352	52	S28	1437	1352	84	V4	-1827	462
21	S62	687	-1352	53	S27	1312	1352	85	GND	-1827	313
22	S63	812	-1352	54	S26	1187	1352	86	CL1	-1827	188
23	S64	937	-1352	55	S25	1062	1352	87	SH11	-1827	63
24	S65	1062	-1352	56	S24	937	1352	88	SH12	-1827	-62
25	S66	1187	-1352	57	S23	812	1352	89	VDD	-1827	-187
26	S67	1312	-1352	58	S22	687	1352	90	CL2	-1827	-312
27	S68	1437	-1352	59	S21	562	1352	91	DI1	-1827	-437
28	S69	1562	-1352	60	S20	437	1352	92	DR1	-1827	-562
29	S70	1687	-1352	61	S19	312	1352	93	DI2	-1827	-687
30	S71	1812	-1352	62	S18	187	1352	94	DR2	-1827	-812
31	S72	1827	-1062	63	S17	62	1352	95	II	-1827	-937
32	S73	1827	-937	64	S16	-63	1352	96	S41	-1827	-1086

100-QFP-1420C

Dimensions in Millimeters



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