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ISD2560/75/90/120 Products

Single-Chip Voice Record/Playback Devices
60-, 75-, 90-, and 120-Second Durations

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Winbond Electronics Corporation America

ChipCorder®
TECHNOLOGY BY ISD

ISD2560/75/90/120 Products

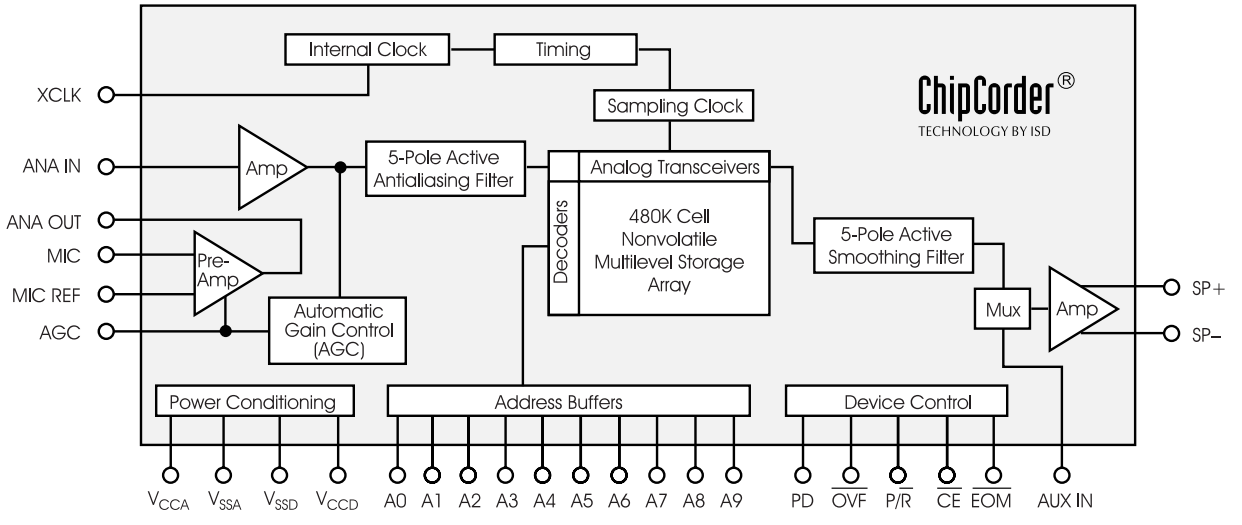
Single-Chip Voice Record/Playback Devices
60-, 75-, 90-, and 120-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD2500 ChipCorder® Series provides high-quality, single-chip record/playback solutions for 60- to 120-second messaging applications. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, speaker amplifier, and high density multilevel storage array. In addition, the ISD2500 is microcontroller compatible, allowing complex messaging and addressing to be achieved.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into memory in their natural form, providing high-quality, solid-state voice reproduction.

Figure i: ISD2560/75/90/120 Device Block Diagram



FEATURES

- Easy-to-use single-chip voice record/ playback solution
- High-quality, natural voice/audio reproduction
- Manual switch or microcontroller compatible playback can be edge- or level-activated
- Single-chip durations of 60, 75, 90, and 120 seconds
- Directly cascadable for longer durations
- Automatic Power-Down (Push-Button Mode)
  - Standby current 1 μA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- Programmer support for play-only applications
- Single +5 volt power supply
- Available in die form, DIP, SOIC, and TSOP packaging

Table i: ISD2560/75/90/120 Product Summary

Part Number	Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7

DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD2500 series includes devices offered at 4.0, 5.3, 6.4, and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects sound quality. Please refer to the ISD2560/75/90/120 Product Summary table on page *ii* to compare filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

DURATION

To meet end system requirements, the ISD2500 series offers single-chip solutions at 60, 75, 90, and 120 seconds. Parts may also be cascaded together for longer durations.

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

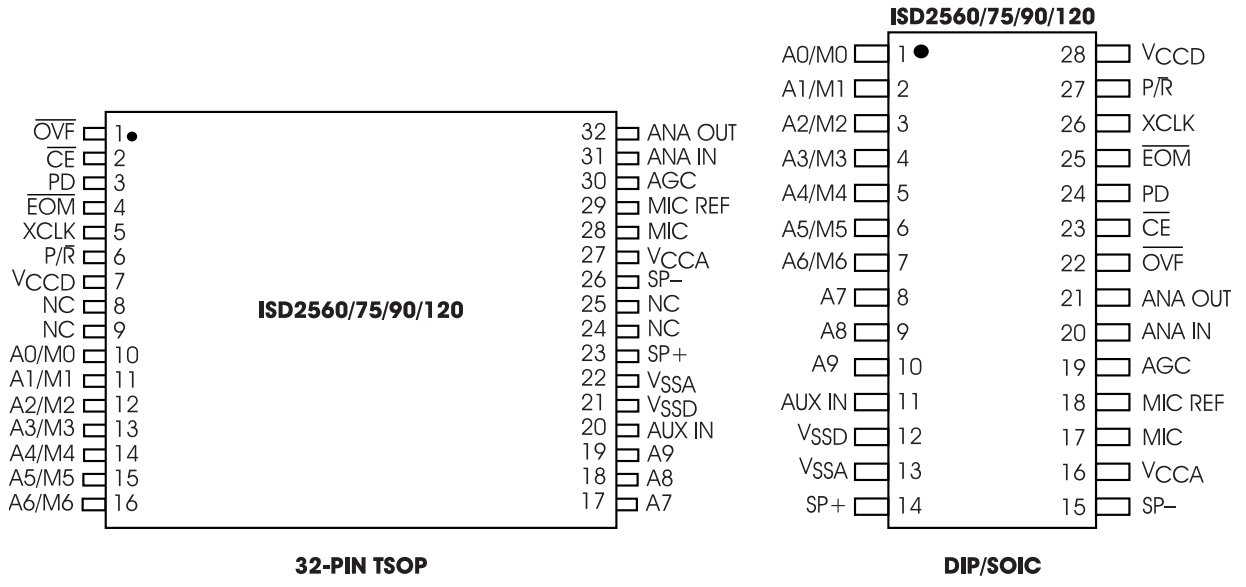
MICROCONTROLLER INTERFACE

In addition to its simplicity and ease of use, the ISD2500 series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

PROGRAMMING

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

Figure 1: ISD2560/75/90/120 Device Pinouts



PIN DESCRIPTIONS

VOLTAGE INPUTS (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

GROUND INPUTS (V_{SSA}, V_{SSD})

The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.

POWER DOWN INPUT (PD)

When not recording or playing back, the PD pin should be pulled HIGH to place the part in a very low power mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the record/playback space. The PD pin has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

CHIP ENABLE INPUT ($\overline{CE}$)

The $\overline{CE}$ pin is taken LOW to enable all playback and record operations. The address inputs and playback/record input (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

PLAYBACK/RECORD INPUT (P/$\overline{R}$)

The P/$\overline{R}$ input is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address inputs provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, an End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue past an $\overline{EOM}$ marker in an Operational Mode, or if $\overline{CE}$ is held LOW in address mode. (See page 5 for more Operational Modes).

END-OF-MESSAGE / RUN OUTPUT ($\overline{EOM}$)

A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message.

In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5 V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in playback-only mode.

When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH RUN signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for a visual indicator of a record or playback operation in process.

OVERFLOW OUTPUT ($\overline{OVF}$)

This signal pulses LOW at the end of memory space, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See Application Information for additional information on low-frequency cutoff calculation.

MICROPHONE REFERENCE INPUT (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.

AUTOMATIC GAIN CONTROL INPUT (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic on page 18) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 μF give satisfactory results in most cases.

ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

ANALOG INPUT (ANA IN)

The analog input pin transfers its signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD2500 devices has an internal pull-down device. These devices are configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. The internal clock has a ±5 percent tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 1: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD2560	8.0 KHz	1024 KHz
ISD2575	6.4 KHz	819.2 KHz
ISD2590	5.3 KHz	682.7 KHz
ISD25120	4.0 KHz	512 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. **If the XCLK is not used, this input must be connected to ground.**

SPEAKER OUTPUTS (SP+/SP–)

All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2 mW from memory).

The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers.

NOTE *Connection of speaker outputs in parallel may cause damage to the device.*

A single output may be used alone (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. Using the differential outputs results in a 4 to 1 improvement in output power.

NOTE *Never ground or drive an unused speaker output.*

AUXILIARY INPUT (AUX IN)

The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, P/$\overline{R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.

ADDRESS/MODE INPUTS (AX/MX)

The Address/Mode Inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address (A8 and A9).

If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{CE}$.

If both MSBs are HIGH, the Address/Mode Inputs are interpreted as Mode bits according to the Operational Mode table. There are six Operational Modes (M0..M6) available as indicated in the table. It is possible to use multiple Operational Modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.

OPERATIONAL MODES

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum additional components. These are described in detail below. The Operational Modes use the address pins on the ISD2500 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH (A8 and A9), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0, which is the beginning of the ISD2500 address space. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current address/mode levels are sampled and executed.

Table 2: Operational Modes Table

Mode Control	Function	Typical Use	Jointly Compatible[1]
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/play multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

1. *Additional Operational Modes can be used simultaneously with the given mode.*

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

M0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the M4 Operational Mode.

M1 — DELETE $\overline{EOM}$ MARKERS

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{EOM}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 — UNUSED

When Operational Modes are selected, the M2 pin should be LOW.

M3 — MESSAGE LOOPING

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{OVF}$ going LOW.

M4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 — $\overline{CE}$-LEVEL ACTIVATED

The default mode for ISD2500 devices is for $\overline{CE}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is specifically useful for terminating playback operations using the $\overline{CE}$ signal.

In this mode, $\overline{CE}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{CE}$ is held LOW. When $\overline{CE}$ goes HIGH, playback will immediately end. A new $\overline{CE}$ LOW will restart the message from the beginning unless M4 is also HIGH.

M6 — PUSH-BUTTON MODE

The ISD2500 series of devices contain a Push-Button Operational Mode. The Push-Button mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in Push-Button Operational Mode, the two most significant address bits must be HIGH, and the M6 mode pin must also be HIGH. A device in this mode always powers down at the end of each playback or record cycle after $\overline{CE}$ goes HIGH.

When this Operational Mode is implemented, several of the pins on the device have alternate functionality:

Table 3: Alternate Functionality in Pins

Pin Name	Alternate Functionality in Push-Button Mode
$\overline{CE}$	Start/Pause Push-Button (LOW pulse-activated)
PD	Stop/Reset Push-Button (HIGH pulse activated)
$\overline{EOM}$	Active-HIGH Run Indicator

$\overline{CE}$ PIN (START/PAUSE)

In Push-Button Operational Mode, $\overline{CE}$ acts as a LOW-going pulse-activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or a record cycle according to the level on the P/$\overline{R}$ pin. A subsequent pulse on the $\overline{CE}$ pin, before an End-Of-Message is reached in playback or an overflow condition occurs, will cause the device to pause. The address counter is not reset, and another $\overline{CE}$ pulse will cause the device to continue the operation from the place where it was paused.

PD PIN (STOP/RESET)

In push-button Operational Mode, PD acts as a HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

$\overline{EOM}$ PIN (RUN)

In Push-Button Operational Mode, $\overline{EOM}$ becomes an active-HIGH RUN signal which can be used to drive an LED or other external device. It is HIGH whenever a record or playback operation is in progress.

Recording in Push-Button Mode

1. The PD pin should be LOW, usually using a pull-down resistor.
2. The P/$\overline{R}$ pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. The $\overline{CE}$ pin is pulsed LOW. Recording pauses, $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but an EOM marker is stored in memory to point to the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set EOM marker. $\overline{EOM}$ goes back HIGH.

NOTE *If the M1 Operational Mode pin is also HIGH, the just previously written EOM bit is erased, and recording starts at that address.)*

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6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set EOM marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The P/$\overline{R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an EOM marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

NOTE *Push-button mode can be used in conjunction with modes M0, M1, and M3.*

GOOD AUDIO DESIGN PRACTICES

ISD products are very high-quality single-chip voice recording and playback systems. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling be followed. See the ISD Application Notes in this book for details.

ISD1000A COMPATIBILITY

The ISD2500 series of devices is designed to provide upward compatibility with the ISD1000A family. When designing with the ISD2500 series, the following differences should be noted.

ADDRESSING

The ISD2560/75/90/120 devices have 480K storage cells designed to provide 60 seconds of storage at a sampling rate of 8.0 KHz. This is approximately four times the storage of the ISD1000A family. To enable the same addressing resolution, two additional address pins have been added. The address space of each device is divisible into 600 increments with valid addressing from 00 to 257 Hex. Some higher addresses are mapped into the Operational Modes. All other addresses are invalid.

OVERFLOW

The ISD1000A series combined two functions on the $\overline{EOM}$ pin: end-of-message indication and overflow. The ISD2500 separates these two functions. Pin 25 (PDIP package) remains as $\overline{EOM}$, but outputs only the EOM signal indication. Pin 22 (PDIP package) becomes $\overline{OVF}$ and pulses LOW only when the device reaches its end of memory, or is "full." This change allows easy message cueing and addressability across device boundaries. This also means that the M2 Operational Mode found in the ISD1000A family is not implemented in the ISD2500 series.

PUSH-BUTTON MODE

The ISD2500 series includes an additional Operational Mode called Push-Button mode. This provides an alternative interface to the record and playback functions of the part. The $\overline{CE}$ and PD pins become redefined as edge-activated "push-buttons." A pulse on $\overline{CE}$ initiates a cycle, and if triggered again, pauses the current cycle without resetting the address pointer (i.e., a Start or Pause function). PD stops any current cycle and resets the address pointer to the beginning of the message space (i.e., a Stop and Reset function). Additionally, the $\overline{EOM}$ pin functions as an active-HIGH run indicator, and can be used to drive an LED indicating a record or playback operation is in progress. Devices in the Push-Button mode cannot be cascaded.

LOOPING MODE

The ISD2500 series can loop with a message that completely fills the memory space.

NOTE *Additional descriptions of ISD2500 device functionality and application examples are provided in the ISD Application Notes in this book.*

TIMING DIAGRAMS

Figure 2: Record

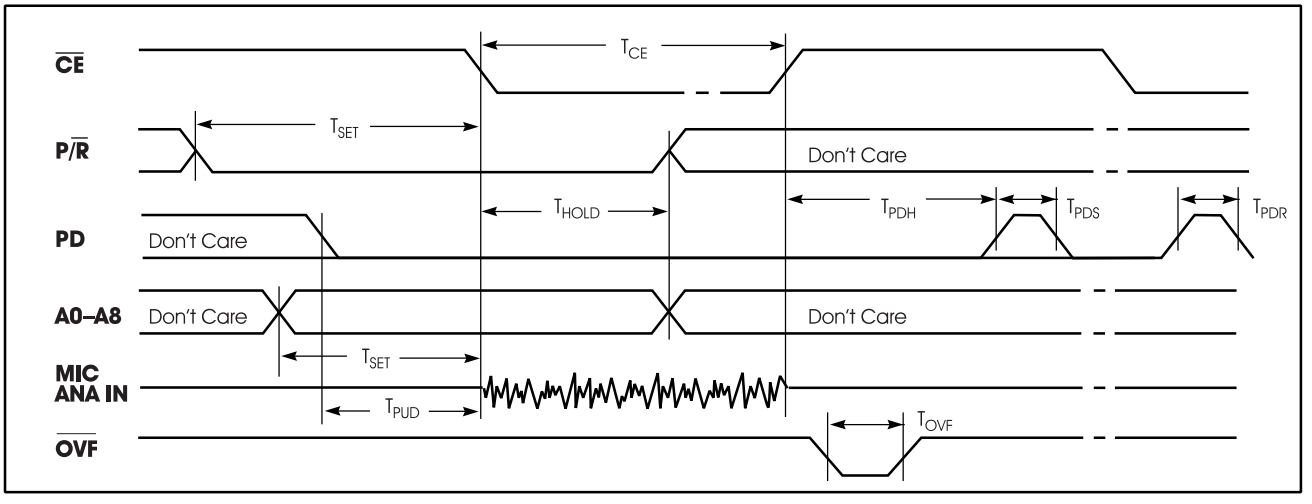


Figure 3: Playback

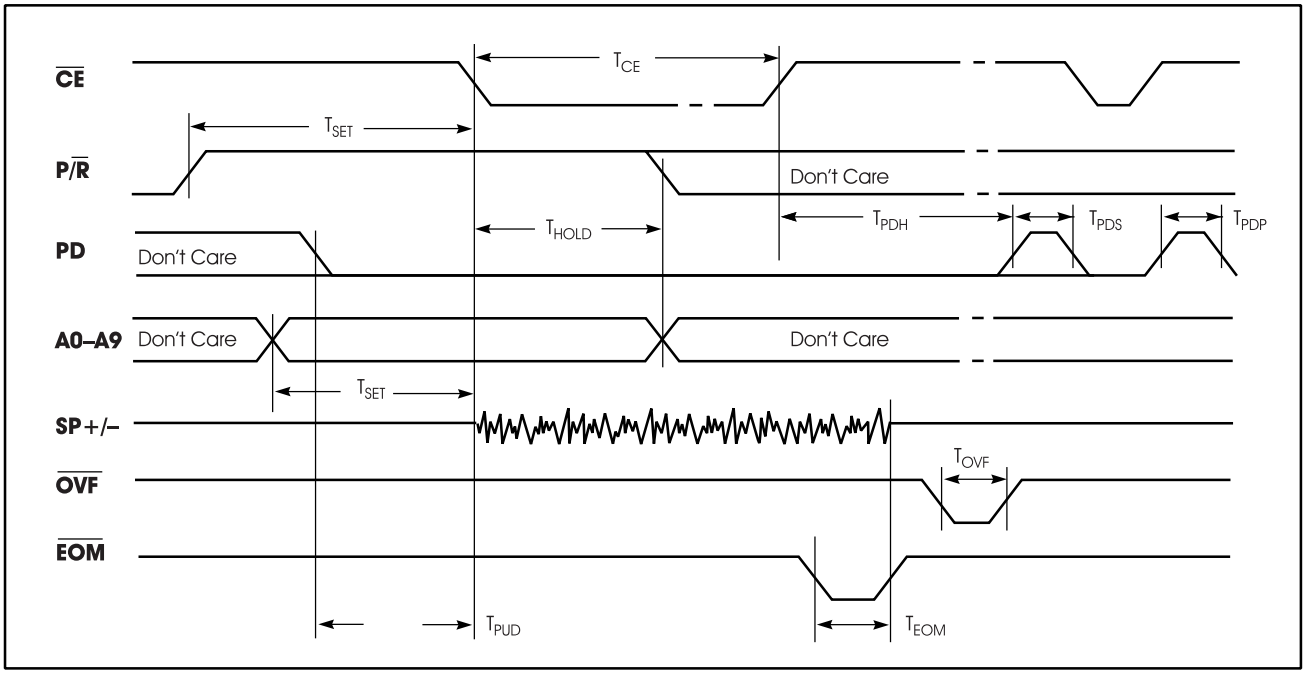


Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Industrial operating temperature range[1]	
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. *$V_{CC} = V_{CCA} = V_{CCD}$.*
3. *$V_{SS} = V_{SSA} = V_{SSD}$.*
4. *Consult factory.*

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC}–0.4			V	I_{OH} = –10 μA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage	V_{CC} – 1.0	V_{CC} – 0.8		V	I_{OH} = –3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	μA	[3]
I_{IL}	Input Leakage Current			±1	μA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	μA	Force V_{CC} [4]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	15	KΩ	MIC and MIC REF Pins
R_{AUX}	AUX INPUT Resistance	5	11	20	KΩ	

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
$R_{ANA\ IN}$	ANA IN Input Resistance	2.3	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		–15	5	dB	AGC = 2.5 V
A_{AUX}	AUX IN/SP+ Gain		0.98	1.0	V/V	
A_{ARP}	ANA IN to SP+/– Gain	21	23	26	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *XCLK pin only.*

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD2560		8.0		KHz	(7)
		ISD2575		6.4		KHz	(7)
		ISD2590		5.3		KHz	(7)
		ISD25120		4.0		KHz	(7)
F_{CF}	Filter Pass Band	ISD2560		3.4		KHz	3 dB Roll-Off Point (3) (8)
		ISD2575		2.7		KHz	3 dB Roll-Off Point (3) (8)
		ISD2590		2.3		KHz	3 dB Roll-Off Point (3) (8)
		ISD25120		1.7		KHz	3 dB Roll-Off Point (3) (8)
T_{REC}	Record Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation(7)
		ISD2560	56.5	60.0	63.8	sec	Industrial Operation(7)
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation(7)
		ISD2575	70.7	75.0	79.7	sec	Industrial Operation(7)
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation(7)
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation(7)
T_{PLAY}	Playback Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation
		ISD2560	56.5	60.0	63.8	sec	Industrial Operation
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation
		ISD2575	70.7	75.0	79.7	sec	Industrial Operation
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation
T_{CE}	$\overline{CE}$ Pulse Width			100		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{HOLD}	Control/Address Hold Time			0		nsec	

Table 7: AC Parameters (Packaged Parts)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
T_{PUD}	Power-Up Delay	ISD2560	24.1	25.0	27.8	msec	Commercial Operation
		ISD2560	23.5		28.5	msec	Industrial Operation
		ISD2575	30.2	31.3	34.3	msec	Commercial Operation
		ISD2575	29.3	31.3	35.2	msec	Industrial Operation
		ISD2590	36.2	37.5	40.8	msec	Commercial Operation
		ISD25120	48.2	50.0	53.6	msec	Commercial Operation
T_{PDR}	PD Pulse Width Record	ISD2560		25		msec	
		ISD2575		31.25		msec	
		ISD2590		37.5		msec	
		ISD25120		50.0		msec	
T_{PDP}	PD Pulse Width Play	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{PDS}	PD Pulse Width Static			100		nsec	(6)
T_{PDH}	Power Down Hold			0		nsec	
T_{EOM}	$\overline{EOM}$ Pulse Width	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{OVF}	Overflow Pulse Width			6.5		µsec	
THD	Total Harmonic Distortion			1	2	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2	50	mW	R_{EXT} = 16 Ω (4)
V_{OUT}	Voltage Across Speaker Pins				2.5	V p–p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak (5)
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak
V_{IN3}	Aux Input Voltage				1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).*
4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.*
5. *With 5.1 KΩ series resistor at ANA IN.*
6. *T_{PDS} is required during a static condition, typically overflow.*
7. *Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range and voltage range and ±5 percent over the industrial temperature and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*
8. *Filter specification applies to both the antialiasing filter and the smoothing filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through both filters.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)

Chart 1: Record Mode Operating Current (I_{CC})

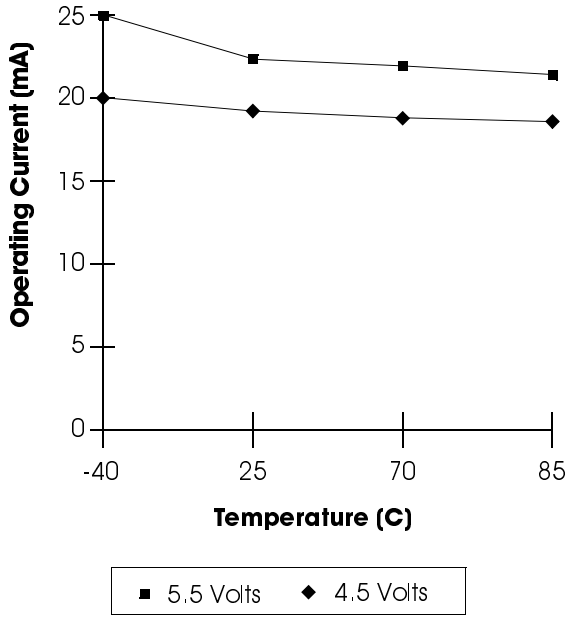


Chart 2: Total Harmonic Distortion

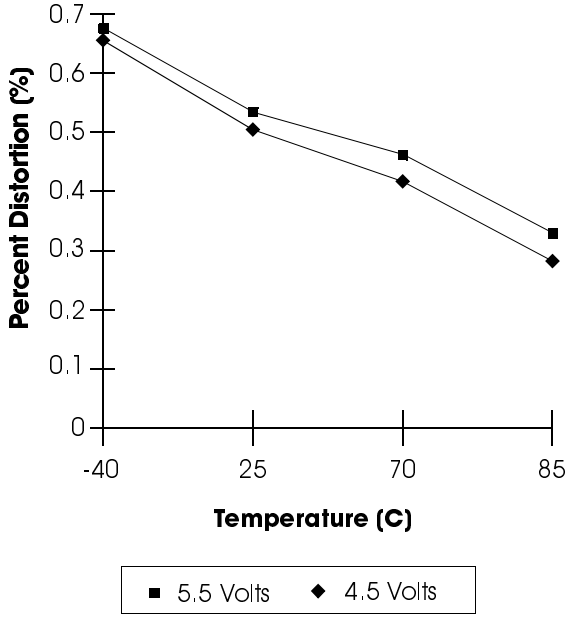


Chart 3: Standby Current (I_{SB})

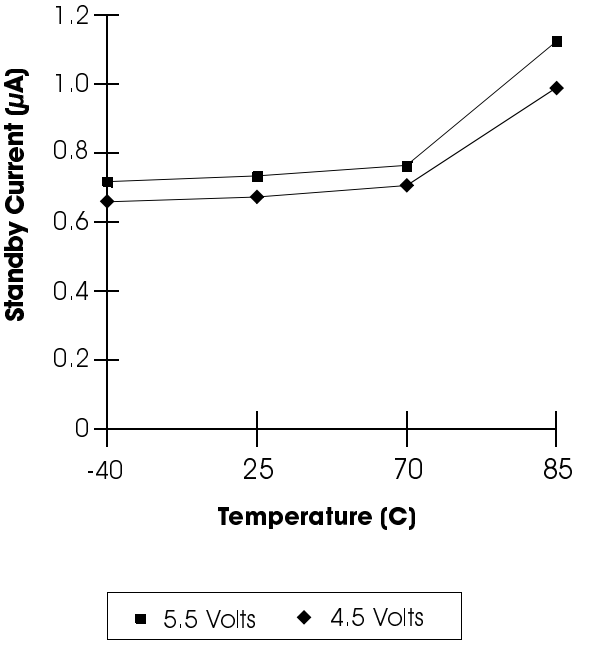


Chart 4: Oscillator Stability

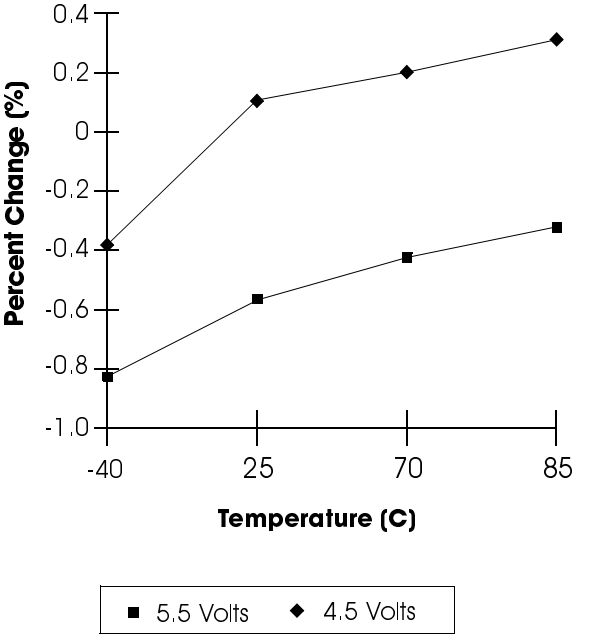


Table 8: Absolute Maximum Ratings (Die)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pad	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V_{SS} –1.0 V) to (V_{CC} + 1.0 V)
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 9: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})[1]	+4.5 V to +6.5 V
Ground voltage (V_{SS})[2]	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.

Table 10: DC Parameters (Die)

Symbol	Parameters	Min[2]	Typ [1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage	V_{CC} – 1.0	V_{CC} – 0.8		V	I_{OH} = –3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	$R_{EXT} = \infty$ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[2]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH with Pull Down			130	µA	Force V_{CC} [4]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	15	KΩ	MIC and MIC REF Pads
R_{AUX}	AUX INput Resistance	5	11	20	KΩ	
$R_{ANA\ IN}$	ANA IN Input Resistance	2.3	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V

Table 10: DC Parameters (Die)

Symbol	Parameters	Min(2)	Typ (1)	Max(2)	Units	Conditions
A_{PRE2}	Preamp Gain 2		–15	5	dB	AGC = 2.5 V
A_{AUX}	AUX IN/SP+ Gain		0.98	1.0	V/V	
A_{ARP}	ANA IN to SP+/- Gain	21	23	26	dB	
R_{AGC}	AGC Output Resistance	2.5	5	9.5	KΩ	

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} connected together.*
4. *XCLK pad only.*

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
F_S	Sampling Frequency	ISD2560		8.0		KHz	(7)
		ISD2575		6.4		KHz	(7)
		ISD2590		5.3		KHz	(7)
		ISD25120		4.0		KHz	(7)
F_{CF}	Filter Pass Band	ISD2560		3.4		KHz	3 dB Roll-Off Point (3) (8)
		ISD2575		2.7		KHz	3 dB Roll-Off Point (3) (8)
		ISD2590		2.3		KHz	3 dB Roll-Off Point (3) (8)
		ISD25120		1.7		KHz	3 dB Roll-Off Point (3) (8)
T_{REC}	Record Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation(7)
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation(7)
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation(7)
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation(7)
T_{PLAY}	Playback Duration	ISD2560	58.1	60.0	62.0	sec	Commercial Operation(7)
		ISD2575	72.6	75.0	77.5	sec	Commercial Operation(7)
		ISD2590	87.1	90.0	93.0	sec	Commercial Operation(7)
		ISD25120	116.1	120.0	123.9	sec	Commercial Operation(7)
T_{CE}	$\overline{CE}$ Pulse Width			100		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{HOLD}	Control/Address Hold Time			0		nsec	
T_{PUD}	Power-Up Delay	ISD2560	24.1	25.0	27.8	msec	Commercial Operation
		ISD2575	30.2	31.3	34.3	msec	Commercial Operation
		ISD2590	36.2	37.5	40.8	msec	Commercial Operation
		ISD25120	48.2	50.0	53.6	msec	Commercial Operation

Table 11: AC Parameters (Die)

Symbol	Characteristic		Min(2)	Typ (1)	Max(2)	Units	Conditions
T_{PDR}	PD Pulse Width Record	ISD2560		25		msec	
		ISD2575		31.25		msec	
		ISD2590		37.5		msec	
		ISD25120		50.0		msec	
T_{PDP}	PD Pulse Width Play	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{PDS}	PD Pulse Width Static			100		nsec	(6)
T_{PDH}	Power Down Hold			0		nsec	
T_{EOM}	$\overline{EOM}$ Pulse Width	ISD2560		12.5		msec	
		ISD2575		15.625		msec	
		ISD2590		18.75		msec	
		ISD25120		25.0		msec	
T_{OVF}	Overflow Pulse Width			6.5		µsec	
THD	Total Harmonic Distortion			1	3	%	@ 1 KHz
P_{OUT}	Speaker Output Power			12.2	50	mW	R_{EXT} = 16 Ω(4)
V_{OUT}	Voltage Across Speaker Pins				2.5	V p–p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage				20	mV	Peak-to-Peak (5)
V_{IN2}	ANA IN Input Voltage				50	mV	Peak-to-Peak
V_{IN3}	Aux Input Voltage				1.25	V	Peak-to-Peak; R_{EXT} = 16 Ω

1. *Typical values @ T_A = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon the value of external capacitors (see Pin Descriptions).*
4. *From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.*
5. *With 5.1 KΩ series resistor at ANA IN.*
6. *T_{PDS} is required during a static condition, typically overflow.*
7. *Sampling Frequency and playback Duration can vary as much as ±2.25 percent over the commercial temperature range and voltage range. For greater stability, an external clock can be utilized (see Pin Descriptions).*
8. *Filter specification applies to the antialiasing filter and the smoothing filter.*

TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

Chart 5: Record Mode Operating Current (I_{CC})

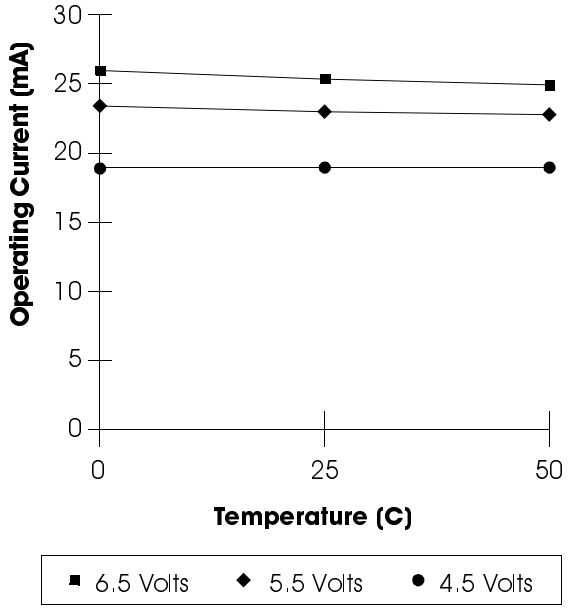


Chart 6: Total Harmonic Distortion

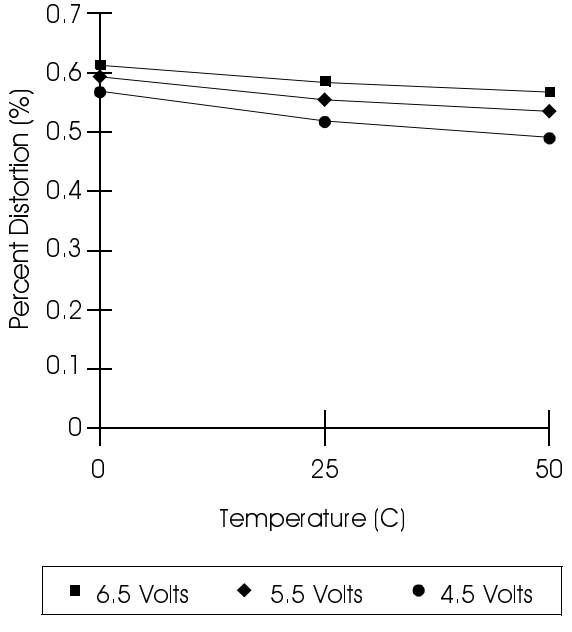


Chart 7: Standby Current (I_{SB})

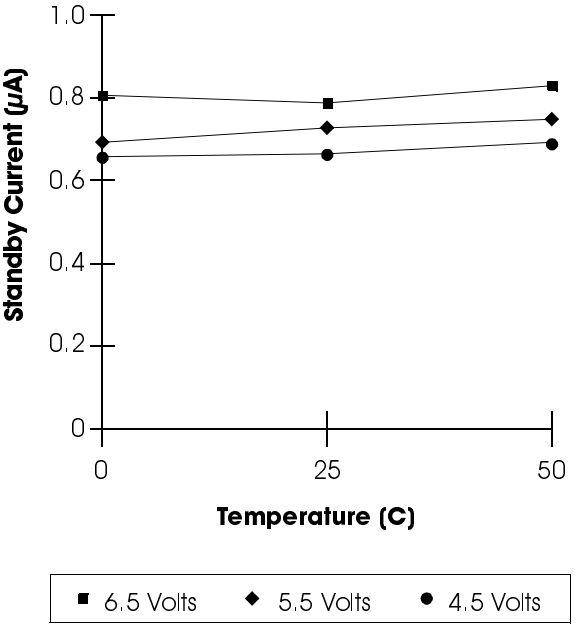


Chart 8: Oscillator Stability

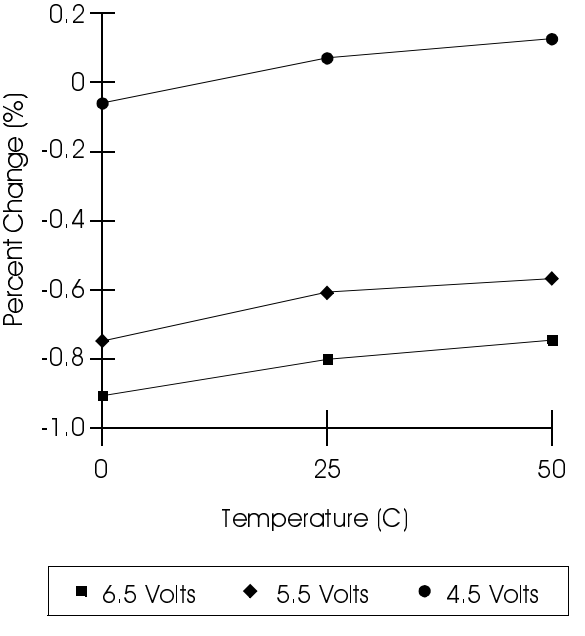
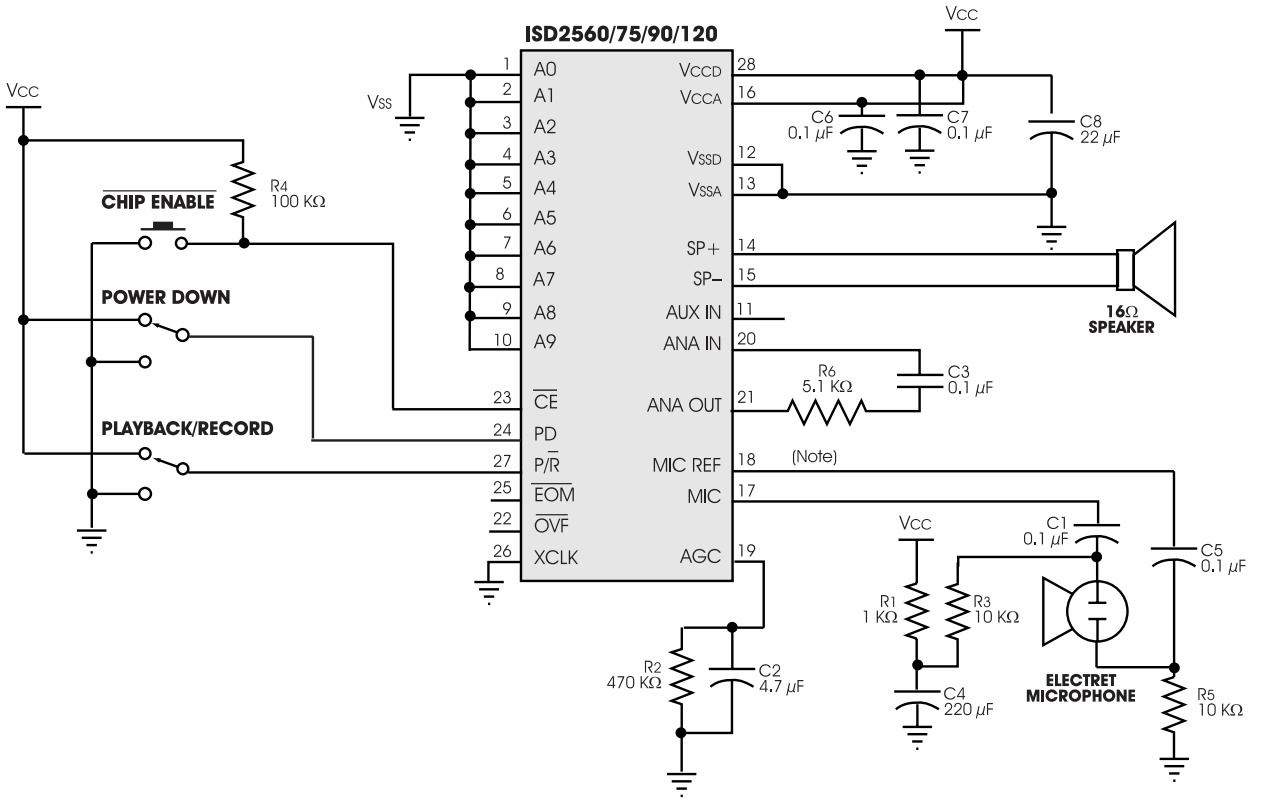


Figure 4: ISD2560/75/90/120 Application Example—Design Schematic



NOTE: *If desired, pin 18 (PDIP package) may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage. Additional design example schematics are provided in the Application Notes in this book.*

Table 12: Application Example—Basic Device Control

Control Step	Function	Action
1	Power up chip and select record/playback mode	(1.) PD = LOW, (2.) P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0–A9
3A	Begin playback	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulsed LOW
3B	Begin record	P/$\overline{R}$ = LOW, $\overline{CE}$ = LOW
4A 4B	End playback End record	Automatic PD or $\overline{CE}$ = HIGH

Table 13: Application Example—Passive Component Functions

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3, R5	Microphone biasing resistors	Provides biasing for microphone operation
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages.
R6	Series limiting resistor	Reduces level to high supply voltages
C1, C5	Microphone DC–blocking capacitor Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-frequency cutoff and common mode noise rejection.
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C6, C7, C8	Power supply capacitors	Filter and bypass of power supply

EXPLANATION

In this simplified block diagram of a microcontroller application, the Push-Button mode and message cueing are used. The microcontroller is a 16-pin version with enough port pins for buttons, an LED, and the ISD2500 series device. The software can be written to use three buttons: one each for play and record, and one for message selection. Because the microcontroller is interpreting the buttons and commanding the ISD2500 device, software can be written for any functions desired in a particular application.

NOTE *ISD does not recommend connecting address lines directly to a microprocessor bus. Address lines should be externally latched.*

Figure 5: ISD2560/75/90/120 Application Example—Microcontroller/ISD2500 Interface

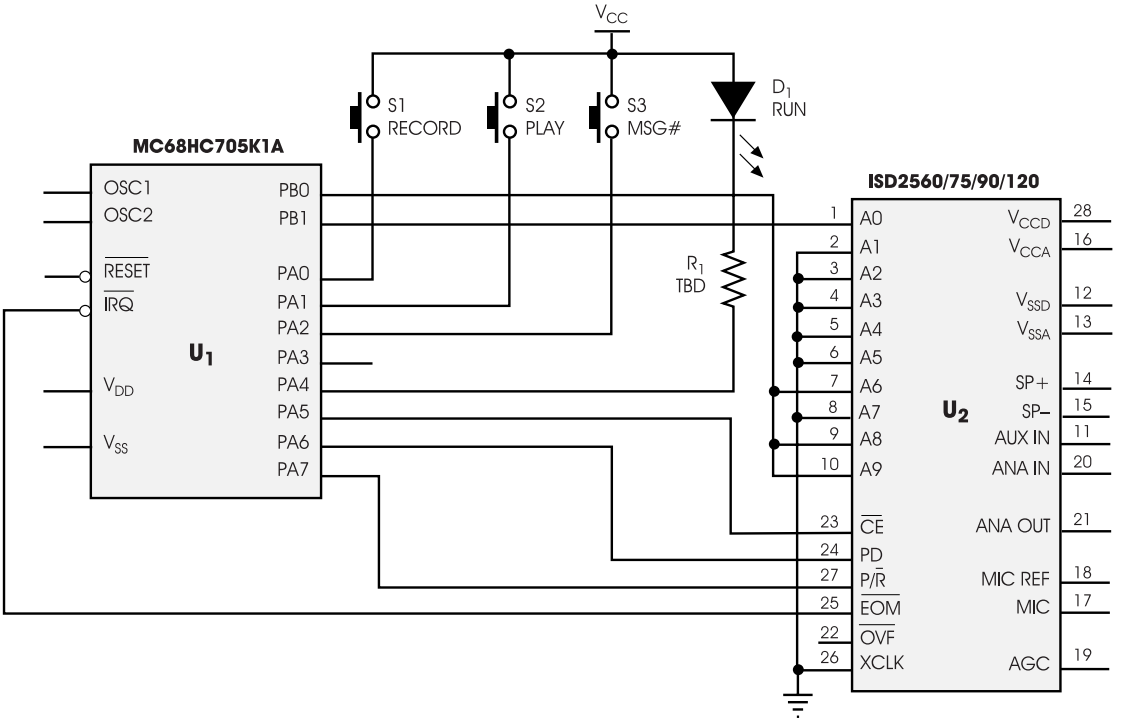
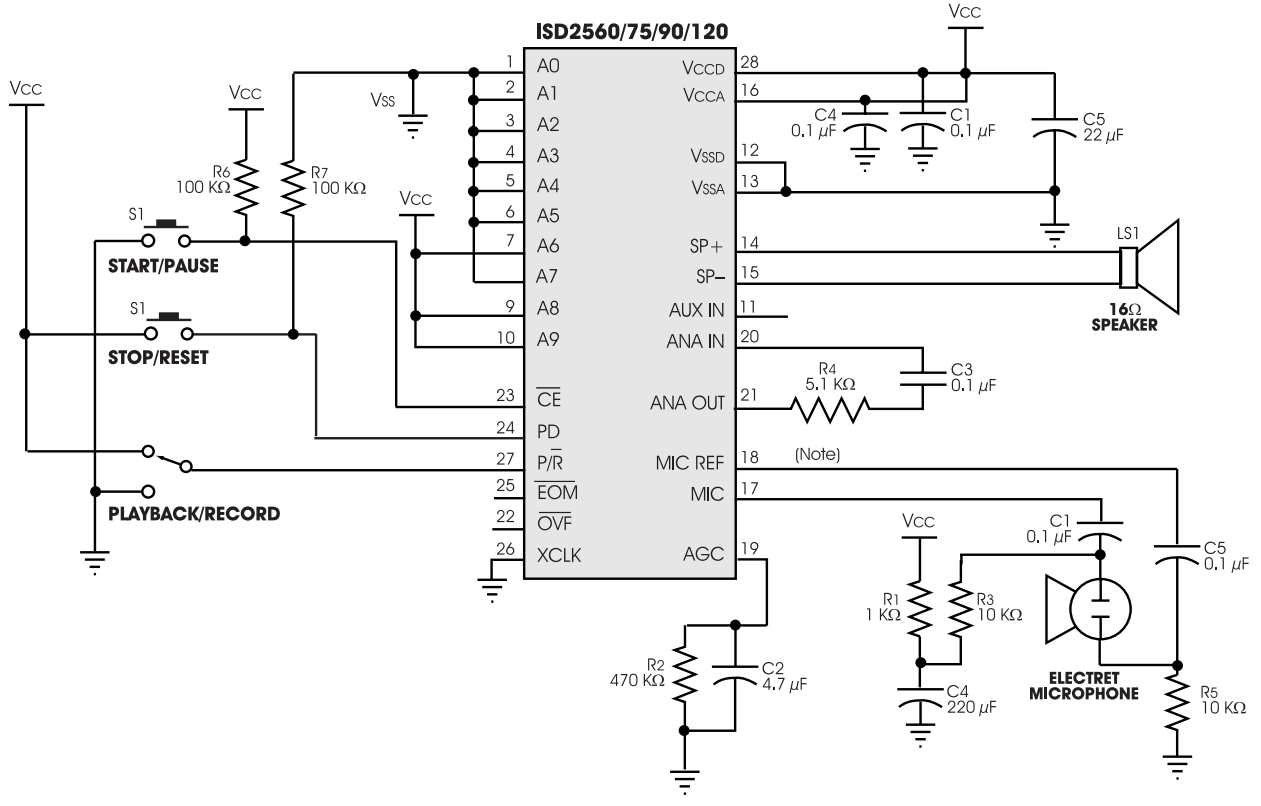


Figure 6: ISD2500 Application Example—Push-Button



NOTE: *Please refer to Application Information.*

Table 14: Application Example—Push-Button Control

Control Step	Function	Action
1	Select record/playback mode	P/$\overline{R}$ = As desired
2A 2B	Begin playback Begin record	P/$\overline{R}$ = HIGH, $\overline{CE}$ = Pulsed LOW P/$\overline{R}$ = LOW, $\overline{CE}$ = Pulsed LOW
3	Pause record or playback	$\overline{CE}$ = Pulsed LOW
4A 4B	End playback End record	Automatic at $\overline{EOM}$ marker or PD = Pulsed HIGH PD = Pulsed HIGH

Table 15: Application Example—Passive Component Functions

Part	Function	Comments
R2	Release time constant	Sets release time for AGC
R4	Series limiting resistor	Reduces level to prevent distortion at higher supply voltages
R6, R7	Pull-up and pull-down resistors	Defines static state of inputs
C1, C4, C5	Power supply capacitors	Filters and bypass of power supply
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff

Table 16: Push-Button Parameters

Symbol	Characteristic		Min	Typ (1)	Max	Units	Conditions
T_{CE}	$\overline{CE}$ Pulse Width [Start/Pause]			300		nsec	
T_{SET}	Control/Address Setup Time			300		nsec	
T_{PUD}	Power-Up Delay	ISD2560 ISD2575 ISD2590 ISD25120		25 31.25 37.25 50.0		msec msec msec msec	
T_{PD}	PD Pulse Width [Stop/Reset]			300		nsec	
T_{RUN}	$\overline{CE}$ to $\overline{EOM}$ HIGH		25		400	nsec	
T_{PAUSE}	$\overline{CE}$ to $\overline{EOM}$ LOW		50		400	nsec	
T_{DB}	$\overline{CE}$ HIGH Debounce	ISD2560 ISD2575 ISD2590 ISD25120	70 85 105 135		105 135 160 215	msec msec msec msec	

PUSH-BUTTON TIMING DIAGRAMS

Figure 7: Push-Button Mode Record

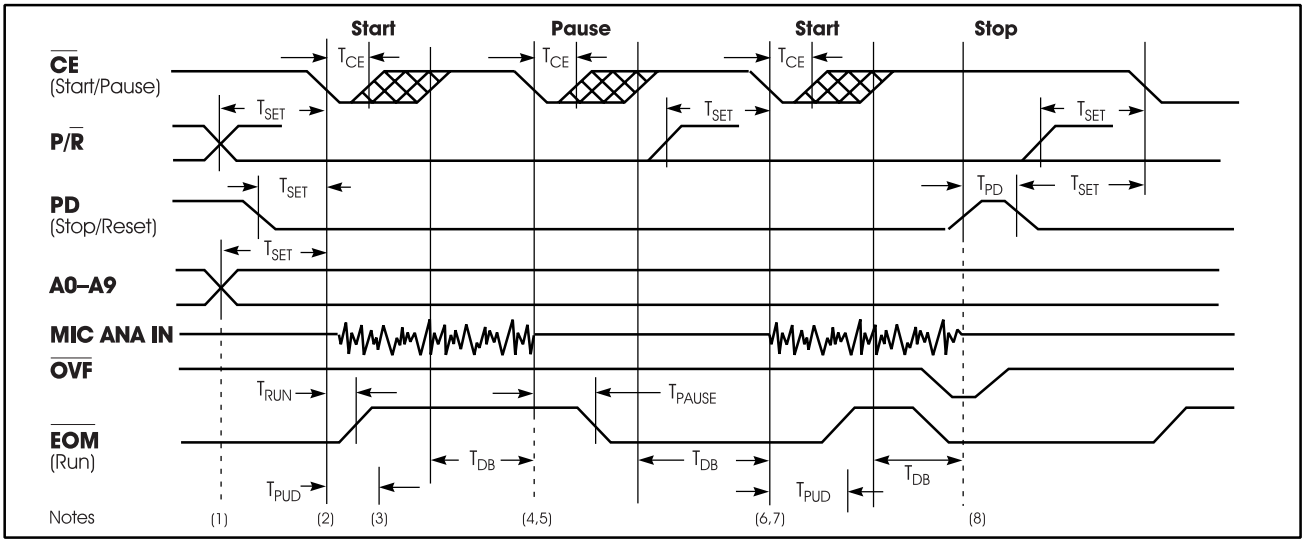
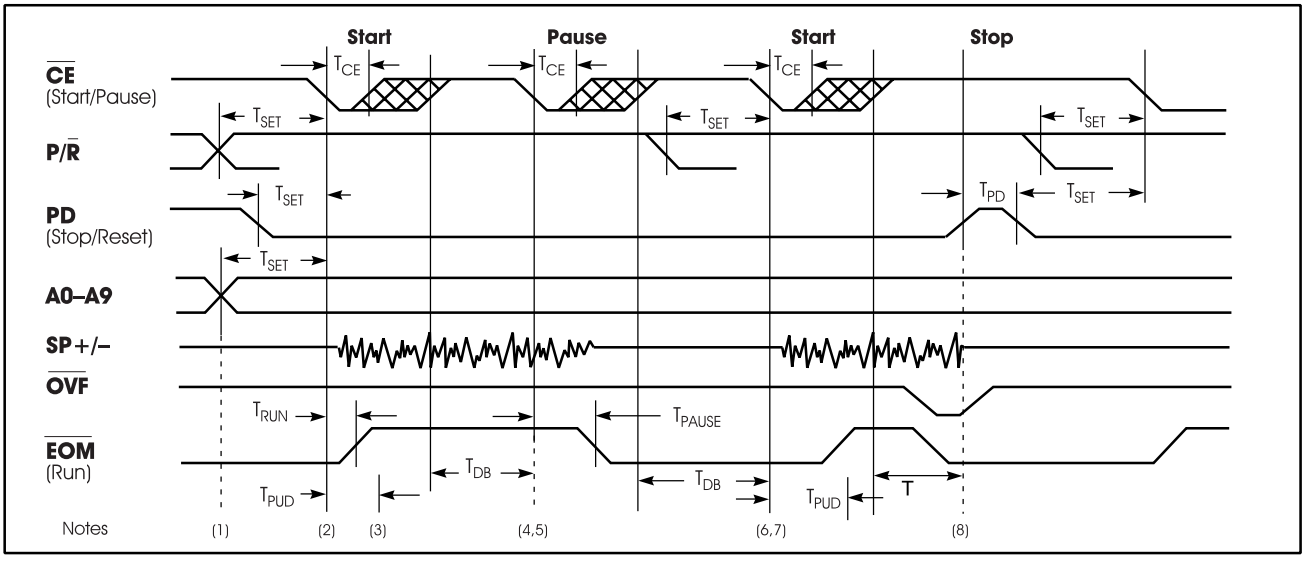


Figure 8: Push-Button Mode Playback



1. *A9, A8, and A6 = 1 for push-button operation.*
2. *The first $\overline{CE}$ LOW pulse performs a Start function.*
3. *The part will begin to play or record after a power-up delay T_{PUD}.*
4. *The part must have $\overline{CE}$ HIGH for a debounce period TDB before it will recognize another falling edge of $\overline{CE}$ and pause.*
5. *The second $\overline{CE}$ LOW pulse, and every even pulse thereafter, performs a Pause function.*
6. *Again, the part must have $\overline{CE}$ HIGH for a debounce period TDB before it will recognize another falling edge of CE, which would restart an operation. In addition, the part will not do an internal power down until CE is HIGH for the TDB time.*
7. *The third $\overline{CE}$ LOW pulse, and every odd pulse thereafter, performs a Resume function.*
8. *At any time, a HIGH level on PD will stop the current function, reset the address counter, and power down the device.*

DEVICE PHYSICAL DIMENSIONS

Figure 9: 28-Lead 8x13.4mm Plastic Thin Small Outline Package (TSOP) Type I (E)

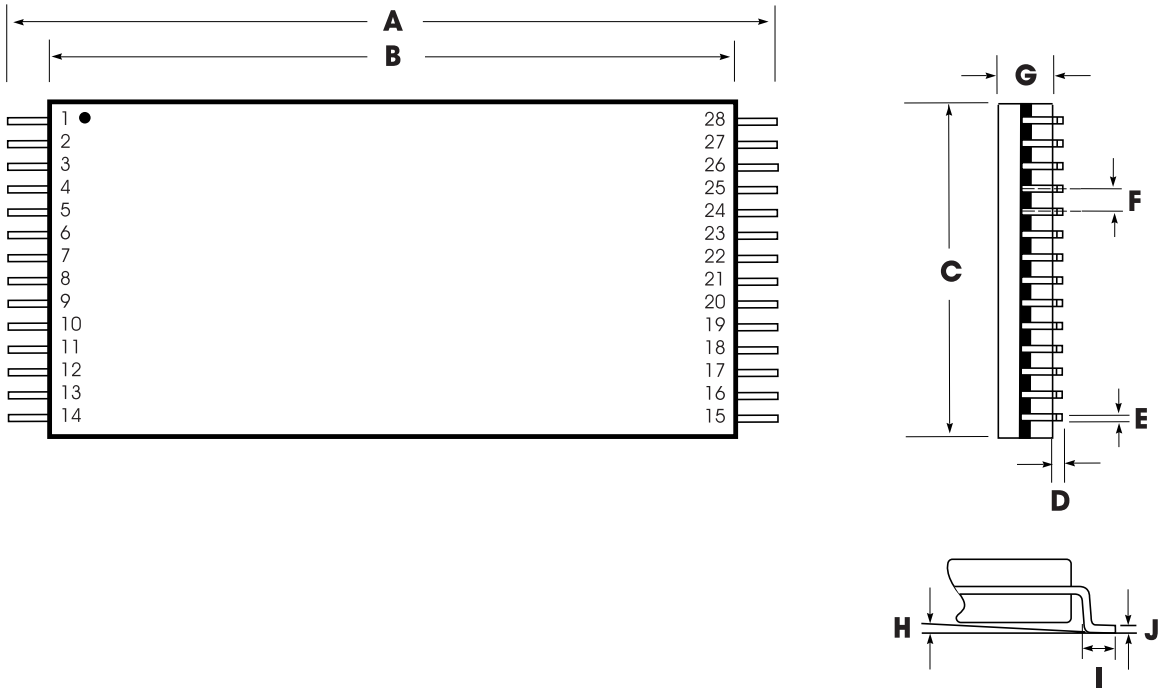


Table 17: Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	6°	0°	3°	6°
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 10: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

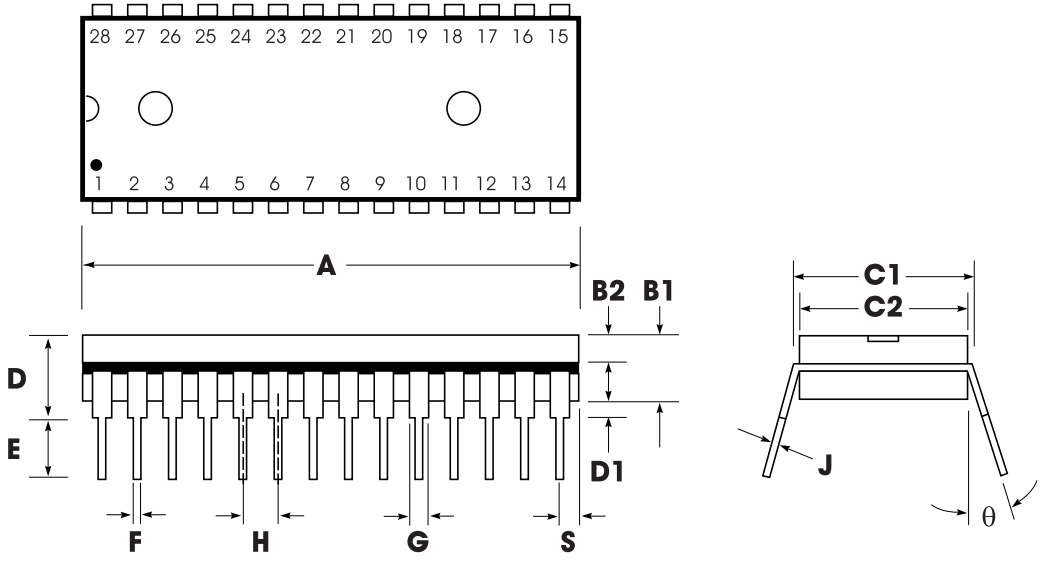


Table 18: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 11: 32-Lead 8x20mm Plastic Thin Small Outline Package (TSOP) Type I (T)

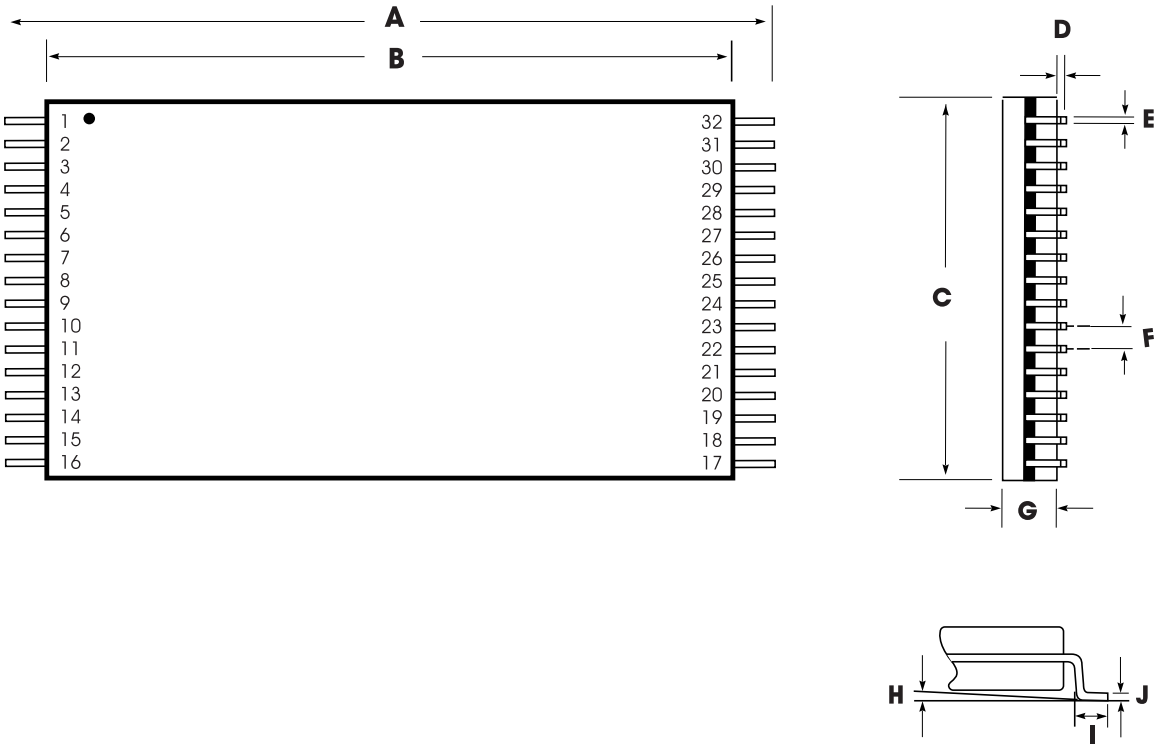


Table 19: Plastic Thin Small Outline Package (TSOP) Type I (T) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min		Max
A	0.780	0.787	0.795	19.80	20.00	20.20
B	0.720	0.724	0.728	18.30	18.40	18.50
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.006	0.009	0.011	0.17	0.22	0.27
F		0.0197			0.50	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	5°	0°	3°	5°
I	0.020	0.024	0.028	0.50	0.60	0.70
J	0.004		0.008	0.10		0.21

NOTE: *Lead coplanarity to be within 0.002 inches.*

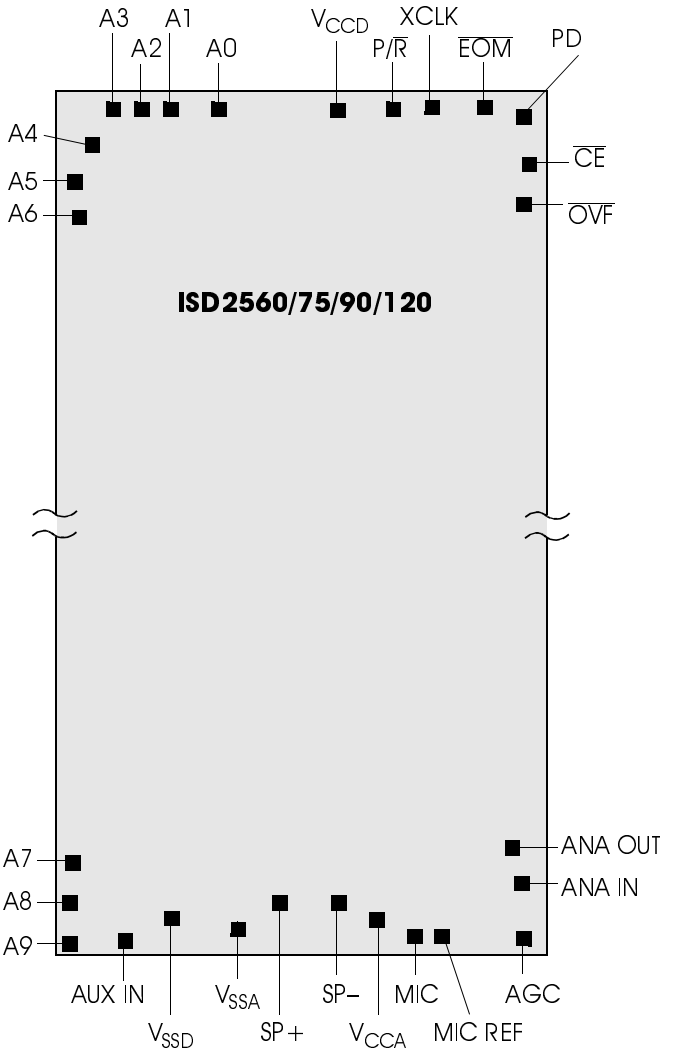
Figure 12: ISD2560/75/90/120 Products *Current* Bonding Physical Layout[1] (Unpackaged Die)

ISD2560/75/90/12[2]

I. Die Dimensions
X: 187 ±1 mils
Y: 399 ±1 mils

II. Die Thickness[2]
17.5 ±1 mils

III. Pad Opening
109 x 109 microns
4.3 x 4.3 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status.*

Table 20: ISD2560/75/90/120 Products *Current* PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	–1148.9	4898.2
A1	Address 1	–1406.9	4898.2
A2	Address 2	–1661.9	4898.2
A3	Address 3	–1916.9	4898.2
A4	Address 4	–2069.9	4608.2
A5	Address 5	–2194.9	4358.2
A6	Address 6	–2194.9	4108.2
A7	Address 7	–2194.9	–4212.3
A8	Address 8	–2194.9	–4456.3
A9	Address 9	–2076.4	–4897.3
AUX IN	Auxiliary Input	–1607.9	–4868.3
V_{SSD}	V_{SS} Digital Power Supply	–1343.9	–4850.8
V_{SSA}	V_{SS} Analog Power Supply	–551.9	–4884.8
SP+	Speaker Output +	–111.4	–4790.8
SP–	Speaker Output –	425.6	–4790.8
V_{CCA}	V_{CC} Analog Power Supply	865.1	–4848.32
MIC	Microphone Input	1320.7	–4897.3
MIC REF	Microphone Reference	1605.1	–4897.3
AGC	Automatic Gain Control	1877.6	–4871.3
ANA IN	Analog Input	2202.11	–4269.8
ANA OUT	Analog Output	2123.1	–3910.8
$\overline{OVF}$	Overflow Output	2142.6	4154.7
$\overline{CE}$	Chip Enable Input	2202.1	4558.7
PD	Power Down Input	2048.1	4898.2
$\overline{EOM}$	End of Message	1648.1	4865.7
XCLK	No Connect (optional)	1221.1	4898.2
P/$\overline{R}$	Playback/Record	965.6	4898.2
V_{CCD}	V_{CC} Digital Power Supply	646.1	4895.7

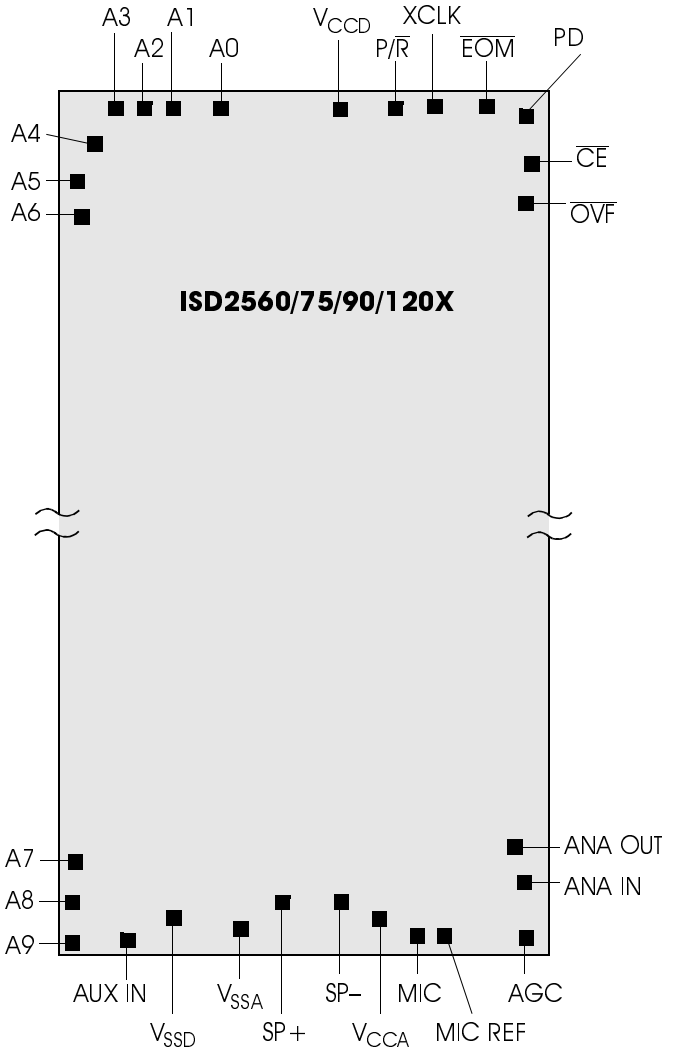
Figure 13: ISD2560/75/90/120 Products *Future* Bonding Physical Layout[1] (Unpackaged Die)

ISD2560/75/90/120X[2]

I. Die Dimensions
X: 149.5 ±1 mils
Y: 262.0 ±1 mils

II. Die Thickness[2]
11.8 ±.4 mils

III. Pad Opening
111 x 111 microns
4.4 x 4.4 mils



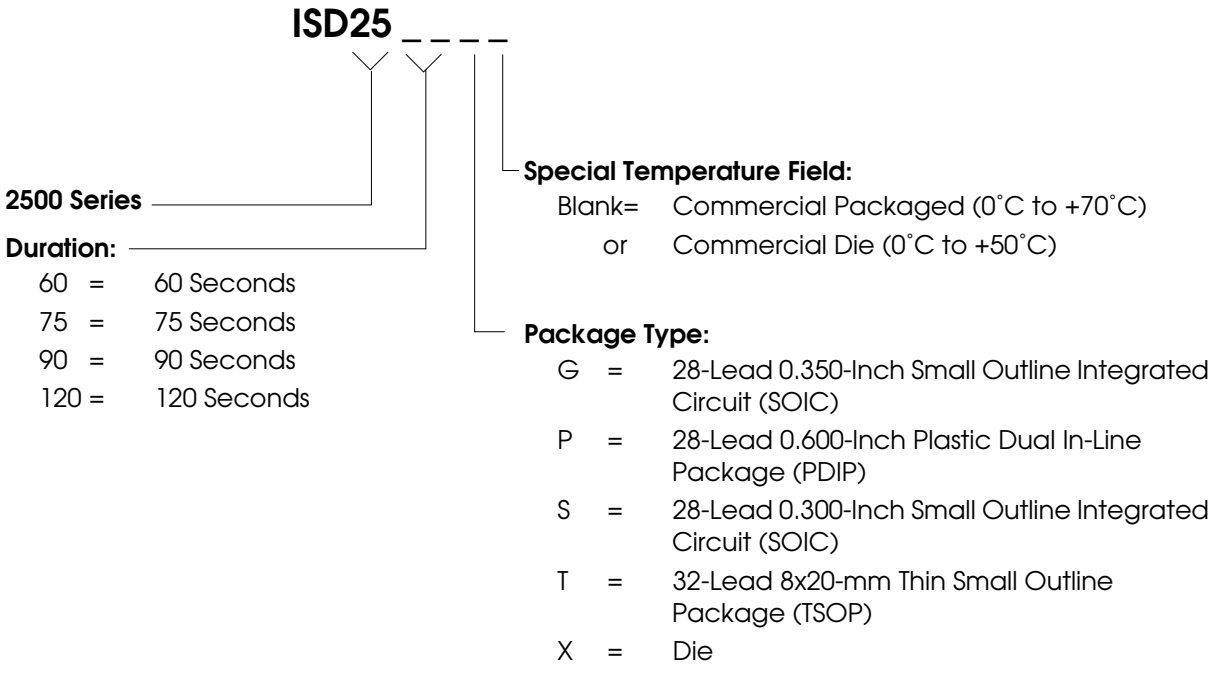
1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status and availability.*

Table 21: ISD2560/75/90/120 Products *Future* PIN/PAD Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
A0	Address 0	–897.9	3135.2
A1	Address 1	–1115.4	3135.2
A2	Address 2	–1331.0	3135.2
A3	Address 3	–1544.0	3135.2
A4	Address 4	–1640.4	2888.9
A5	Address 5	–1698.2	2671.0
A6	Address 6	–1698.2	2441.5
A7	Address 7	–1731.2	–2583.2
A8	Address 8	–1731.2	–2768.4
A9	Address 9	–1731.2	–3050.8
AUX IN	Auxiliary Input	–1410.1	–3115.7
V_{SSD}	V_{SS} Digital Power Supply	–1112.8	–3096.2
V_{SSA}	V_{SS} Analog Power Supply	–407.8	–3138.5
SP+	Speaker Output +	–47.4	–3067.7
SP–	Speaker Output –	386.9	–3067.7
V_{CCA}	V_{CC} Analog Power Supply	746.5	–3110.4
MIC	Microphone Input	1101.2	–3146.0
MIC REF	Microphone Reference	1294.7	–3146.0
AGC	Automatic Gain Control	1666.4	–3130.3
ANA IN	Analog Input	1728.6	–2654.0
ANA OUT	Analog Output	1700.9	–2411.0
$\overline{OVF}$	Overflow Output	1340.9	3121.7
$\overline{CE}$	Chip Enable Input	1726.7	2824.4
PD	Power Down Input	1730.5	3094.0
$\overline{EOM}$	End of Message	1340.9	3121.7
XCLK	No Connect (optional)	986.5	3160.7
P/$\overline{R}$	Playback/Record	807.2	3163.4
V_{CCD}	V_{CC} Digital Power Supply	544.7	3159.2

ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD2560/75/90/120 products, please refer to the following valid part numbers.

Part Number	Part Number	Part Number	Part Number
ISD2560G	ISD2575G	ISD2590G	ISD25120G
ISD2560P	ISD2575P	ISD2590P	ISD25120P
ISD2560S	ISD2575S	ISD2590S	ISD25120X
ISD2560T	ISD2575T	ISD2590T	
ISD2560X	ISD2575X	ISD2590X	

For the latest product information, access ISD's worldwide website at http://www.isd.com.