Integrated Circuit Systems, Inc.

ICS9DB202-01

PCI EXPRESS™ JITTER ATTENUATOR

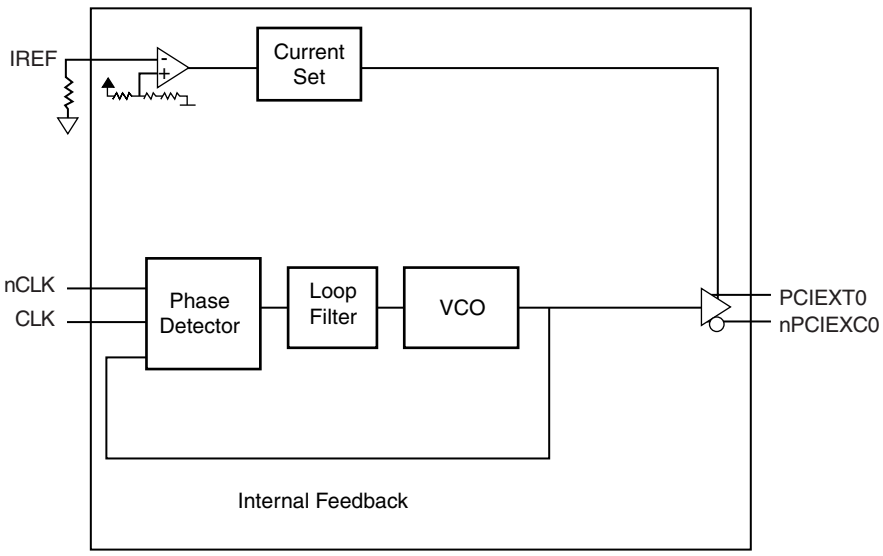
GENERAL DESCRIPTION

The ICS9DB202-01 is a high performance 1-to-1 Differential-to HCSL Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express™ systems, such as those found in desktop PCs, the PCI Express™ clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuating device may be necessary in order to reduce high frequency random and deterministic jitter components from the PLL synthesizer and from the system board.

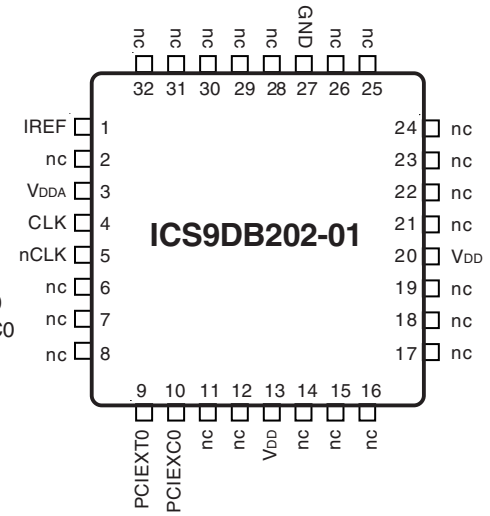
Features

- One 0.7V current mode differential HCSL output pair
- 1 differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 140MHz
- Cycle-to-cycle jitter: 30ps (maximum)
- RMS phase jitter @ 100MHz, (1.5MHz - 22MHz): 2.31ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package available
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead VFQFN
5mm x 5mm x 0.95 package body
K Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	IREF	Input		A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode PCIEX clock outputs.
2, 6, 7, 8, 11, 12, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 28, 29, 30, 31, 32	nc	Unused		No connect.
3	V_{DDA}	Power		Analog supply pin. Requires 24Ω series resistor.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
9, 10	PCIEXT0, PCIEXC0	Output		Differential output pairs. HCSL interface levels.
13, 20	V_{DD}	Power		Core supply pins.
27	GND	Power		Power supply ground.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	34.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C, RREF = 475Ω

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				112	mA
I_{DDA}	Analog Supply Current				22	mA

TABLE 3B. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C, RREF = 475Ω

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK, nCLK	V_{DD} = 3.465V, V_{IN} = 0V			150	µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.

TABLE 3C. HCSL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C, RREF = 475Ω

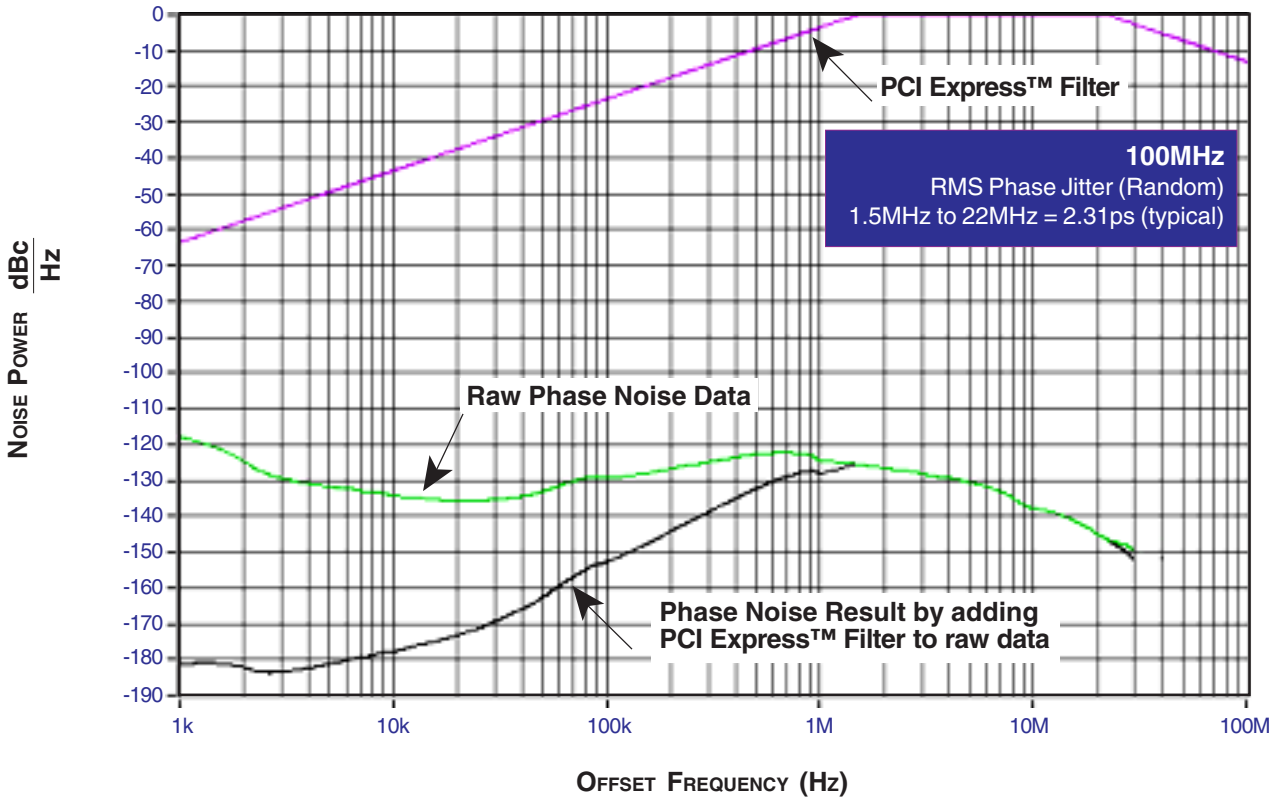
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{OH}	Output Current		12	14	16	mA
V_{OH}	Output High Voltage		745			mV
V_{OL}	Output Low Voltage				-5	mV
I_{OZ}	High Impedance Leakage Current		-10		10	µA
V_{OX}	Output Crossover Voltage		250		550	mV

TABLE 4. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = 0°C TO 70°C, RREF = 475Ω

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				140	MHz
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 1	Integration Range: 1.5MHz - 22MHz		2.31		ps
$t$jit(cc)	Cycle-to-Cycle Jitter				30	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Please refer to the Phase Noise Plot following this section.

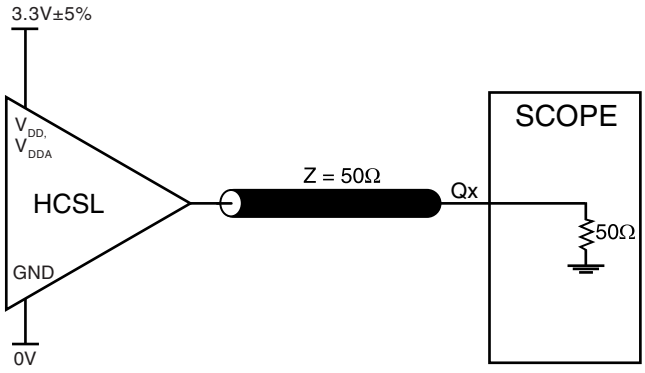
TYPICAL PHASE NOISE AT 100MHZ



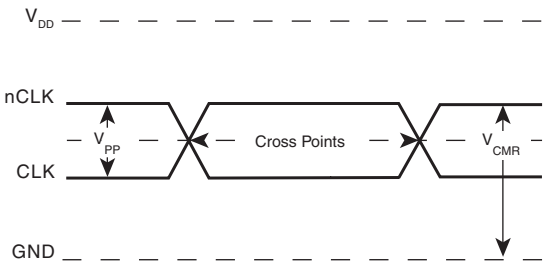
The illustrated phase noise plot was taken using a low phase noise signal generator, the noise floor of the signal generator is less than that of the device under test.

Using this configuration allows one to see the true spectral purity or phase noise performance of the PLL in the device under test. Due to the tracking ability of a PLL, it will track the input signal up to its loop bandwidth. Therefore, if the input phase noise is greater than that of the PLL, it will increase the output phase noise performance of the device. It is recommended that the phase noise performance of the input is verified in order to achieve the above phase noise performance.

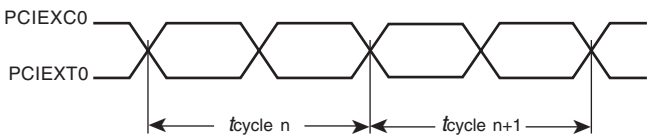
PARAMETER MEASUREMENT INFORMATION



3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT



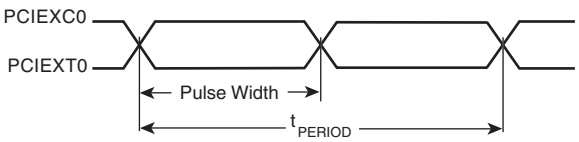
DIFFERENTIAL INPUT LEVEL



$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

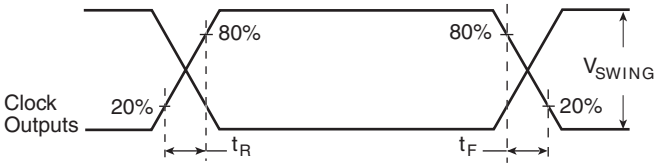
1000 Cycles

CYCLE-TO-CYCLE JITTER



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



HCSL OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS9DB202-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 24Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

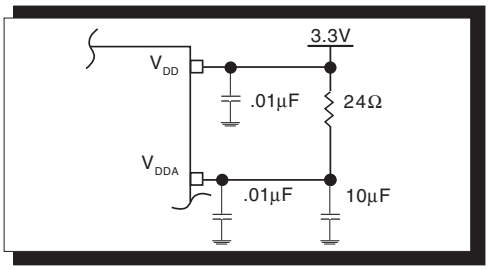


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

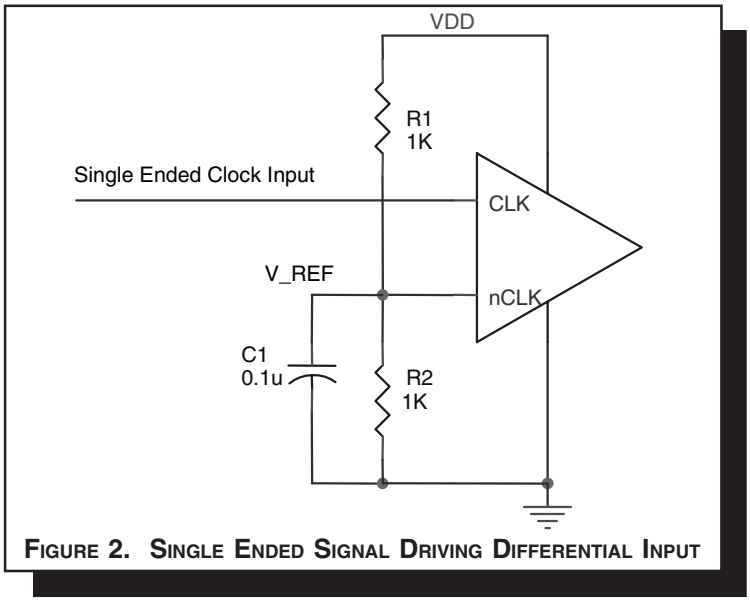


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

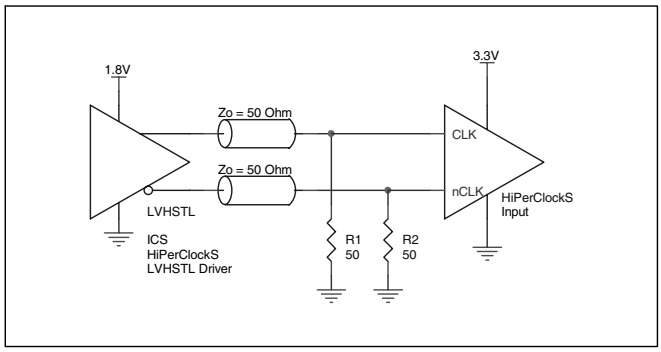


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

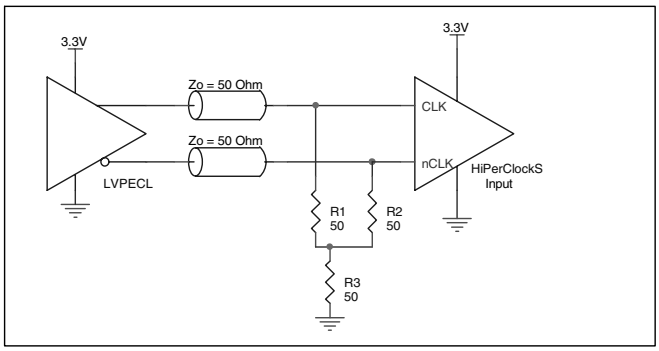


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

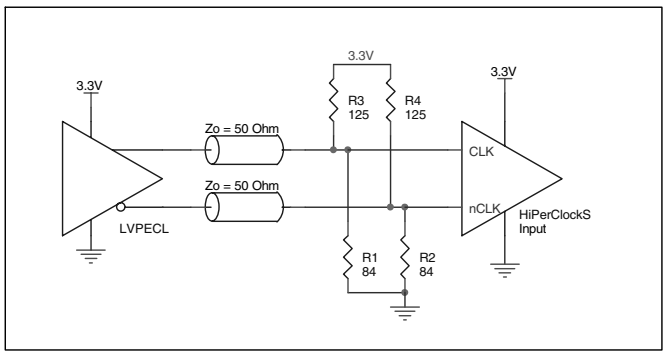


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

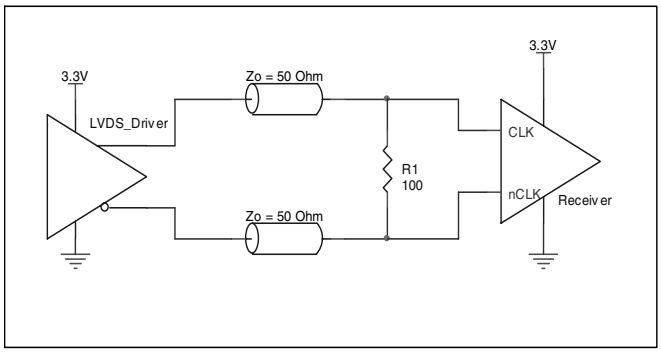


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

SCHEMATIC EXAMPLE

The schematic below illustrates two different terminations. Both are reliable and adequate. The PCI Express™ termination is recommended for all PCI Express™ application. The optional termination, which has a slightly better signal integrity, is recommended for all other applications.

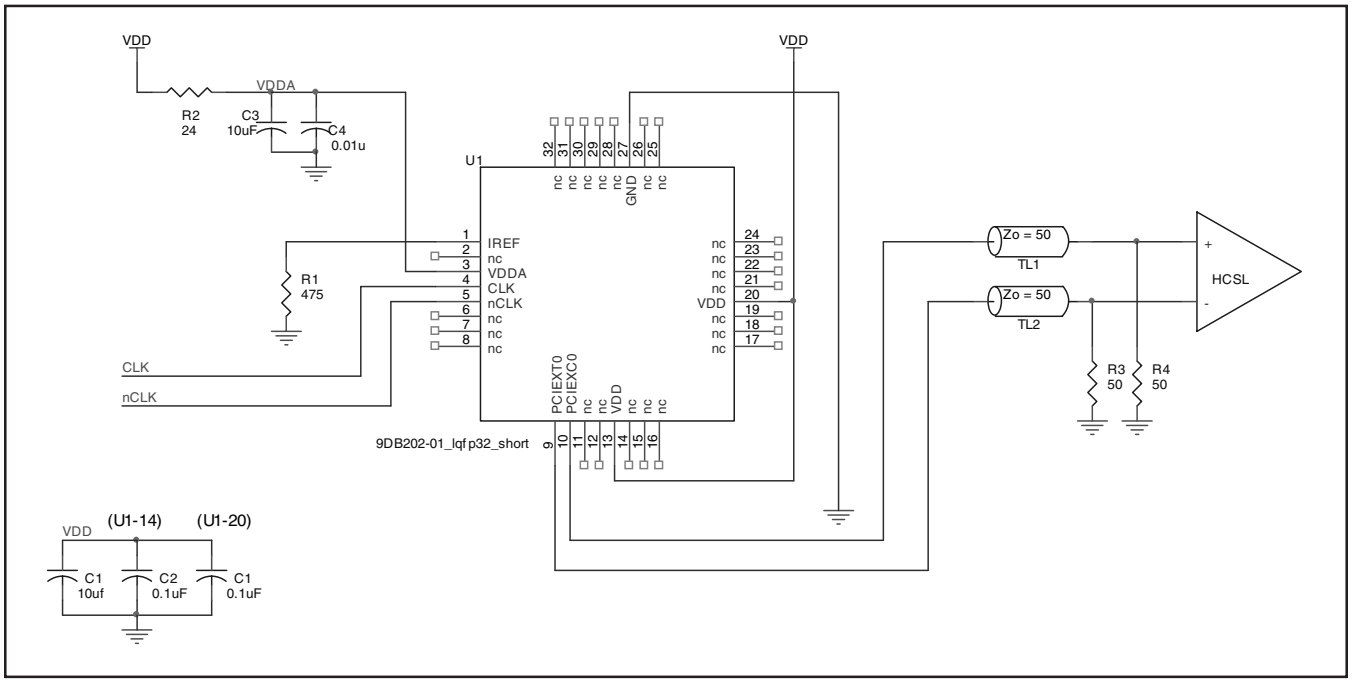


FIGURE 4. EXAMPLE OF ICS9DB202-01

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD VFQFN PACKAGE

θ_{JA} 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	34.8C/W

TRANSISTOR COUNT

The transistor count for ICS9DB202-01 is: 2471

PACKAGE OUTLINE - K SUFFIX FOR 32 LEAD VFQFN

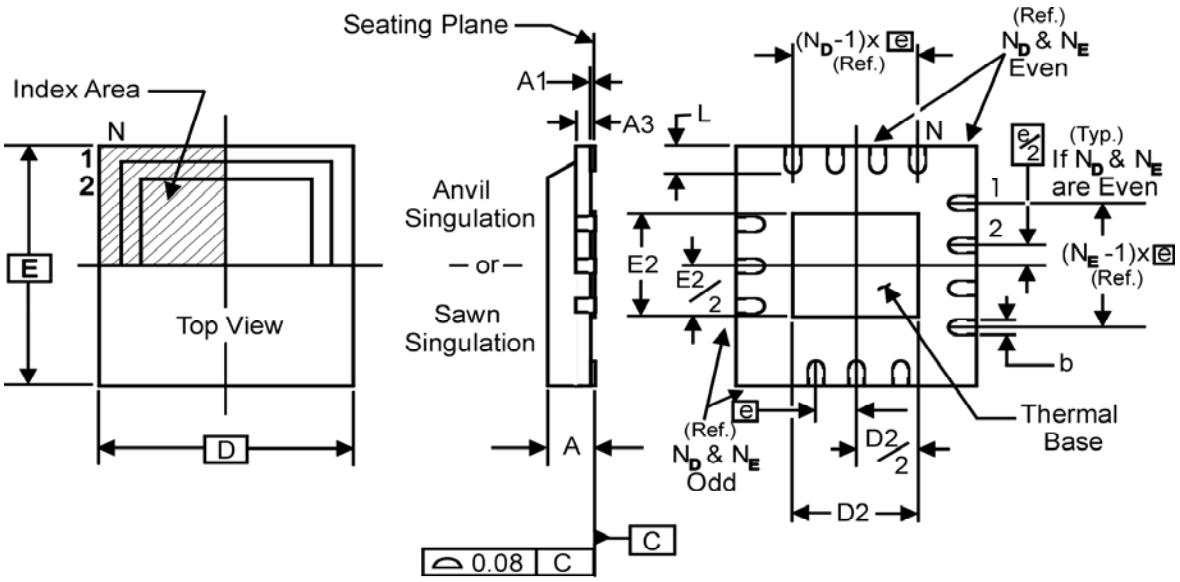


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	8	
N_E	8	
D	5.0	
D2	1.25	3.25
E	5.0	
E2	1.25	3.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS9DB202CK-01	ICS9DB202CK-01	32 Lead VFQFN	490 per Tray	0°C to 70°C
ICS9DB202CK-01T	ICS9DB202CK-01	32 Lead VFQFN on Tape and Reel	2500	0°C to 70°C
ICS9DB202CK-01LF	ICS9DB202CK-01L	32 Lead "Lead-Free" VFQFN	490 per Tray	0°C to 70°C
ICS9DB202CK-01LFT	ICS9DB202CK-01L	32 Lead "Lead-Free" VFQFN on Tape and Reel	2500	0°C to 70°C

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