



### GENERAL DESCRIPTION

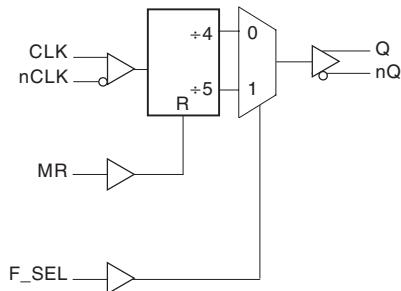


The ICS87354I is a high performance ÷4/÷5 Differential-to-3.3V LVPECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLK, nCLK pair can accept most standard differential input levels. The ICS87354I is characterized to operate from a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS87354I ideal for those clock distribution applications demanding well defined performance and repeatability.

### FEATURES

- One differential 3.3V LVPECL output
- One CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum clock input frequency: 1GHz
- Translates any single ended input signal (LVCMOS, LVTTTL, GTL) to LVPECL levels with resistor bias on nCLK input
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 2.1ns (maximum)
- LVPECL mode operating voltage supply range:  $V_{CC} = 3.0V$  to  $3.465V$ ,  $V_{EE} = 0V$
- $-40^{\circ}C$  to  $85^{\circ}C$  ambient operating temperature
- Lead-Free package fully RoHS compliant

### BLOCK DIAGRAM



### PIN ASSIGNMENT

CLK	1	8	V <sub>CC</sub>
nCLK	2	7	Q
MR	3	6	nQ
F_SEL	4	5	V <sub>EE</sub>

**ICS87354I**  
**8-Lead SOIC**  
 3.90mm x 4.90mm x 1.37mm package body  
**M Package**  
 Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	CLK	Input	Pulldown	Non-inverting differential clock input.
2	nCLK	Input	Pullup	Inverting differential clock input.
3	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output (Q) to go low and the inverted output (nQ) to go high. When logic LOW, the internal dividers and the output are enabled. LVCMOS / LVTTTL interface levels. See Table 3.
4	F_SEL	Input	Pulldown	Selects divider value for Q, nQ outputs as described in Table 3. LVCMOS / LVTTTL interface levels.
5	V <sub>EE</sub>	Power		Negative supply pin.
6, 7	Q, nQ	Output		Differential output pair. LVPECL interface levels.
8	V <sub>CC</sub>	Power		Positive supply pin.

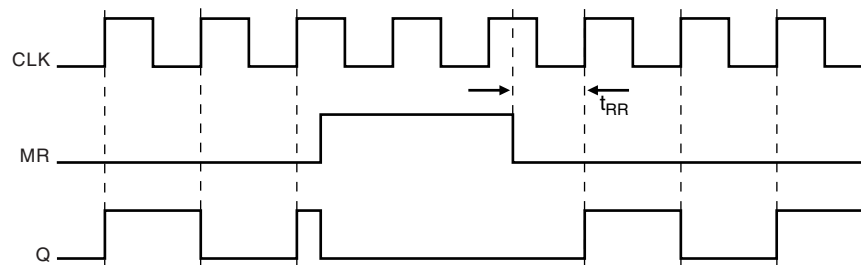
NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**TABLE 3. FUNCTION TABLE**

MR	F_SEL	Divide Value
1	X	Reset: Q output low, nQ output high
0	0	÷4
0	1	÷5



**FIGURE 1. TIMING DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_i$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_o$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	112.7°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.0V$  TO  $3.465V$ ,  $V_{EE} = 0$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		3.0	3.3	3.465	V
$I_{EE}$	Power Supply Current				104	mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = 3.0V$  TO  $3.465V$ ,  $V_{EE} = 0$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	MR, F_SEL $V_{CC} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	MR, F_SEL $V_{CC} = 3.465V, V_{IN} = 0V$	-5			$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = 3.0V$  TO  $3.465V$ ,  $V_{EE} = 0$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK $V_{CC} = V_{IN} = 3.465V$			150	$\mu A$
		nCLK $V_{CC} = V_{IN} = 3.465V$			5	$\mu A$
$I_{IL}$	Input Low Current	CLK $V_{CC} = 3.465V, V_{IN} = 0V$	-5			$\mu A$
		nCLK $V_{CC} = 3.465V, V_{IN} = 0V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{CC} + 0.3V$ .



**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.0V$  TO  $3.465V$ ,  $V_{EE} = 0$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

**TABLE 5. AC CHARACTERISTICS,  $V_{CC} = 3.0V$  TO  $3.465V$ ,  $V_{EE} = 0$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{CLK}$	Clock Input Frequency				1	GHz
$t_{PD}$	Propagation Delay; NOTE 1	CLK to Q (Dif)	1.7		2.1	ns
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 3				300	ps
$t_{RR}$	Reset Recovery Time				400	ps
$t_{PW}$	Minimum Input Pulse Width	CLK	550			ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		600	ps
odc	Output Duty Cycle		48		52	%

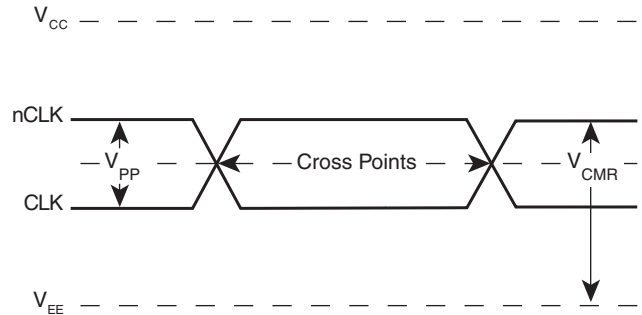
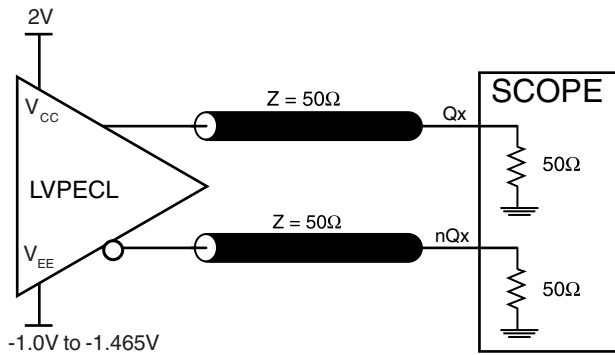
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

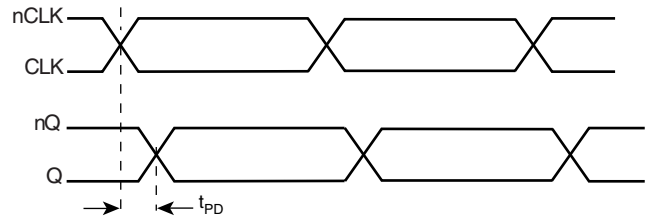
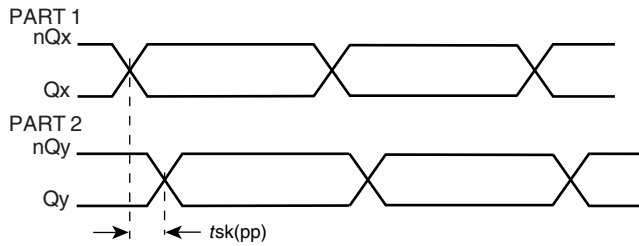


## PARAMETER MEASUREMENT INFORMATION



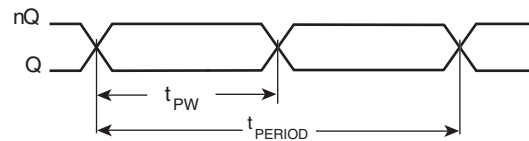
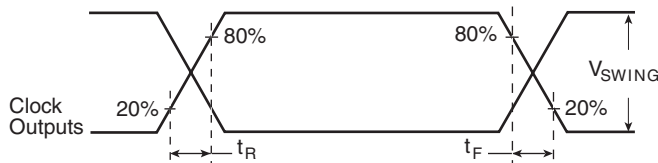
### 3.3V OUTPUT LOAD AC TEST CIRCUIT

### DIFFERENTIAL INPUT LEVEL



### PART-TO-PART SKEW

### PROPAGATION DELAY



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

### OUTPUT RISE/FALL TIME

### OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

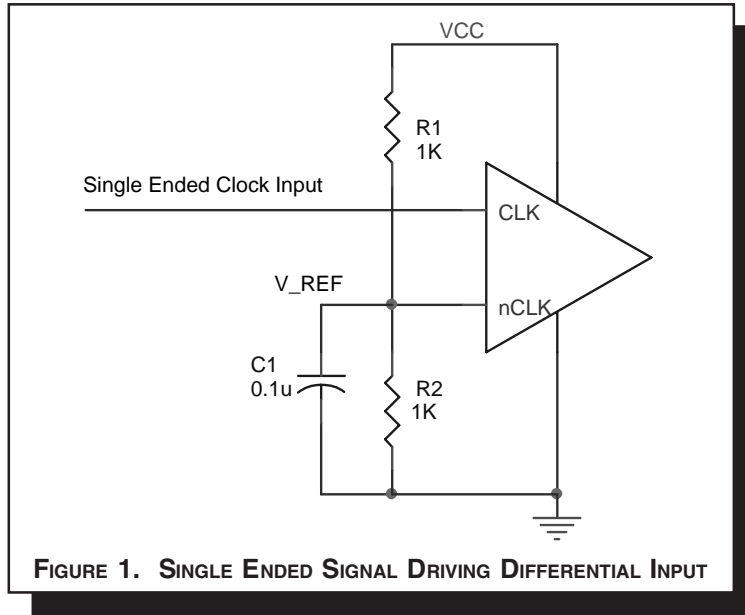


## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin.

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

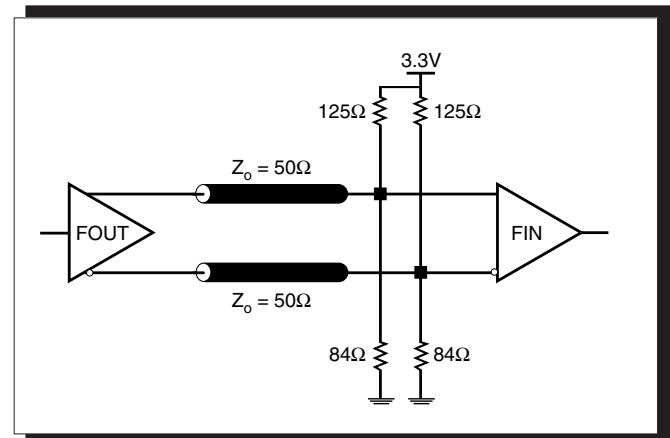
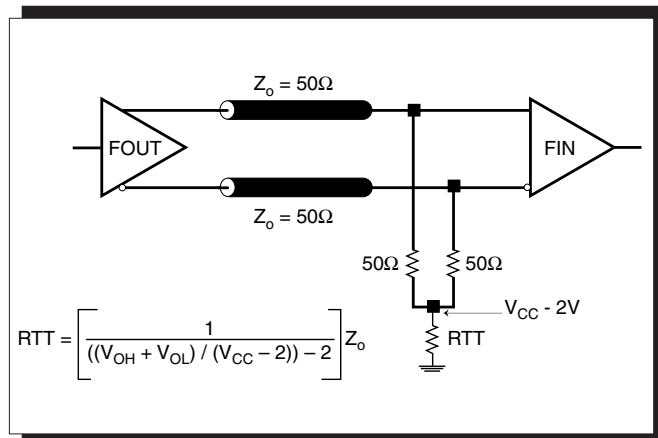


### TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 2A and 2B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

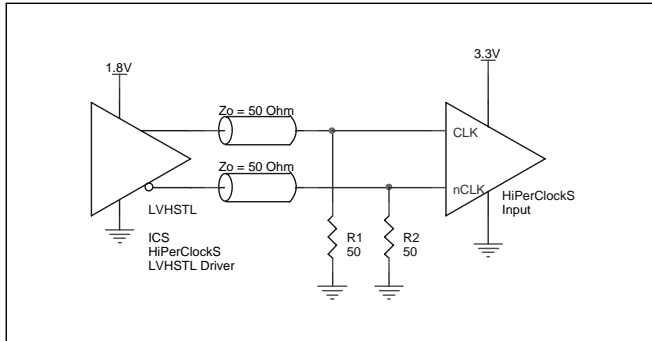




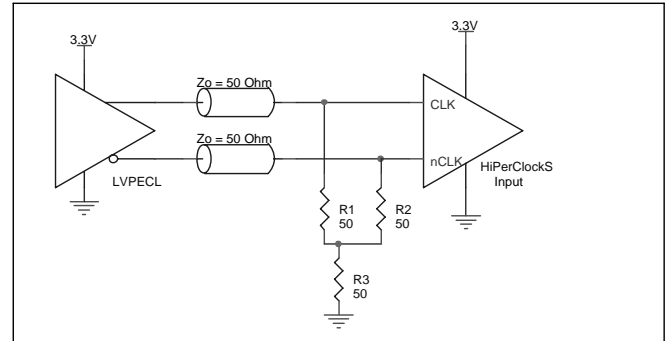
### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

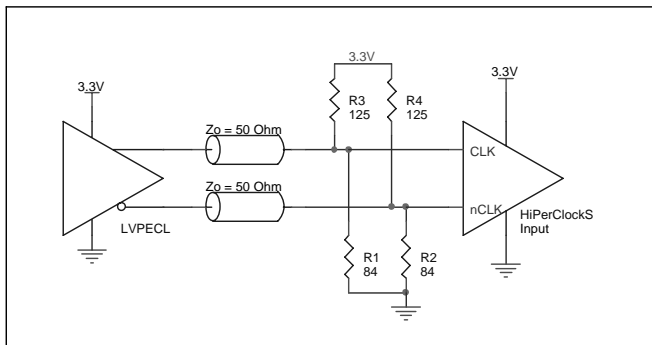
here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



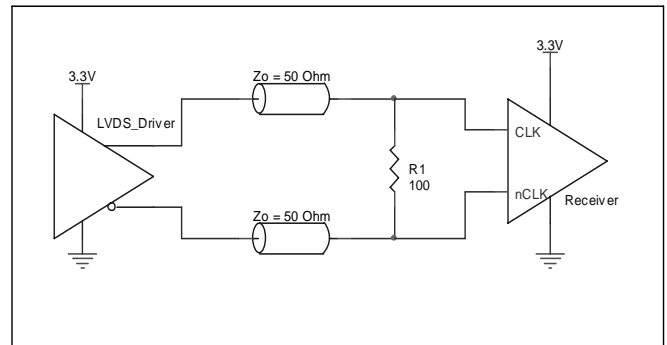
**FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



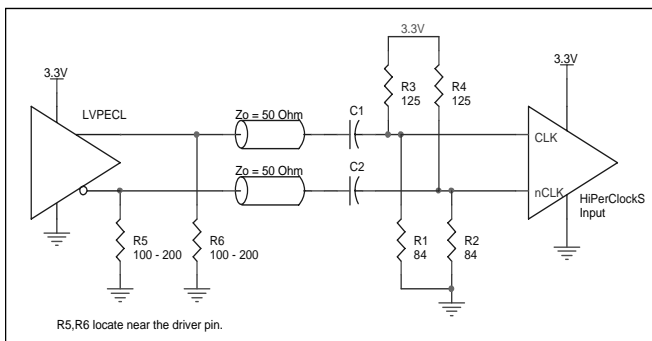
**FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



**FIGURE 3E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS87354I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS87354I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 104mA = 360mW$
- Power (outputs)<sub>MAX</sub> = **3.465mW/Loaded Output pair**

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 360mW + 30mW = 390mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.390W * 103.3^\circ C/W = 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN SOIC, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

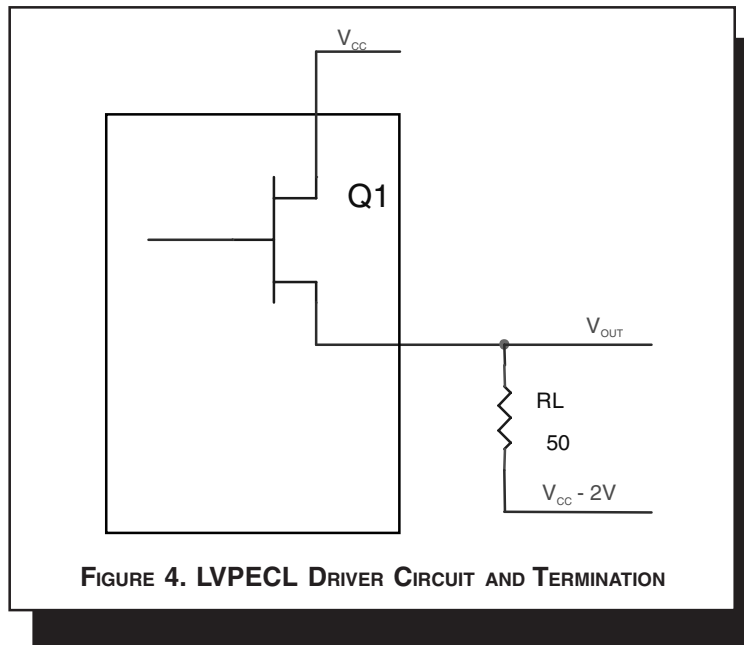




### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V$   
 $(V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$   
 $(V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V$

$Pd\_H$  is power dissipation when the output drives high.  
 $Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = 30mW$



## RELIABILITY INFORMATION

**TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD SOIC**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS87354I is: 1745



PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

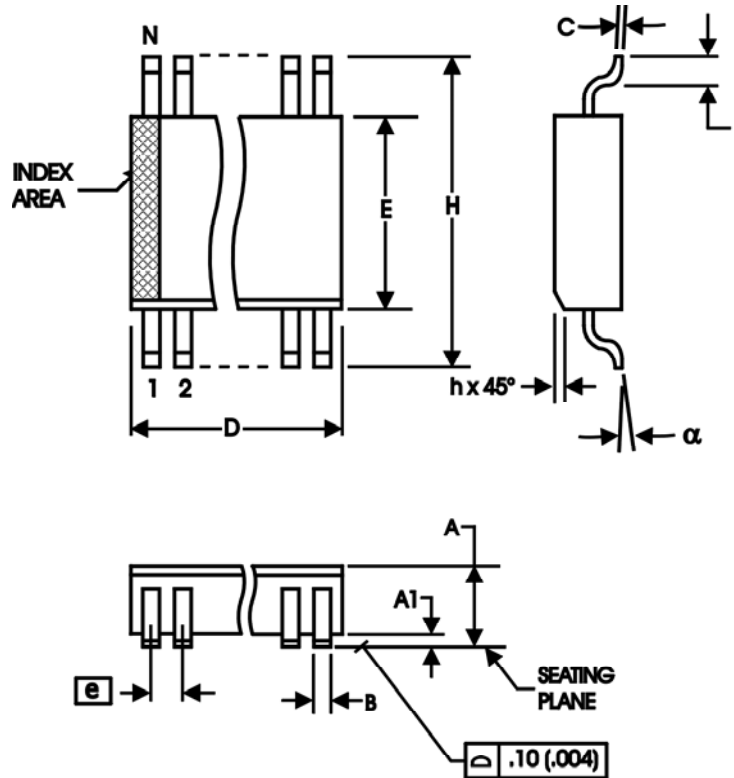


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
$\alpha$	0°	8°

Reference Document: JEDEC Publication 95, MS-012



Integrated  
Circuit  
Systems, Inc.

# ICS87354I

## ÷4/÷5 DIFFERENTIAL-TO- 3.3V LVPECL CLOCK GENERATOR

**TABLE 8. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87354AMI	87354AMI	8 lead SOIC	tube	-40°C to 85°C
ICS87354AMIT	87354AMI	8 lead SOIC	2500 tape & reel	-40°C to 85°C
ICS87354AMILF	87354AIL	8 lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS87354AMILFT	87354AIL	8 lead "Lead-Free" SOIC	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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